What is claimed is:

1. A system for testing a device under test (DUT), the DUT comprising a first core and a second core, the system comprising:

channels for connecting to a number of pins on the DUT, the channels for sending test data to the DUT and for receiving measurement data from the DUT based on the test data;

wherein the measurement data comprises time-division-multiplexed (TDM) data comprised of successive data packets received from the DUT over the channels as part of a bitstream, where each data packet comprises a first number of bits from the first core and a second number of bits from the second core, where the data packets are transmitted in time slots with each time slot corresponding to a transmission of the bitstream on the number of pins, and where the TDM data is repeated in a pattern on the channels every predetermined number of time slots; and

circuitry associated with the channels to compare the measurement data with expected data, and to determine pass/fail status for the first core and for the second core based on the comparison;

wherein the circuitry is configured to determine fail counts for the first core and for the second core based on the comparison, with a fail count indicating how many times that the first core or the second core has failed a test; and

wherein the circuitry is configured to limit storage of subsequently-received measurement data for the first core or for the second core when the fail count exceeds a threshold number for the first core or the second core.

2. The system of claim 1, wherein limiting storage comprises ignoring the subsequently-received measurement data for the first core or the second core.

3. The system of claim 1, wherein limiting storage comprises not storing, in memory, the subsequently-received measurement data for the first core or the second core.

4. The system of claim 1, wherein limiting storage comprises limiting a number of fails in the first core or the second core that affect how many cycles of the subsequently-received measurement data are stored in memory for the first core or the second core, where a cycle comprises a time slot and where a fail comprises a single failure of the test.

5. The method of claim 1, wherein the circuitry is configured to output the fail count.

6. The system of claim 1, further comprising memory; wherein at least some cycles of measurement data from the first core and the second core are stored in a results log in the memory, where a cycle corresponds to a time slot.

7. The system of claim 1, wherein the first number of bits and the second number of bits are each different, and cumulatively different from a number of the pins such that parts of two different data packets are contained in at least some of the time slots.

8. The system of claim 1, wherein the predetermined number of time slots is greater than one time slot.

9. The system of claim 1, wherein the circuitry is configured to determine pass/fail status by accumulating pass/fail data associated with a time slot in a current frame of data with prior pass/fail data for time slots in prior frames of data, where a frame of data comprises the predetermined number of time slots.

10. The system of claim 9, wherein the pass/fail data is based on a cumulative status for the first core and the second core over multiple repeated patterns of time slots.

11. The system of claim 1, wherein determining the fail counts comprises separately counting a number of times that the first core or the second core failed the test.

12. The method of claim 11, wherein counting comprises incrementing an address of memory based on a time slot.

13. The method of claim 11, wherein counting comprises incrementing an address of a first memory based on a time slot, where that memory maps the time slot to a core number, and where that core number addresses a second memory.

14. The system of claim 1, further comprising memory; wherein the circuitry is configured to store, in the memory, a fail count per core following a predetermined number of cycles of the measurement data.

15. A system for testing a device under test (DUT), the DUT comprising a first core and a second core, the system comprising:

channels for connecting to a number of pins on the DUT, the channels for sending test data to the DUT and for receiving measurement data from the DUT based on the test data;

wherein the measurement data comprises time-division-multiplexed (TDM) data comprised of successive data packets received from the DUT over the channels as part of a bitstream, where each data packet comprises a first number of bits from the first core and a second number of bits from the second core, where the data packets are transmitted in time slots with each time slot corresponding to transmission

of the bitstream on the number of pins, and where the TDM data is repeated in a pattern on the channels every predetermined number of time slots; and

circuitry associated with the channels to compare the measurement data with expected data, and to determine fail counts per core based on the comparison, with a fail count indicating how many times that the first core or the second core has failed a test;

wherein the circuitry is configured to limit storage of subsequently-received measurement data for the first core or for the second core when the fail count exceeds a threshold number for the first core or the second core.

16. The system of claim 15, wherein the circuitry is configured to compare the measurement data with expected data by aggregating pass/fail data associated with a time slot in a current frame of data with prior pass/fail data for time slots in prior frames of data, where a frame of data comprises the predetermined number of time slots.

17. The system of claim 16, wherein the pass/fail data is based on a cumulative status per time slot.

18. The system of claim 15, wherein limiting storage comprises ignoring the subsequently-received measurement data for the first core or the second core.

19. The system of claim 15, wherein limiting storage comprises not storing the subsequently-received measurement data for the first core or the second core.

20. A system for testing a device under test (DUT), the DUT comprising a first core and a second core, the system comprising:

channels for connecting to a number of pins on the DUT, the channels for sending test data to the DUT and for receiving measurement data from the DUT based on the test data;

wherein the measurement data comprises time-division-multiplexed (TDM) data comprised of successive data packets received from the DUT over the channels as part of a bitstream, where each data packet comprises a first number of bits from the first core and a second number of bits from the second core, where the data packets are transmitted in time slots with each time slot corresponding to a transmission of the bitstream on the number of pins, and where the TDM data is repeated in a pattern on the channels every predetermined number of time slots, and where each of the channels is configured to transmit data from both the first core and the second core; and

circuitry associated with the channels to mask data from the first core or the second core based on user input, where masking comprises not storing, in memory, data from one of the channels for a selected one of the first core or the second core and storing data from the one of the channels for a non-selected one of the first core or the second core.

21. The system of claim 1, wherein the circuitry comprises solid state circuitry.

22. The system of claim 1, wherein the circuitry comprises means for: (i) comparing the measurement data with expected data, (ii) determining pass/fail status for the first core and for the second core based on the comparison, (iii) determining the fail counts; and (iv) limiting storage of subsequently-received measurement data.

23. The system of claim 1, wherein the circuitry comprises one or more processing devices.