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(54) SWITCHING SYSTEM

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED of 195 Broadway, New York City, New York State, United States of America, a Corporation organized and existing under the laws of the State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to telephone switching systems.

Switching systems are known in which scanners and digit registers communicate with line circuits, trunk circuits, and other service circuits by means of control conductors that are often termed code leads. Control signals and data are transmitted over these conductors to assist these systems in their call serving operations.

Patent No. 1,108,701 (Abbott) discloses a Private Branch Exchange (PBX) system having a set of line side code leads which interconnect line circuits with a line scanner as well as with the readout circuitry of digit registers. The system disclosed also has a set of trunk side code leads which interconnect a trunk side scanner with trunk circuits and with the selection circuitry of the digit registers. The use of code lead signalling as taught in the Abbott patent and, in particular, the use of line side code leads, minimizes or eliminates the need for the costly and complex connectors and interconnecting arrangements of earlier prior art systems.

Signals are initially transmitted over the line side code leads from a line scanner in the Abbott system to identify a calling line circuit that has gone off-hook and is requesting service. The identification of the line circuit is required at this time so that it may be connected to a digit register. Signals are subsequently transmitted from the line scanner via the same code leads to reidentify the calling line circuit after the digits required by the PBX to serve the call have been dialed into a register. A reidentifica-

tion of the line circuit is required at this time so that it may be connected to a trunk circuit. The line side code leads are also used to select a called line circuit. This is done by gating signals representing the called number from the output of the register onto the line side code leads. The trunk side code leads are used in conjunction with a trunk side scanner to select idle trunk side circuits such as registers, trunk circuits, tone circuits, etc.

The system disclosed in the Abbott patent uses an end marked network which establishes a connection between a line side and a trunk side circuit in response to the application of a marking potential to the network appearances of the circuits to be interconnected. A calling line circuit that is connected to a register is identified by what is termed a call-back operation after the called number has been dialed. The register determines that it has received all the digits that will be dialed and, in response thereto, applies a call-back potential through the network to the calling line circuit. This potential partially enables or primes logic elements within the line circuit so that it may be identified by a subsequent line scanning operation.

Although the Abbott system satisfactorily performs its intended functions, its use of code leads is limited to systems that have end marked networks as well as call-back signalling facilities. This requirement tends to limit the applicability of code lead signalling and control.

It is therefore, an object of the invention to provide an improved switching system.

According to the present invention there is provided a switching system comprising a switching network having a line side and a trunk side, a plurality of line circuits connected to said line side, register means and a plurality of trunk circuits connected to said trunk side, controller means, a first set of code leads interconnecting said line circuits with said register means and the controller means, means for applying signals to said code leads from said controller means in

order to identify a calling one of said line circuits requesting service, means for applying signals identifying said calling line circuit from said code leads to the register means, means for applying signals from said register means to said code leads in order to select a called one of the line circuits, means for subsequently applying calling line identification signals from said register means to said code leads in order to reidentify said calling line circuit, and means responsive to the signals applied to said first code leads for controlling the establishment of network paths via a selected trunk circuit.

One system embodying the invention uses code leads for transmitting control signals and data but does not require the use of an end marked network or call-back signalling. Instead, the system uses a conventional crossbar type switching network; it further uses the code leads and signals from a digit register to identify a calling line circuit.

The system includes a set of line side code leads which interconnect a line scanner with line circuits as well as with the output circuitry of digit registers. The system further includes a set of trunk side code leads which interconnect a trunk side scanner with the selection control circuitry of the digit registers as well as with other trunk side service circuits such as trunk circuits, tone circuits, etc. Both sets of code leads also connect their respective scanners with the network controller.

A calling line is identified at the initiation of a call when the system controller detects the off-hook state of the line circuit, activates the line scanner, and causes it to scan the line circuits. When the calling line is scanned, the scanner applies coded signals to the line side code leads that match the number of the calling line circuit. This activates logic circuitry within the line circuit which, in turn, transmits a signal back to the system controller to stop the scanner. The common control then activates the trunk side scanner which applies scanning signals to the trunk side code leads to select an idle register for use on the call. After the register is selected, the line scanner output signals, which are still on the line side code leads and which represent the calling line, are gated into and stored in the selected register.

The signals on the line side code leads at this time identify the calling line circuit; the signals on the trunk side code leads identify the selected register. Both sets of code leads extend to the control circuitry of the switching network. Next, the system controller transmits an enable signal to the network to cause it to establish a connection from the calling line circuit to the selected register under control of the code lead information. The line scanner and the trunk scanner are reset upon completion of the network con-

nection so that they may be free to serve other calls.

The register signals the common control when it has received all the dialed digits it requires to serve the call. The register and the common control then analyze these digits to determine what circuit actions are required. If the prefix digit 9 is dialed, a connection to a central office trunk circuit is required; if a 0 is dialed, a connection to the attendant is required, etc. Let it be assumed that the dialed digits represent an intra-PBX call and that, therefore, a connection to an idle intercom trunk circuit is required. After this determination is made, the called number information is applied by the register to the line side code leads. This activates logic circuitry within the called line circuit which returns a signal to the system controller indicating whether the called line is currently busy or idle. If it is idle, the controller (1) activates the trunk side scanner which applies scanning signals to the trunk side code leads to select an idle intercom trunk circuit, and (2) applies an enable or control potential to the network to cause it to establish a path between the called line circuit and the selected trunk circuit. This path is established under control of the signals currently applied by the scanners to the line side and trunk side code leads.

Next, the called line information is removed and the calling line information is gated out of the digit register onto the line side code leads. This activates logic circuitry in the calling line circuit which generates class mark information indicating the type of call service to which the calling line is entitled. At this time, the line side code lead signals identify the calling line; the signals on the trunk side code leads identify the selected trunk circuit. This line side and trunk side code lead information is applied to the input circuitry of the switching network which establishes a path between the calling line circuit and the selected trunk circuit. Since the called line circuit is also connected to this trunk circuit, the calling and called stations may converse when the called party answers.

The storage of the calling number in the register and the gating of this number from the register back onto the code leads permits the system to avoid the complexities of call-back signalling and to identify the calling line circuit by simpler means. Also, the connection of the code leads to the input circuitry of the network provides an efficient means of transmitting to the network the information it requires for the establishment of call connections.

A feature of the embodiment is that code lead signalling is used to identify a calling line circuit when it goes off-hook at the beginning of a call, as well as to reidentify

the line circuit when the line circuit is to be connected to a trunk circuit.

A further feature is that the signals applied to the code leads to identify a calling line circuit at the initiation of a call are gated into and stored by the register to which the calling line circuit is connected, and are subsequently gated out from the register back onto the line side code leads to re-identify the calling line circuit.

A further feature is that the code leads are connected to the network controller to supply the signals the network requires for the establishment of call connections.

A further feature is the provision of circuitry including logic circuitry in a calling line circuit which responds to the signals applied by the register to the line side code leads for generating calling line class information.

A further feature is the provision of line side and trunk side code leads for identifying calling line circuits, for selecting called line circuits, for selecting trunk side circuits, as well as for supplying the code lead signals to the switching network as path control signals.

A further feature is the provision of line side and trunk side code leads in which (1) signals are applied to the line side code leads by a scanner to identify a calling line circuit when it goes off-hook, (2) signals are applied to the trunk side code leads by a trunk side scanner to select a register to which the calling line circuit is to be connected by the network, (3) the line side and trunk side code lead signals are applied to a network controller to establish a network path between the calling line circuit and the selected register, (4) the line side code lead signals identifying the calling line are transmitted to and stored in the register for subsequent use on the call, (5) the called number information dialed into the register is applied to the line side code leads to select a called line circuit and to determine whether the called line circuit is currently busy or idle, (6) signals are subsequently applied by the trunk side scanner to the trunk side code leads to select an idle trunk side circuit for use on the call, (7) the line side code leads signals identifying the called line circuit and the trunk side code lead signals identifying the selected trunk circuit are applied to the network controller to establish a network path between the called line circuit and the selected trunk circuit, (8) the calling line information stored in the register is applied back onto the line side code leads to reidentify the calling line circuit and to generate calling line class information, and (9) the line side code lead signals identifying the calling line circuit and the trunk side code lead signals identifying the selected trunk circuit are applied to the network controller to establish a path be-

tween the calling line circuit and the selected trunk circuit.

One advantage which may be found in systems embodying the invention is in the use of code lead signalling and control without the requirement for an end marked switching network or call back signalling facilities.

An embodiment of the invention will now be described with reference to the accompanying drawings in which:—

Fig. 1A, 1B, 1C, and 1D, when arranged as shown on Fig. 1E, illustrate a specific embodiment of our invention;

Fig. 2A, 2B, 2C, 2D, 2E, and 2F, when arranged as shown on Fig. 2G, illustrate additional details of the embodiment of our invention;

Fig. 3A, 3B, 3C, 3D, 3E, 3F, and 3G illustrate additional details of the logic elements used;

Fig. 4A, 4B, 4C, and 4D illustrate additional details of the sequence circuit shown in the drawing; and

Fig. 5A and 5B disclose additional details of the mode control shown in Fig. 2E.

General Description—

Fig. 1A, 1B, 1C and 1D

Fig. 1A through 1D, when arranged with respect to each other as shown in Fig. 1E, disclose a specific embodiment of the invention. The embodiment is in the form of a wired logic, electronically controlled type PBX system similar to that disclosed in detail in the Abbott patent referred to above.

The system includes a switching network 112 including a network controller 112A. If desired, the network may be of the well-known crossbar switch type. The paths that are established are controlled by signals transmitted from the rest of the system over conductors 103 and 107 to the controller 112A. The system further includes a plurality of stations ST00 through ST99 each of which is connected to one of line circuits LC00 through LC99. Each line circuit is connected by various conductors to common control 113 on Fig. 1B. These conductors include a set of code leads 107, control leads 101, and signal leads 102. Each line circuit is also connected by the code leads 107 to the network controller. As subsequently described, the code leads 107 together with the control leads 101 enable the common control to scan, identify, and select any line circuit; the leads 102 permit common control to receive signals from the line circuits indicating their current conductive states as well as other useful information.

The embodiment also includes a plurality of circuits which are connected to the right hand or trunk side of switching network 112. These circuits include intercom trunk circuits 114, of which only one is shown, as well as register circuits 104, of which only

one is shown. Only a single trunk circuit and a single register are shown in order to minimize the complexity of the drawing. The trunk side network connections to the other register, the other intercom trunk circuits, as well as the other types of trunk circuits that would normally be provided in a PBX, are represented by the dashed conductors extending to the right from network 112 on Fig. 1C. The signals that are required to control the network in establishing a connection between a selected line side and a selected trunk side circuit are applied to controller 112A from the line side over path 107 and from the trunk side over path 103.

The system is of the common control type in which common control 113 governs the order in which the various circuits are interconnected via the network during the serving of each call. Common control receives call service requests from line circuits, from registers, and from the trunk circuits. Upon the receipt of each request, common control sets its mode control and sequence circuits 115 to a state unique to the request. Common control regulates the operation of the requesting circuit, as described in the Abbott patent, and controls the establishment of a network connection between the requesting circuit and any circuit of the system with which the requesting circuit must be connected. The serving of a call may require a plurality of network connections to be established sequentially.

Each line circuit includes a control logic element 108 which comprises a plurality of transistor gates which are selectively controlled to assume either an ON or an OFF conductive state. A gate is said to be ON whenever it receives an energizing potential at its input (its base), and said to be OFF when energizing potentials are not applied to all of its inputs. The conductive state of the line circuit gates is jointly controlled by the supervision circuit 105 within each line circuit, by the code leads 107, and by control leads 101. The code leads 107 extend from the line circuits to a line scanner 116 within common control; they further extend to registers 104. As is subsequently described, the code leads receive signals at certain times from scanner 116 and at other times from the register.

Signals indicating the conductive states of the line circuit gates are transmitted over signal leads 102 to common control. These signals enable common control to monitor the state of the line circuits and, by means of prewired logic, to determine whether a line circuit requires action by common control with regard to either a call initiated by or directed to the line circuit.

Included among the functions controlled by common control in connection with the

establishment of calls are the recognition of a service request from a calling line circuit when it initially goes off-hook, the identification of the calling line circuit so that it may be connected to a register, the selection of a called line circuit following the reception of a called number by the register, the selection of a trunk circuit for interconnecting the calling and called stations, and the reidentification of a calling line circuit at the time it is to be connected to the selected trunk circuit and, in turn, to the called line circuit.

Line scanner 116 has a plurality of output positions which are connected over separate ones of the code leads to the line circuits. The code leads are designated U0 through U9 and T0 through T9 and each line circuit is connected to a unique combination of code leads in such a manner that the numerical designation of a line circuit indicates the code leads to which it is connected. Thus, line circuit 00 is connected to code leads U0 and T0; line circuit 99 is connected to code leads U9 and T9.

Common control also includes a class of service translator 106 and a gate output signal translator 117. Translator 117 is connected to signal leads 102A and 102B; translator 106 is connected only to signal leads 102B. Translator 117 translates the signals received from the line circuit gates and informs common control regarding line circuits that require further call service. Translator 106 receives output signals from the line circuits and generates class of service information to indicate the type of call service to which the calling line is entitled.

Common control also includes a register bid circuit 118, a trunk bid circuit 119, and a trunk side scanner 120. The function of these circuits is to select an idle register or an idle trunk circuit when the services of either of these circuits is required on a call.

Detailed Description—

Fig. 1A, 1B, 1C, and 1D

The following describes the operation of the system of Fig. 1 in connection with the serving of a call initiated at station ST00 and directed to station ST99.

The off-hook condition at station ST00 is detected by supervision circuit 105 of line circuit LC00. This circuit, in turn, activates control logic 108 which transmits a signal over conductor LD00 and path 102A to translator 117 and mode control and sequence circuits 115 within common control. The receipt of this signal causes common control to go into what is termed the "line dial tone mode" and to apply an enable potential to control lead conductor DTE which extends to the control logic 108 of each line circuit. The receipt of this signal also causes common control to activate the line scanner 116 over path 116A. The scanner now begins a stepping or counting

operation in which it applies enable potentials to different combinations of the T- and U- code lead scanning conductors.

The scanner has stepping or counting positions individual to each line circuit. When the scanner steps to a position associated with a particular line circuit, it applies enable potentials to the U- and T- conductors to which the line circuit is connected. Thus, when line circuit LC99, for example, is scanned, enable potentials are applied to code lead conductors U9 and T9.

No line circuit other than LC00 is assumed to be in a newly initiated off-hook state. Therefore, the scanning of all line circuits other than LC00 produces no change of state in their logic circuit gates. However, when the scanner advances to its position 00, it applies enable potentials to conductors T0 and U0 to scan line circuit LC00. The simultaneous application of potentials to conductors DTE, U0, and T0, as well as the receipt of enable potentials from supervision circuit 105, activates the control logic 108 of line circuit LC00 and causes it to apply a change of state signal to its conductor LS00. This signal is applied over path 102B to the class of service translator 106, to the gate output signal translator 117, as well as to the mode control and sequence circuits 115. In response to the receipt of this signal, common control applies a signal over conductor path 116A to stop the line scanner in its position associated with line circuit LC00.

As described in the Abbott patent, common control now initiates the sequence of circuit actions required to select an idle register and to connect it to the calling line circuit. The trunk side scanner 120 has an operative position for each register and trunk circuit. It also has an output conductor that extends from each of its positions to the register or trunk circuit with which the position is associated. The output conductors of this scanner are designated R0 to RN and T0 to TN. The R- conductors extend to the registers; the T- conductors extend to the trunk circuits. Thus, conductor R0 extends from the scanner to intercom trunk circuit 0.

Common control with its mode control and sequence circuits 115, together with common control, initiates the selection of a register by applying potentials to conductors 120A and 118A. These conductors extend from the mode circuit to the trunk side scanner 120 and to the register bid circuit 118, respectively. The register bid circuit responds to the signal on conductor 118A and applies an enable potential to conductor MTR which extends to the selection and control element 104B within each register.

A register can be selected only when its selection and control circuit simultaneously

receives a potential on conductor MTR, a potential on its R- scan conductor, and a signal from its supervision circuit indicating that the register is idle. Thus, if register 0 is currently idle, its supervision circuit applies a signal to the selection and control circuit at the same time the register bid circuit applies a signal to conductor MTR. This leaves the conductive state of circuit 104B under control of the potential on scan conductor R0.

The signal on conductor 120A activates scanner 120. When register 0 is scanned, a signal is applied to conductor R0 which causes the selection and control circuit to change state and apply a stop scan signal to conductor RT. This signal extends back to the trunk side scanner 120 to stop it in its operative position associated with register 0. The signal on conductor RT also advises common control that an idle register has been selected and that the next sequence of operations required to serve the call may be initiated.

At this stage of the call, line scanner 116 is in its operative position associated with the calling line circuit and the trunk side scanner is in its operative position associated with register 0. Thus, the signals now applied to code leads 107 identify the calling line circuit; the signals applied to code leads 103 identify the selected register. Since code leads 107 extend to the line side of the network controller and since code leads 103 extend to the trunk side of the network controller, this circuit receives the signal information that identifies calling line circuit LC00 and register 0. Common control at this time applies an enable signal to conductor NETE* which extends to the network controller. This signal and the code lead signals cause the network to establish a path between line circuit LC00 and register 0.

Common control next activates gate CNGI. This applies the calling line information on code leads 107 to conductor CLN which extends to all registers. Element 104D in register 0 registers this information, under control of circuit 104B, for later use on the call. Common control then releases line scanner 116 and trunk side scanner 120 so that they may be used on other calls.

It is assumed that the present call is directed to station ST99. This being the case, the calling party dials the digits 99 which are received by the register and stored in its element 104C in the conventional manner. The register applies a signal to conductor FOR when all the digits required to serve the call have been dialed. This signal advises common control that the next sequence of circuit actions required for the call may now be initiated.

The receipt of the signal on conductor FOR causes the mode control to go into

what is termed the "read register mode" in which the dialed digits representing the called station information are read out of the register to identify and select the called station. Gate CLD1 is activated to gate the called number digits (99) onto code leads T9 and U9. Simultaneously, common control applies an enable potential to conductor LSE extending to all line circuits. The control logic element 108 of line circuit LC99 is activated at this time since both of its code leads U9 and T9 and conductor are enabled. The line circuit responds to these signals and applies an output signal to conductor LI which extends back to common control to advise it whether the line circuit is currently idle or busy. An output signal is also applied by the line circuit to its conductor LS99 which extends to class of service translator 106 to cause that circuit to generate class mark information.

Let it be assumed that station ST99 is idle. In this case, common control initiates the sequence of circuit actions required to select an idle intercom trunk circuit for use in interconnecting the calling and called line circuits. Let it be assumed that intercom trunk circuit 0 is idle and is selected for use on this call.

The selection of this circuit is controlled by its selection and control circuit 114B under joint control of signals received from its supervision circuit 114A, from conductor MIC, and from its scan conductor T0. At this time, common control applies a signal to path 119A to cause the trunk bid circuit 119 to enable conductor MIC extending to all trunk circuits. Common control also activates the trunk side scanner 120 so that it begins a scanning operation to select an idle trunk circuit. When trunk circuit 0 is scanned, the potential on conductor T0 activates the selection and control circuit 114B which, in turn, applies a signal over conductor OT1 extending back to common control to stop the scanner in its operative position associated with trunk circuit 0. The receipt of the signal on conductor OT1 also advises common control that an idle trunk circuit has been selected.

Gate CLD1 remains enabled and continues to apply the called number information to the code leads 107. The trunk side scanner is currently in its position unique to the selected trunk circuit. This being the case, the network controller receives code lead signals identifying both the called station and trunk circuit 0. Common control at this time applies an enable potential to conductor NETE to cause the controller to establish a network path between called line circuit LC99 and intercom trunk circuit 0. The network advises common control by a signal applied to conductor PC when the path is established.

After the called line circuit is connected to intercom trunk circuit 0, common control initiates the circuit actions required to re-identify the calling line circuit so that it may also be connected to trunk circuit 0. It has already been described how the calling line number information on code leads 107 was stored in the register following the scanning of line circuit LC00. Common control now activates gate CNG0 to gate the calling number from conductor CLN into line scanner 116 to force it to its operative position associated with calling line circuit LC00. Common control also applies an enable signal to conductor LSE extending to all line circuits. This activates the control logic element 18 for line circuit LC00 since conductors U0 and T0 are now enabled from the scanner under the control of signals applied to it by gate CNG0. Element 108 now applies an answer signal to conductor LS00 extending back to common control and the class of service translator 106. The class of service information generated by translator 106 indicates to common control whether the calling line circuit is entitled to initiate the type of call service being requested.

The signals on code leads 107 are also applied to the left side of the network controller. The trunk side scanner advances to its position T0-A which is also associated with the selected trunk circuit. The network now releases its connection between the calling line circuit and the register and re-establishes a new connection between the calling line circuit and the second network appearance of the selected trunk circuit. The calling and called stations are connected speechwise upon the establishment of this path.

Logic Circuits—Fig. 3A Through 3G

The illustrative embodiment of the invention makes extensive use of logic elements such as AND gates, OR gates, inverting AND and inverting OR gates, flip-flops, etc. The complexity of the drawing has been reduced by representing such elements with symbols indicating their logical functions, rather than by disclosing circuit details each time such an element appears on the drawing. Fig. 3 illustrates the details of the more commonly used logic elements in the system.

Fig. 3A shows the circuit which comprises the basic element of many of the logic circuits. This circuit comprises an AND NOT gate, commonly referred to as an AND or inverting AND gate. The circuit may also be operated as an inverting OR gate in the manner subsequently described. The circuit may be functionally divided into an AND gate and an inverting amplifier. The AND gate comprises diodes 301-1 through 301-N, together with resistor 302 and positive

potential source 308. The inverting amplifier comprises diode 304, resistors 305 and 307, and transistor 306. The operation of the AND gate is such that terminal 303 may go positive only when all of inputs 1 through N are raised above ground potential. The holding of one or more inputs at ground or negative potential prevents terminal 303 from going positive. The inverting transistor amplifier 306 is turned OFF except when it receives a base current from source 308 via resistor 302 and diode 304. Source 308 is effective to supply base current to the transistor only when terminal 303 goes positive as all of the inputs 1 through N are driven positive. The turn-ON of the transistor at this time lowers the potential on output conductor 310 from that of the positive source 309 to a lesser potential as determined by the IR drop across resistor 307.

It may be seen from the foregoing that the circuit of Fig. 3A operates in such a manner that positive signals on all inputs turn the transistor ON and produce a negative-going signal at its output. Conversely, the grounding of at least one input prevents the transistor from turning ON even though the remainder of the inputs are positive. This circuit may be operated as an AND NOT circuit by normally maintaining one or more of its inputs low, i.e., ground, and by subsequently driving all of its inputs HIGH for the AND condition of the circuit. When the circuit of Fig. 3A is operated as an inverting AND gate in our system, it is represented on the drawing by the symbol shown in Fig. 3B.

Noninverting AND gates are represented on the drawing by the symbol shown in Fig. 3C. This symbol differs from that of 3B in that the output conductor is directly connected to the semicircle representing the gate, rather than being connected to it by the small circle of Fig. 3B. The noninverting AND gate of Fig. 3C may be of any type well known in the art. For example, it could, if desired, be the inverting AND gate of Fig. 3B followed by an inverter.

The circuit of Fig. 3A may be operated as an inverting OR gate by normally maintaining all inputs above ground and by subsequently driving at least one input to either ground or to a negative potential to represent the OR condition. The symbol shown on Fig. 3D is used whenever the circuit of Fig. 3A is operated as an inverting OR gate. The symbol shown on Fig. 3E is utilized to represent the noninverting OR gates. These OR gates may be of any type well known in the art, such as for example, the inverting OR gate of Fig. 3D with an inverter in each of the input leads.

Flip-flops are constructed by cross-connecting two inverting AND gates as shown in Fig. 3F. These flip-flops are re-

presented by the symbol shown on Fig. 3G.

The circuit of Fig. 3F operates as follows: The bias circuit for the gate holds inputs S and R HIGH when the flip-flop is quiescent. Assume at this time that the transistor in gate G1 is OFF while that in gate G2 is ON. In this case, the output 1 is HIGH since its transistor is cut OFF; output 0 is low since its transistor is ON. Input signals applied to the S conductor at this time are ineffective to change the state of its transistor since the low on the cross-connected input from the output of gate G2 keeps the G1 gate turned OFF. However, a negative-going pulse applied to the R input at this time removes the base drive for the transistor in gate G2. This turns the gate OFF and drives its 0 output HIGH, which is cross-connected to the input of gate G1 to turn it ON and drive its output LOW.

Sequence Circuits—Fig. 4A Through 4D

The illustrative embodiment of the invention makes extensive use of sequence circuits. In particular, the common control portion of the system contains a number of sequence circuits whose function is to apply signals or control potentials to various portions and circuit elements of the system in a predetermined sequence. The complexity of the drawing has been reduced by representing the sequence circuits with symbols indicating their logical function, rather than by disclosing circuit details each time a sequence circuit appears on the drawing.

Two types of sequence circuits are used in the system. The type shown in Fig. 4A has a plurality of stages or elements of which two are shown and are designated 1 and 2. This type of sequence circuit, once it is activated, automatically steps from element to element without any response from the system. The circuit details of the sequence circuit of Fig. 4A are shown on Fig. 4B. The sequence circuit of Fig. 4C is similar to that of Fig. 4A, except that it does not step from element 3 to element 4 until it receives a system response on conductor RBC. Fig. 4D illustrates the circuit details of the circuit of Fig. 4C.

The following describes the operation of the sequence circuits of Fig. 4B. Stage 1 is enabled when both inputs of gate A go HIGH. The upper input of gate A is driven HIGH by a potential applied to conductor 401 from the preceding stage. A LOW on conductor 402 from the preceding stage is propagated, after a predetermined delay, through delay element D, applied to the input of inverting AND gate Z, and applied as a HIGH to the lower input of gate A.

Gate A turns ON and drives its output LOW when both of its inputs go HIGH. The LOW on its output turns OFF gate C and drives conductor ABC HIGH. The

HIGH from gate C turns ON gate B and drives conductor ABC* LOW. The potentials on conductors ABC and ABC* are applied to other elements of the system to control those elements in the performance of their assigned system functions. The potentials on these two conductors also extend to stage 2 of the sequence circuit to activate it in a manner analogous to that already described for stage 1. Specifically, the upper input of gate F is HIGH at this time from conductor ABC. The lower input of gate F is driven HIGH, after a predetermined delay, in response to the LOW on conductor ABC*. The purpose for the delay is so that the outputs from the first and second stages of the sequence circuit will have a predetermined sequence in time. When gate F turns ON after the predetermined delay, gate G turns OFF and drives conductor BBC HIGH and drives conductor BBC* LOW from gate H. This delay insures that conductors ABC and ABC* assume their active state and then, after a predetermined time, conductors BBC and BBC* will assume their active state as gates G and H respond to the turn-ON of gate F when both of its inputs go HIGH.

Conductors BBC and BBC* extend both to the next stage of the sequence circuit as well as to other elements of the system to control them in the performance of their system functions. The next stage of the sequence circuit is activated by the potentials on conductors BBC and BBC* in a manner analogous to that already described for elements 1 and 2.

The sequence circuits of Fig. 4A and 4B, as well as those of 4C and 4D, operate in such a manner that the output conductors of an activated stage remain enabled with a HIGH or a LOW potential, as the case may be, when the sequence circuit steps to the next position to activate it. In other words, after the output conductors of a stage are enabled, they remain enabled when the sequence circuit steps through the remainder of its positions. The output conductors of each stage are disabled or reset to their normal state only when the enable potentials are removed from the control gate of the first stage; namely, the gate that corresponds to gate A of stage 1. The turn-OFF of that gate disables the outputs of all other stages of the sequence circuit.

The following describes the operation of the sequence circuit of Fig. 4C and 4D. Stage 3 operates in the same manner as described for stages 1 and 2 of Fig. 4B. Namely, both inputs of gate A1 to HIGH; its output goes LOW; the output of gate C1 goes HIGH to conductor CBC; and the output of gate B1 goes LOW to conductor CBC*.

The output of gates B1 and C1 are connected to element 405 which is entitled

"System Logic Circuits". The output of gate C1 also extends to the upper input of gate F1. Element 405 receives the control potentials on conductor CBC*, performs its assigned system function, and then transmits a signal over conductor RBC to the lower input of gate F1. The receipt of this signal indicates that the system function assigned to element 405 has been completed and that the sequence circuit may now step from position 3 to position 4. The simultaneous application of signals to the lower and upper inputs of gate F1 turns the gate ON, turns gate G1 OFF, and gate H1 ON. This drives conductors DBC HIGH and DBC* LOW in a manner similar to that already described.

The connections from stage 4 to the next stage depend upon whether the next stage must wait for a system response before it assumes its active state. If it is desired that the stepping action be automatic after a predetermined time delay, the next stage will be of the type shown for stages 1, 2, and 3, and conductors DBC and DBC* will supply its controlling potentials. On the other hand, if the next stage must wait for a system response before it becomes active, it will be of the type shown for stage 4. In this case, only one of its control potentials will be supplied by conductor DBC. Its other input will come from a system logic circuit over a conductor analogous to conductor RBC for element 4.

Each position of the sequence circuit of 4D that becomes active holds its output conductors enabled as the succeeding stages become active. All output conductors, once they are enabled, remain enabled until the entire sequence circuit is reset when an enable potential is removed from one of the inputs of the AND gate corresponding to AND gate A1 for element 3 provided that any external input signal to the position and all prior positions remains applied. The removal of an external signal turns OFF the controlling AND gate for the stage to which it is connected as well as to all subsequent stages.

Mode Control—Fig. 5A and 5B

The mode control circuit, which is shown as element 223 on Fig. 2E, is shown in further detail on Fig. 5A and 5B. Fig. 2E and 5A show the mode control as having five sections designated A through E. Input conductors enter the left side of each section; output conductors extend from the right side, sections B, C, D, and E. The mode control of Fig. 5B is also subdivided into operational elements A through E; it further has input and output conductors that correspond to those of Fig. 5A.

The mode control circuit of Fig. 5B uses JK flip-flops in a ring counter configuration. The clock 501 is connected via gate A4 to

the T input of each flip-flop. At certain times, as subsequently described, the clock output pulses are effective to advance the operational state of the counter from stage-to-stage one step at a time.

Each JK flip-flop has inputs designated S, J, T, K and R; each JK flip-flop also has outputs designated 1 and 0. A HIGH on the R input resets a flip-flop. This causes its 0 output to be HIGH and its 1 output to be LOW. Conversely, a HIGH on the S input sets a flip-flop so that its 1 output is HIGH and its 0 output is LOW. The J input is functionally associated with the S input and the K input is associated with the R input. The J and K inputs differ from the S and R inputs in that a high input signal to either the J or K input is not effective to alter the state of the flip-flop unless the signal is received coincidentally with a clock pulse on the T input.

The J and K inputs of each flip-flop are connected to the 1 and 0 outputs, respectively, of the previous stage. Depending upon the conductive state of each flip-flop, one of its outputs is HIGH while the other is LOW. When a clock pulse is received on the T input of a flip-flop, it is set to the state of the previous stage under control of the signals applied to its J and K inputs. If the J input is HIGH, the flip-flop is set; if the K input is HIGH, the flip-flop is reset. JK flip-flops are well known in the art and, therefore, no further description of their operation is necessary.

The initial or rest condition of the mode control circuit of Fig. 5B occurs when a reset pulse is applied to the RESET conductor and, in turn, to the S input of flip-flop A1. The RESET conductor also extends to the input of gate 503 as well as to the R input of flip-flops B1, C1, D1, and E1. The reset signal is a HIGH and its application to the RESET conductor sets flip-flop A1 and resets any of flip-flops B1, C1, D1, or E1 that may have previously been in a set state. By means of gate 503, the reset signal also resets flip-flop 502. Subsequently, after the reset signal terminates, the clock pulses pass through gate A4 and advance the JK flip-flop counter chain step-by-step in response to the reception of each clock pulse. Thus, following the setting of flip-flop A1, the next clock pulse sets flip-flop B1 and resets flip-flop A1. The counter chain advances in this manner one step for each clock pulse received until a mode control request signal is received.

When a request is received for a particular mode such as, for example, mode B, the request signal on conductor RDRQ enables or primes the upper input of gate B2. Subsequently, when the counter advances to its position in which the B1 flip-flop is set, the 1 output of the flip-flop enables the lower input of gate B2. This turns the gate on and

makes its output HIGH. This HIGH extends to an input of gate A2 which makes its output HIGH. This HIGH is inverted by gate A3 to a LOW. This LOW is extended to the set input of flip-flop 502 to switch it to a set state. The LOW on the 0 output of flip-flop 502 inhibits the upper input of gate A4 so that the clock pulses no longer pass through the gate to the JK flip-flops.

Flip-flop B1 remains set and its 1 output applies a HIGH to the RDR output conductor of element B. The mode control circuit remains in this state until a HIGH is subsequently received on the RESET conductor from one of the sequence circuits shown on Fig. 2. At this time, the reset signal sets the A1 flip-flop, resets flip-flop B1, and resets flip-flop 502. When the reset pulse terminates, the clock pulses are again applied to the JK flip-flop as described so that the circuit advances one step for each pulse until a subsequent service request signal is received.

Because of the order in which the ring counter steps through its sequence, the stages have a preference. In the case of simultaneous mode requests, the highest preference mode is selected. After the mode control is again reset, the highest preference remaining mode request is served so that eventually all waiting mode requests are served.

Detailed Description—Fig. 2A Through 2F

Fig. 2A through 2F, when arranged as shown on Fig. 2G, illustrate additional details of the system shown in Fig. 1A to 1D. The system of Fig. 2 is similar in most respects to that of Fig. 1. Each element of Fig. 2 corresponding directly to an element on Fig. 1 is designated in a manner that facilitates an appreciation of the correspondence. Thus, network 122 on Fig. 1C corresponds to network 212 on Fig. 2D; code leads 107 on Fig. 1 correspond to code leads 207 on Fig. 2. The highest numbered element on Fig. 1 is trunk scanner 120. Therefore, elements designated 220 or lower on Fig. 2 directly correspond to elements on Fig. 1; elements designated 221 and higher on Fig. 2 do not correspond directly to an element on Fig. 1 due to the inclusion of greater detail on Fig. 2.

The system of Fig. 1 contains 100 lines. The system of Fig. 2 is somewhat more complex in that it shows a system having a plurality of groups of lines with each group containing 100 lines. The stations or lines of the first group are designated 100 to 199 and are shown in detail. Line circuit LC100 for line 100 is shown in detail; it is connected to station ST100 on its left side, and is connected on its right side to an appearance on network 212. In an analogous manner, every other line of the system in-

cludes a line circuit LC- that is connected on its left side to a station subset and connected on its right side to the switching network.

5 In the system of Fig. 1, the code leads 107 extend directly from the line scanner 116 to each line circuit. In the system of Fig. 2, each group of 100 lines has its own set of code leads which extend from the output of a line selector 221 to each line circuit of the group. Each group has its own line selector connected in the manner shown in detail for lines 100 through 199. Line scanner 216 of Fig. 2C corresponds to line scanner 116. However, line scanner 216 communicates only indirectly, rather than directly, with the line circuits via the code leads. It directly controls the operation of the line selector of each line group. Each line selector responds to the signals from the scanner and applies scanning signals from its output to the U- and T- code conductors of its line group and, in turn, to the line circuits of its group.

25 In a manner similar to that shown for Fig. 1, common control 213 on Fig. 2 communicates with the line circuits by means of control leads 201 and signal leads 202 which correspond to leads 101 and 102 on Fig. 1. The connections between common control and the leads 201 and 202 are shown in greater detail on Fig. 2 than they are on Fig. 1.

35 The system of Fig. 2 contains a plurality of registers of which only register 204 is shown in detail. It further contains a plurality of trunk circuits. These include an intercom trunk circuit 214-0 and a plurality of central office trunk circuits 214-1 through 214-9. It also includes a busy tone circuit 222. The remainder of the trunk and register circuits that comprise the system are shown only diagrammatically by the tip, ring, and sleeve (T.R.S.) connections extending from the right side of the switching network 212.

45 The common control 213 is shown in considerably greater detail on Fig. 2 than it is on Fig. 1. Some of this additional detail includes the gates and logic circuits by means of which elements of common control exchange information with other common control elements as well as with the rest of the system. The remainder of this additional detail comprises a plurality of sequence circuits which are used to provide the control potentials required by the system. The gates and the sequence circuits used in the common control are shown only diagrammatically on Fig. 2. However, these elements are shown in greater detail on Fig. 3, 4 and 5.

Description of a Call From Station ST100 to Station ST101

65 The following paragraphs describe the

operation of the system of Fig. 2 with reference to an assumed call initiated at station 100 (ST100) and directed to station 101. The CO cutoff relay of line circuit 100 (LC100) is released during the idle state of the circuit. At such times, the L relay is bridged directly across the tip and ring conductors between battery and ground via the break contacts of the CO relay. Subsequently, when station 100 goes off-hook, the L relay operates and closes its make contacts L-1 which apply a ground or LOW to conductor LDTCQ*. This conductor extends to the input of the LDT gate on Fig. 2B. This gate inverts the LOW and applies a HIGH to conductor LDTCQ which extends from Fig. 2B to element D of the mode control circuit 223. The receipt of this signal steps the circuit to its position D which, in turn, applies an output signal over conductor 223D to the input of element A of the LDT sequence circuit 224. This signal steps circuit 224 to its position A which applies a LOW to its output conductor LSG*. The LSG* signal extends from Fig. 2E to Fig. 2C where it is inverted by gate LSG and applied as a HIGH to the left input of each of the AND gates LU1 to LT8 and LH1 to LH8. This HIGH partially primes these gates so that they may subsequently gate the binary output signals from the scanner to line selector 221 and line group selector 225.

Subsequently, after a predetermined time delay, sequence circuit 224 steps from position A to its position B and applies a LOW to conductor DTE*. This LOW extends from Fig. 2E to Fig. 2B where it is applied to the input of gate DT. This gate inverts the LOW and applies a HIGH to conductor DTE which extends to input 2 of the DTE AND gate of each line circuit. Input 1 of this gate in line circuit 100 is currently at a HIGH potential from resistor R3 since the break contacts L-2 of its operated L relay are currently open. Inputs 3 and 4 of the gate are currently LOW. They are driven HIGH when the line circuit is scanned as subsequently described in detail. For the time being, the LOW on inputs 3 and 4 hold the gate in its OFF state in which its output is HIGH.

Sequence circuit 224 next steps from its position B to its position C and applies a LOW to conductor LSS*. The LOW on this conductor extends from Fig. 2E back to Fig. 2C where it is applied to the input of line scanner to cause it to begin a line scanning operation.

The scanner is essentially a binary counter having a units, tens, and hundreds stage. The output conductor of each counter position is normally LOW but is driven HIGH when the scanner steps to a position associated with a particular conductor. The scanner is arranged to count in binary from 100

through 899 with each of its positions being unique to the correspondingly designated line circuit. The signals from its units and tens positions extend over conductors SU- and ST- to gates LU- and LT- and from there to the input of the line selector for each group of 100 lines. The line selector for each group converts the scanner binary output information to decimal and applies it to the code leads of its group. The binary output signals from the hundredths stage of the counter extend through the LH- gates to the line group selector 225 which energizes one of its output conductors LG1 through LG8, depending upon the current operative position of the counter. Output conductor LG1 of the line group selector extends to line selector 221 for the first group of 100 lines. The remaining output conductors of line group selector 225 each extend to the line selector for a different one of the remaining groups of 100 lines. Although all line selectors receive the units and tens-binary information generated by the scanner, a line selector can respond to these signals only if it also receives an output signal from the line group selector. Thus, line selector 221 for lines 100 through 199 is energized or primed by a single output conductor LG1 from the line group selector. At that time, only this line selector may respond to the tens and units signals generated by the line scanner.

When the line scanner steps to its hundredths position in which it energizes its output conductor SH1, this signal passes through AND gate LH1 since the left-hand input of all scanner output AND gates are currently HIGH from the output of gate LSG. The signal on conductor LH1 causes the line group selector to apply a signal to conductor LG1 to activate line selector 221. During the time the signal on conductor LG1 persists, the tens and units signals generated by the scanner are transmitted through the LT- and LU- AND gates to the line selector 221. This circuit responds to these signals and applies scanning potentials to code leads 207.

Each code lead is normally LOW but is driven HIGH when the scanner assumes a position associated with the code lead. Thus, when line circuit 100 is scanned, its code leads U0 and T0 are HIGH and the other code leads are LOW. This causes a HIGH to be applied to inputs 3 and 4 of AND gate DTE of line circuit 100. The other two inputs of the gate are HIGH for reasons already mentioned and, therefore, the gate turns ON at this time and drives its output LOW. This LOW extends to the input of gate LSA to turn it OFF and drive its output HIGH. This, in turn, turns gate LSM ON and drives its output conductor LS100 LOW. This LOW is extended through diode D00 to

terminal CS1 of the class of service detector 226. This circuit receives the class of service mark from the line circuit LS- leads, generates appropriate class of service information, and applies a LOW to its output conductor LS* and to one of its output conductors CS*, such as CS1*. The signal on conductor LS* extends from Fig. 2B to Fig. 2E where it is inverted by gate LS1 and steps the sequence circuit 224 to its position D. The HIGH on conductor LS also extends to the right side of the line scanner 216. The receipt of this signal causes the scanner to terminate its scanning operation and to stop in its operative position associated with line 100.

The next step in serving the call is for the system to select and connect an idle register via the switching network to the calling line circuit. The stepping of sequence circuit 224 to its position D applies a signal to conductor IRS which extends on Fig. 2F to the input of the scanner control circuit 220B and to the input of the register bid circuit 218. The receipt of the IRS signal by these circuits initiates the system operations required to select an idle register.

Let it be assumed that register 204 on Fig. 2D is idle and is selected for use on the call. The selection of the register is controlled by its gate MTR. This gate has three input conductors and the register is selected only when its gate is switched from a normally OFF to an ON state. The supervision circuit 204A of the register applies an enable potential to the upper input of its gate whenever the register is idle. The MTR conductor extends from the output of the register bid circuit 218 to the lower input of the MTR gate. The middle input of the gate of register 204 is connected to output conductor R0 of scanner 220.

The signal on conductor IRS causes the register bid circuit 218 to apply an enable conductor to output conductor MTR which extends to all register circuits. With reference to the call now being described, this signal enables the lower input of gate MTR of register 204. The receipt of the IRS signal by scanner control 220B activates scanner 220 and causes it to step through its counting positions in which it applies a scanning potential to each one of its output conductors in sequence. When it steps to its position associated with conductor R0, it applies a scan signal to that conductor and, in turn, to the middle input of gate MTR of the register. The other two inputs of the gate are already enabled and, therefore, the enabling of its middle input turns the gate ON and drives its output LOW. This LOW extends over conductor RT in Fig. 2F and, from there, to the right input of gate SSICA. This signal is propagated through the gate and applied as a stop scan signal to scanner

220. This stops the scanner in its operative position associated with conductor R0 and register 204.

5 The output signal from gate SSICA is also extended over conductor SSICA from Fig. 2F to the input of section E of sequence circuit 224. This steps the sequence circuit to its position E and applies a LOW to its output conductor NETE*.

10 Line scanner 216 is still in its operative position 100. Therefore, the signals it is currently applying to its output conductors constitutes an identification of calling line 100. Similarly, the signals scanner 220 is currently applying to its output conductors constitutes an identification of the selected register, i.e., register 204. The identification information from the line scanner is applied over cables 227A and 227B to the line side input of the network controller 212A; the register identification from scanner 220 is applied over cable 228 to the trunk side input of the network controller. This identification information from the two scanners, together with the signal on conductor NETE*, causes the network to establish a path between line circuit 100 and register 204.

20 The sequence circuit 224 advances from its position E to its position F subsequent to the application of the LOW to conductor NETE*. This causes the sequence circuit to apply an enable signal to conductor CNGI which extends to one input of each of the CNGI gates on Fig. 2C. The other input of each of these gates is connected to an individual one of the output conductors of line scanner 216. The potential on conductor CNGI enables the gates associated with position 100 of the scanner and thereby gates the calling number 100 onto cable CNI. This cable extends from Fig. 2C to Fig. 2D where it applies the number 100 into the calling number store 204B of register 204. Element 204B stores the calling number for subsequent use on the call. The output of the MTR gate in register 204 permits only the calling number store of register 204 to receive the information currently gated onto cable CNI.

50 The network applies a path complete signal to conductor PC when it completes the establishment of a network connection between calling line circuit 100 and register 204. The signal on conductor PC advances the sequence circuit 224 to its position G in which it applies an output signal to the RESET conductor extending to element A of mode control circuit 223. This steps the mode control from position D to position A. 60 The removal of the output signal from mode control element D disables sequence circuit 224 and, in so doing, removes the currently applied signals from all of its output conductors. This effectively releases common

control from the present call and permits it to serve other calls. 65

The calling party at station 100 now dials digits of the called station. Since it has been assumed that the call is to be extended to station 101, the calling party now dials the digits 101. The dialed digits are transmitted through the network to the register and stored in its called number store 204C in the conventional manner. The register applies a readout request signal to conductor FOR after it determines that the digits representing a complete number have been dialed. The signal on conductor FOR is extended through the RDRQ gate on Fig. 2E and applied to element B of mode control 223. This steps the mode control to its position B and, in so doing, applies a signal to the input of element A of the read register sequence circuit 229. The next function to be performed by the system in connection with the serving of the presently described call is for the called line to be identified, selected, and then tested to determine whether it is currently idle or busy. The activation of element A of sequence circuit 229 initiates these system functions. 80 85 90

The activation of element A applies a signal to the register selector 230 which has an operative position and an output conductor unique to each different register in the system. The output conductor unique to register 204 is designated RDA1 and it extends from the output of the register selector to register 204. 95

The register selector 230 responds to the input signal from sequence circuit 229, steps in known manner to its operative position associated with register 204, and applies an enable potential to conductor RDA1. This signal causes the called number store 204C of register 204 to gate the called number digits 101 onto cable RN which extends from Fig. 2D to the register number store 231. The signals received by this element from cable RN are registered for subsequent use in identifying and selecting the called line. 100 105 110

The read register sequence circuit 229 next steps from its position A to its position B and applies a signal over its output conductor to the upper input of AND gate RNSG. Conductor LSG* is currently HIGH because sequence circuit 224 is not active at this time. Therefore, the signal applied to the upper input of gate RNSG is propagated through the gate and applied to conductor RNSG which extends to the RT-, RU-, and RH- AND gates on Fig. 2C. These gates are connected to the output conductors of the register number store. The signal on conductor RNSG partially enables each of these AND gates and, in so doing, gates the called number digits 101 from store 231 to the input of the line group selector 225 and the line selector 221. Group selector 225 enables its 115 120 125

output conductor LG1 which extends to the input of line selector 221. The T- and U- input conductors of selector 221 receive signals representing the digits 01. This causes the line selector to apply a HIGH to code lead conductors T0 and U1. The signals on these conductors have no immediate effect on the DTE gate of line circuit 101 since conductor DTE is not currently enabled. The code lead signals have no effect on gate LSE of line circuit 101 since its lower input is not currently enabled.

The output gates RH1 through RH8 also apply information identifying the hundreds digit of the called number to binary to decimal translator 270 when conductor RNSG is enabled. Element 270 translates the information to decimal form and applies it over the H- conductors of cable 271 extending from Fig. 2C to the cross-connection field comprising terminals 272 and 273 on Fig. 2E. The hundreds information of the called digit at this time activates the terminal connected to the H- conductor that corresponds to the hundreds digit. Thus, since the hundreds digit of called line 101 is 1, translator 270 activates its H1 output conductor and, in turn, terminal 272-1 on Fig. 2E. The terminals 272 are cross-connected by means of the indicated straps to terminals 273. The potential on conductor H1 and terminal 272-1 is extended to terminal 273-1 and from there to the lower input of AND gate SIC. The upper input of this gate is HIGH and, therefore, a LOW is now generated at the output of the gate. This LOW switches the flip-flop IC to a set state in which its 1 output is HIGH. The upper input of gate SIC is HIGH since both inputs of gate RNSG are HIGH. The HIGH on the 1 output of flip-flop IC primes the lower input of gate ICA so that it can subsequently respond to a HIGH on its upper input from the output of gate LSE5.

The preceding has described how flip-flop IC is set in response to the dialing of a hundreds digit of 1. The circuit actions resulting from the dialing of a prefix digit 9 are described subsequently in the specification.

The read register sequence circuit 229 subsequently steps to its position C and, in so doing, applies a LOW to its output conductor LSE*. The LOW on this conductor is extended to the input of gate LSE5 which inverts it and applies a HIGH to the upper input of gate ICA. Gate ICA now turns ON and applies a HIGH to the lower input of gate LSE4. Flip-flop 236 is currently in a reset state in which its 0 output is HIGH to the upper input of gate LSE4. This gate now turns ON and applies a LOW to its output conductor which extends over conductor 239 to the upper input of gate LS and gate LSE2. This LOW turns gate LSE2 OFF and applies

a HIGH to conductor LSE1 which extends to the input of gate LS1 on Fig. 2B. This gate inverts the HIGH and applies a LOW to conductor LSE which extends to the input of the HTLSE gate of each line circuit. This LOW turns each HTLSE gate OFF and drives its output HIGH which extends to the lower input of the LSE gate of each line circuit. Only code leads T0 and U1 are energized at this time by line selector 221. These two potentials extend to line circuit 101 where they, together with the LOW on conductor LSE, cause gate LSE to turn ON and drive its output LOW. The LSE gate of no other line circuit turns ON at this time since no other line circuit currently has both of its code leads energized by line selector 221. The LOW on the output of gate LSE in line circuit 101 turns OFF its gate LSA to drive its output HIGH. The HIGH on the output of this gate turns ON gate LSM to drive conductor LS101 LOW. This HIGH is also extended to the upper input of gate LI. The circuit operations resulting from the LOW on conductor LS101 are described subsequently.

The circuit actions resulting from the application of the HIGH to the upper input of gate LI depends upon whether line 101 is currently busy or idle. If the line is busy, its cutoff relay CO is operated and the make contacts of this relay apply a ground to the lower input of gate LI to prevent the gate from turning ON. This holds conductor LI HIGH. On the other hand, if the line is idle, the CO relay is released and the lower input of the gate is HIGH. This permits the LI gate to turn ON and drive conductor LI LOW when gate LSA turns OFF and drives the upper input of the LI gate HIGH. In summary, the gating of the called number 101 onto the code leads, and the resultant turn-ON of gate LSE in called line circuit 101, causes a LOW to be applied to conductor LI if the called line is idle and a HIGH to remain on the conductor if the called line is busy.

The Called Line is Idle

Let it initially be assumed that the called line is idle. Consequently, both of its gates LI and LSM turn ON and apply a LOW to conductors LS101 and LI. The LOW on conductor LS101 is applied to the class of service detector 226 where it causes that circuit to apply a LOW to its output conductor LS*. The LOW on conductor LI is inverted by gate L and applied as a HIGH to conductor LIA. The LOW on conductor LS* is inverted by gate LS1 and applied as a HIGH to conductor LS. The HIGH on conductors LIA and LS are applied to the lower two inputs of gate LI on Fig. 2E. The upper input of the gate is HIGH at this time by virtue of the LOW on conductor 239 from

gate LSE4. This LOW is inverted by gate LS and applied as a HIGH to the upper input of the LI gate. The LI gate, therefore, turns ON at this time and activates element A of the line idle subsequence circuit 232. This causes a HIGH to be applied to conductor SLIC which extends both to the scanner control 220B and to the trunk bid circuit 219. The receipt of this signal by the trunk bid circuit activates its output conductor MIC which extends to input 3 of the MIC gate of each intercom trunk circuit. This partially enables the gate and subsequently permits the first intercom trunk circuit that is scanned to be seized for use on this call.

The receipt of the signal on conductor SLIC by scanner control 220B activates scanner 220 and causes it to apply scanning signals to its output conductors. Let it be assumed that intercom trunk circuit 214-0 is idle and available for use on this call. Input 1 of its gate MIC is enabled at this time by its supervision circuit 274. Input 2 of the gate is enabled when the scanner applies an enable potential to code lead conductor T0. This turns ON the MIC gate and drives its OT1 output conductor LOW which extends back to the scanner control circuit 220B on Fig. 2F. This signal is propagated through the SSICA gate and applied as a stop scan signal to scanner 220. This stops the scanner in its operative position associated with it output conductor T0 and intercom trunk circuit 214-0.

At this stage of the call, the called number 101 is currently being gated from the register number store 231 to the line selector 221 and, in turn, to the code leads 207; the output of scanner 220 is currently applied to conductor T0 extending to trunk circuit 214-0. These two items of information respectively identify the called line circuit 101 and intercom trunk circuit 214-0. The called number 101 is supplied at this time over cables 227A and 227B to the line side of the network controller; the intercom trunk circuit identification is supplied to the trunk side of the network controller by conductor T0.

The line idle subsequence circuit 232 now steps to its position B and applies a LOW to conductor NETE*. This LOW extends to the network controller where it causes the network to establish a connection between line circuit 101 and the upper network appearance of intercom trunk circuit 214-0. The controller applies an enable signal to conductor PC when this path is established. This signal steps sequence circuit 232 to its position C in which it applies a potential to its output conductor 232C. This potential is extended through gate 237 to set flip-flop 236. This potential is further extended to the input of scanner control 220B.

The receipt of this potential by scanner control causes the scanner 220 to advance

one step, namely, from its position T0 to its position T0-A. This transfers the scanner output potential from conductor T0 to conductor T0-A which extends to network controller 212A. As is described in subsequent paragraphs, the purpose of transferring the scanner output conductor to potential T0-A is to apply the necessary control information to the network so that when the calling line is subsequently selected, the network will establish a path between the calling line and the second (the lower) appearance of the intercom trunk circuit 214-0. The called line has already been connected to the upper network appearance by virtue of the scanner output potential applied to conductor T0. The calling line is connected to the lower appearance by the signal on conductor T0-A. The signal on conductor 232C is inverted by gate 277 and applied as a LOW to switch flip-flop 276 to a set state. The resultant HIGH on the 1 output of this flip-flop is extended through gate 275 to the lower input of gate LSIC. This signal holds the lower input of gate LSIC HIGH when the SSICA signal terminates as the scanner is advanced from its position T0 to its position T0-A.

With flip-flop 236 in a set state, its 1 output applies an enable potential to the input of position A of the calling line select subsequence circuit 233 to activate it. The 0 output of the flip-flop applies a LOW to turn OFF gate LSE4 and drive its output HIGH. The output of the LSE4 gate going HIGH propagates through gates LS and LI making the output of the LI gate LOW disabling sequence circuit 232 and returning its outputs to their idle state. The activation of position A of sequence circuit 233 applies a potential to its conductor CNG0 which extends from Fig. 2F to the right-hand input of each of the CNG0 AND gates of Fig. 2C. This conductor also extends to the supervision circuit 204A of all registers, such as register 204. The receipt of the CNG0 signal by register 204 causes its supervision circuit 204A to release the circuitry that is currently holding up the network connection from the register 204. The receipt of the CNG0 signal on conductor RDA1 controls supervision circuit 204A so that only register 204 responds to the CNG0 signal and releases its network holding circuitry.

The outputs of gates CNG0 extend to the lower input of line scanner 216. The register selector 230 is currently applying an enable potential to conductor RDA1 which extends to register 204. This potential causes the register to gate the calling number information over its output conductors of cable CNO to the left-hand input of the CNG0 gates on Fig. 2C. The enable potential now on conductor CNG0 gates the calling number information from cable CNO into the line scanner and forces

it to its operative position associated with calling line 100. The calling number is applied by the scanner to its output conductors which extend to gates LH-, LT-, and LU-.

Next, sequence circuit 233 steps from its position A to position B and applies a LOW to conductor LSG*. This LOW is applied to the lower input of AND gate RNSG on Fig. 2E to disable it. This removes the output signal from conductor RNSG which extends to the RH-, RT-, and RU- output gates of the register number store 231 on Fig. 2C. This disables these gates and removes the called number information from the input of line selector 221. The LOW on the LSG* lead is inverted by the LSG gate on Fig. 2C and applies as a HIGH to the output gates of the line scanner 216 to enable them. This permits the line scanner to pass the calling number information to the line selector 221 and line group selector 225. Selector 221, in turn, applies potentials to the code leads T0 and U0 to identify line circuit 100.

Next, sequence circuit 233 steps to its position C, and applies a LOW to conductor LSEA* and, in turn, to the lower input of gate LSE2. The upper input of gate LSE2 is currently HIGH from the output of gate LSE4 since flip-flop 236 is in a set state. Gate LSE2 inverts the LOW on conductor LSEA* and applies a HIGH to conductor LSE1 which extends to the input of gate LS1 on Fig. 2B. Gate LS1 inverts the HIGH and applies a LOW to conductor LSE which extends to an input of the HTLSE gate of each line circuit. Each HTLSE gate inverts the LOW and applies a HIGH to the lower input of the LSE gate of its line circuit. Only the LSE gate of calling line circuit 100 can respond since only its code lead conductors U0 and T0 are enabled at this time. The turn-ON of this gate in line circuit 100 turns OFF gate LSA, and turns ON gates LSM and LI. Gate LI turns ON since relay C0 released when the register released the network connection to line circuit 100. The turn-ON of gate LSM applies a LOW to its output conductor LS100. The LOW on conductor LS100 is extended to the class of service detector 226 which applies a LOW to its LS* output conductor. The LOW on the LS* conductor is inverted by gate LS1 making its output conductor LS HIGH.

The HIGH on conductor LS extends to the upper input of gate LSIC on Fig. 2F. The lower input of the gate is currently HIGH from gate 275. Gate LSIC now turns ON and applies a HIGH to conductor LSIC which extends to position D of the calling line select subsequence circuit to cause that circuit to advance to its position D. This, in turn, applies a LOW to conductor NETE* which extends to the input of the network controller 212A. The signals applied from cables 227A and 227B to the line side of

the network controller at this time identify the calling line circuit; the signals applied to the trunk side, namely, the signal on conductor T0-A, identify the selected trunk circuit. The signal on conductor NETE* causes the network to establish a connection between calling line circuit 100 and the second appearance of the intercom trunk circuit 214.

The network controller returns a signal on conductor PC when this path is established. This signal advances sequence circuit 233 to its position E and causes it to apply a signal to the RESET conductor which extends from Fig. 2F to position A of the mode control 223. This resets the mode control 223 to its position A and removes the output signal from its position B. The removal of this signal, in turn, disables sequence circuits 229 and 233. This restores common control to its normal state in which it is free to serve other calls.

The completion of the network connection between calling line circuit 100 and intercom trunk circuit 214-0 completes the establishment of a call connection between calling line 100 and called line 101 via intercom trunk circuit 214-0.

Called Station Is Busy

It was assumed in connection with the call connection described in the preceding paragraphs that the station 101 was idle and, therefore, free to receive the call initiated by station 100. Let it now be assumed that station 101 is busy. This condition is detected when the called number 101 is gated out of the register number store 231, through the line selector 221 and line group selector 225, and applied to code leads T0 and U1. The turn-ON of gate LSE of line circuit 101 at this time turns OFF gate LSA, turns ON gate LSM, and applies a HIGH to the upper input of gate LI. Since the called line is assumed to be busy, its CO cutoff relay is operated and applies a ground to the lower input of its LI gate. This ground prevents the gate from turning ON. Therefore, conductor LI remains HIGH.

The turn-ON of gate LSM of line circuit 101 applies a LOW to conductor LS101 extending to the class of service detector 226. This causes a LOW to appear on output conductor LS* of this circuit. This LOW is extended to Fig. 2E, inverted by gate LS1 as a HIGH on conductor LS, where it is applied to the lower input of the LI gate and to the middle input of the LB gate. The HIGH on conductor LI is inverted by gate L (Fig. 2B) and applied via conductor LIA as a LOW to the middle input of gate LI. This inhibits the gate, holds its output LOW, and holds the output of inverting gate LBI HIGH. This HIGH is connected to the upper input of the LB gate. The lower input

of the LB gate is HIGH at this time by virtue of the ground on conductor LSE* from position C of the read register sequence circuit 229. This ground is propagated through gates LSE5, ICA, LSE4, and LS and appears as a HIGH on the lower input of gate LB.

Al three inputs of gate LB are now HIGH. This drives its output HIGH which extends via gate SLBT to conductor SLBT which, in turn, extends to the lower input of gate 237, to the input of the scanner control 220B, as well as to the input of the trunk bid circuit 219. The trunk bid circuit activates its output conductor NBT which extends to the busy tone circuit 222 to prime its selection gate BTR so that it may be enabled on a subsequent scanning operation. The SLBT signal to scanner control causes that circuit to activate scanner 220. This circuit now begins a scanning operation to select a busy tone circuit to which the calling line may be connected. The scanner steps to its position BT and activates output conductor BT which extends a scan signal to busy tone circuit 222, as well as to the trunk side of the network controller. A stop scan signal is returned over conductor OBT to the input of gate SSICA within scanner control when busy tone circuit 222 is scanned. This signal stops the scanner in its position BT so that it maintains an enable or scan potential on scan conductor BT.

The application of the SLBT signal to gate 237 sets flip-flop 236. The "1" output of the flip-flop now enables element A of the sequence circuit 223 which, as already described, gates out the calling line number to the code leads and causes the switching network to establish a path from the calling line circuit to the selected busy tone circuit. The network returns a signal on conductor PC when this path is established. This signal steps sequence circuit 233 to its position E which applies a signal to the RESET conductor to restore the mode control and common control to its idle state.

Serving of Dial 9 Calls

In order to describe the manner in which the system serves dial 9-central office type calls, let it be assumed that station ST100 initiates such a call by dialing the customary prefix digit 9 to obtain a connection via a central office trunk circuit to the central office serving the PBX. This call is served by connecting an idle register to the calling line in a manner similar to that already described for the intra-PBX call. Let it be assumed that register 204 is selected for use on this dial 9 call and is connected by the network to station 100.

The calling party next dials the digit 9 which is stored in the register. In the manner well known in the art the register detects the dialing of the digit 9 and, over con-

ductor FOR, requests a common control register readout operation. When this request is honored, the register transmits information over the conductors of cable RN indicating that the prefix digit 9 has been dialed. This causes a HIGH to appear on output conductor H9 of the binary to decimal translator 270 on Fig. 2C. The HIGH on conductor H9 is extended from terminal 272-9 to terminal 273-9 and, in turn, to the lower input of gate SOT on Fig. 2E. The upper input of the SOT gate is HIGH at this time since both inputs of the gate RSNB are HIGH. With both of its inputs HIGH, gate SOT applies a LOW to switch the OT flip-flop to a set state in which its 1 output applies a HIGH to the lower input of gate OTA. The LOW that is on conductor LSE* at this time is inverted by gate LSE5 and applied to the upper input of gate OTA. Both inputs of gate OTA are now HIGH and, therefore, the gate applies a HIGH from its output to the upper input of both gates SLBT1 and SLOT. As is described in the subsequent paragraphs, gate SLOT is activated at this time if station 100 is permitted to initiate dial 9 calls. In this case, the system connects station 100 to an idle central office trunk. Conversely, gate SLBT1 is activated at this time if station 100 is not permitted to initiate dial 9 type calls. In this event, the station is connected to a busy tone trunk.

Let it initially be assumed that station 100 is permitted to place central office calls. In this case, conductor LS100 from line circuit LC100 would be connected through diode D00 to terminal CS2 rather than CS1 as shown. With the conductor being connected in this manner, the signal on conductor LS100 generates a LOW on conductor CS2* from the class of service detector 226. This signal, in turn, extends to Fig. 2E where it is inverted by gate CS2 and applied to the lower input of gate SLOT.

The output of gate OTA also extends to the middle input of gate 237 which, in turn, switches the flip-flop 236 to a set state and initiates the calling line select sequence operation in a manner similar to that already described. This sequence circuit steps from position to position to reidentify the calling line circuit. Finally, when the sequence circuit steps to its position C, it applies a LOW to its output conductor LSEA* which extends to the input of gate LSEA on Fig. 2E. This gate inverts the LOW and applies a HIGH to the second input of both gates SLBT1 and SLOT. The HIGH on conductor LS from the class of service detector 226 extends to the third input of both of these gates. Thus, the activation of one or the other of these gates depends upon which of gates CS1 or CS2 is activated. If gate CS2 is activated as a consequence of line 100 being assigned a class of service 2, the HIGH

on the lower input of gate SLOT activates it, applies a potential to conductor SLOT which extends to both the trunk bid circuit 219 and the scanner control 220B. The receipt of the
 5 SLOT signal by the trunk bid circuit activates conductor MOT which extends to all central office trunk circuits 214-1 through 214-9. The receipt of the signal on conductor SLOT by scanner control activates the
 10 scanner so that it operates in the manner already described to hunt and select an idle central office trunk circuit. When such a trunk circuit is found, a signal is applied to conductor OT1 and through the SSICA gate
 15 to conductor SSICA to stop the scanner 220 in its operative position associated with the trunk circuit. The activated output conductor of the scanner at this time identifies the trunk circuit. The output of the calling number store 240B of the register identifies the
 20 calling line as already described. Subsequently, the calling line select sequence circuit 233 steps to its position D, activates its conductor NETE* to cause the network to
 25 establish a path from the calling line to the selected outgoing trunk. Once this path is established, the calling party may then dial the remaining digits required to establish a connection to the called party.

30 Let it next be assumed that calling station 100 is not permitted to dial central office calls. This being the case, the LOW on conductor LS100 generates a LOW on class of service conductor CS1* and a HIGH on conductor LS. The LOW on conductor CS1* is inverted by gate CS1 on Fig. 2E. The resultant HIGH on the output of this gate is applied to the lower input of gate
 35 SLBT1 to activate it and drive its output HIGH. This HIGH extends to conductor SLBT which by means of the trunk bid circuit and the scanner 220 selects an idle busy tone trunk 222 and causes the calling party to be connected to this trunk in a manner
 40 similar to that described for connections to other trunk circuits. The busy tone supplied by this trunk circuit advises the calling party that the call he is attempting cannot be completed.

50 WHAT WE CLAIM IS:—

1. A switching system comprising a switching network having a line side and a trunk side, a plurality of line circuits connected to said line side, register means and
 55 a plurality of trunk circuits connected to said trunk side, controller means, a first set of code leads interconnecting said line circuits with said register means and the controller means, means for applying signals to said
 60 code leads from said controller means in order to identify a calling one of said line circuits requesting service, means for applying signals identifying said calling line circuit from said code leads to the register means,
 65 means for applying signals from said register

means to said code leads in order to select a called one of the line circuits, means for subsequently applying calling line identification signals from said register means to said code leads in order to reidentify said calling
 70 line circuit, and means responsive to the signals applied to said first code leads for controlling the establishment of network paths via a selected trunk circuit.

2. A switching system according to claim 1, wherein said means for applying signals in order to identify said calling line comprises first scanning means and wherein said register means comprises a plurality of registers, the system further comprising a second set
 75 of code leads interconnecting said trunk circuits and said registers with second scanning means, and means serving to apply signals from the second scanning means to the second code leads in order to select an idle
 80 one of the registers, said means for controlling the establishment of network paths further being responsive to signals applied to the second set of code leads and serving to control the establishment of a network path
 85 between the calling line and the selected register.

3. A switching system according to claim 2, wherein the selected register includes means for storing called line identification signals received from the calling line circuit via said network path, the system further comprising means responsive to said
 90 selection of a called line circuit for applying signals from said second scanning means to said second code leads in order to select an idle one of said trunk circuits, said means for controlling network paths serving to control the establishment of a network path
 95 between said called line circuits and said selected trunk.

4. A switching system according to claim 3, wherein said means for controlling the establishment of network paths is responsive to said reidentification of said calling line
 100 circuit and serves to establish a path between said calling line and said trunk circuit in order to connect said called line circuit with said calling line circuit via said selected trunk circuit.
 105

5. A switching system according to any one of claims 1 to 4, further comprising means for generating calling class information in response to said reidentification, means responsive to said class information
 110 for determining whether said calling line circuit is entitled to the class of service associated with the call, means responsive to a determination that the calling line circuit is not entitled to said class of service for indicating that said call cannot be completed,
 115 and means responsive to a determination that the calling line circuit is entitled to said class of service for enabling the further serving of said call.
 120
 125
 130



6. A switching system according to any one of claims 2 to 5, wherein said line circuits are connected to the first set of code leads on a coded basis with each respective line circuit being connected to a unique combination of the leads.

7. A switching system according to claim 2 or any preceding claim dependent thereon, wherein said trunk circuits and said registers are connected to said second set of code leads on a coded basis with each respective register and respective trunk circuit being connected to a unique combination of the leads.

8. A switching system according to claim 2 or any preceding claim dependent thereon, wherein said means for applying signals to identify the calling line circuit comprises means for activating the first scanning means to scan said line circuits by applying coded signals to the first set of code leads and means responsive to the scanning of said calling line circuit for stopping said line scanner in an operative position unique to said calling line circuit.

9. A switching system according to claim 8, wherein said means serving to apply signals from the second means to select said idle register comprises means responsive to the stopping of said first scanning means for activating said second scanning means to scan said registers by applying coded signals to the second set of code leads, means responsive to the scanning of an idle one of the registers for selecting that register, and means responsive to the selection of the idle register for stopping said second scanning means in an operative position unique to said selected register.

10. A switching system according to claim

2 or any preceding claim dependent thereon, further comprising means for determining the type of call represented by the called number information received by the register means from the calling line circuit, means responsive to a determination that said information represents a central office type call for applying said calling line identification signals from said register to the first set of code leads to reidentify the calling line circuit, means responsive to the reidentification for generating line class information indicating whether said calling line is permitted to initiate central office type calls, means responsive to an indication that said calling line circuit is so permitted for causing said second scanning means to apply coded signals to said second set of code leads in order to select an idle one of said trunks having connections extending to a central office, and means responsive to the selection of such a trunk for applying signals from both sets of code leads to said means for controlling the establishment of network paths in order to establish a path from the calling line circuit to said selected trunk circuit.

11. A switching system according to any one preceding claim, wherein the register means includes means for storing an identification of said calling line for said subsequent application of calling line identification signals to said first code leads.

12. A switching system substantially as herein described with reference to the accompanying drawings.

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