(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
28 August 2025 (28.08.2025)

WIPO | PCT

(10) International Publication Number
WO 2025/178988 A1

(51) International Patent Classification:
H01L 21/02 (2006.01) *C23C 16/44* (2006.01)
H01L 21/28 (2006.01) *C23C 14/22* (2006.01)

(21) International Application Number:
PCT/US2025/016527

(22) International Filing Date:
19 February 2025 (19.02.2025)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
63/557,314 23 February 2024 (23.02.2024) US

(71) Applicant: **LAM RESEARCH CORPORATION** [US/US]; 4650 Cushing Pkwy., Fremont, California 94538 (US).

(72) Inventors: **CHAN, Michael Anthony**; 4650 Cushing Pkwy., Fremont, California 94538 (US). **HUANG, Yanhui**; 4650 Cushing Pkwy., Fremont, California 94538 (US). **YOSHIZAWA, Katsunori**; 4650 Cushing Pkwy., Fremont, California 94538 (US). **SHAIKH, Fayaz A.**; 4650 Cushing Pkwy., Fremont, California 94538 (US). **PORTER, David W.**; 4650 Cushing Pkwy., Fremont, California 94538 (US).

(74) Agent: **MURRY, Price W.** et al.; WEAVER AUSTIN VILLENEUVE & SAMPSON LLP, P. O. BOX 70250, OAKLAND, California 94612-0250 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UY, UZ, VC, VN, WS, ZA, ZM, ZW.

(54) Title: NEGATIVE COEFFICIENT THERMAL EXPANSION MATERIALS FOR DYNAMIC BOW COMPENSATION APPLICATION

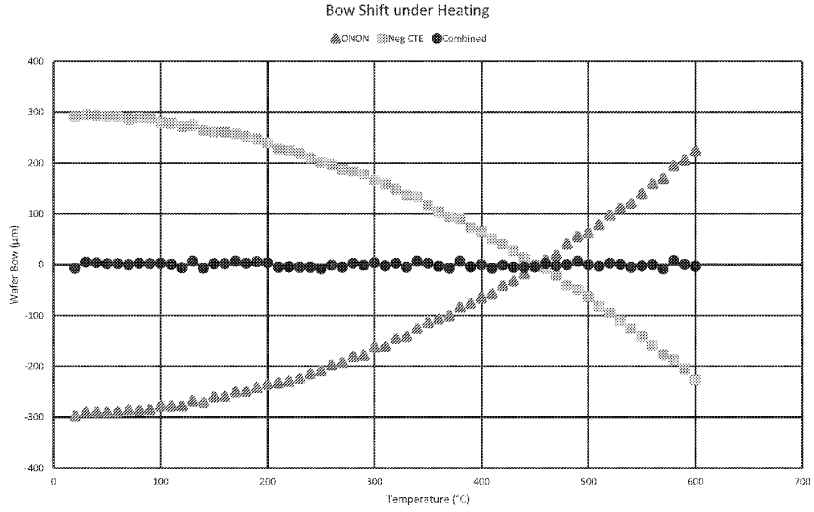


FIG. 5

(57) Abstract: Mitigating wafer bow of a semiconductor wafer includes depositing one or more backside layers that compensate for wafer bow caused by one or more frontside layers. Deposition of a backside layer stack may mitigate wafer bow caused by one or more frontside layers, including changes in wafer bow caused by the one or more frontside layers when the wafer is heated. Each of the backside layers may be deposited by a backside deposition apparatus.

[Continued on next page]

WO 2025/178988 A1

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*