

ABSTRACT OF THE DISCLOSURE

A selective calling receiver includes a decoder having a reference clock oscillator and a CPU having a CPU operating clock oscillator. The decoder includes a timing control circuit for generating a timing signal in synchronism with a synchronizing signal contained in a POCSAG signal and a BCH error correcting circuit for extracting a message code from the POCSAG signal. If the CPU is supplied with a message code from the decoder when no timing signal is inputted from the decoder, the CPU stores the message code in RAM in the CPU or a buffer memory area of external RAM connected to the CPU. In this case, the CPU operates with a first clock signal generated by the reference clock oscillator. When the CPU is supplied with the timing signal from the decoder, the CPU reads the message code from the RAM or the buffer memory area and processes the message code with a second clock signal generated by the CPU operating clock oscillator and the second clock signal has a frequency higher than the frequency of the first clock signal.

This Sheet Has Been Replaced

