CLAIMS

What is claimed is:

1. A transistor device, comprising:

a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode; and

source and drain regions formed in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 1E20 cm^{-3}.

2. The device of claim 1 wherein the device is one of a planar or FinFET PMOS transistor.

3. The device of claim 1 further comprising metal-germanide source and drain contacts.

4. The device of claim 1 further comprising an interlayer dielectric over the source and drain regions.

5. The device of claim 1, the device further comprising:

a buffer between the substrate and the boron doped germanium layer.

6. The device of claim 5 wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 95 atomic %.

7. The device of claim 6 wherein the high concentration reflects pure germanium.

8. The device of claim 5 wherein the buffer has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.

9. The device of claim 1 wherein the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon.

10. The device of claim 9 wherein the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a germanium concentration in excess of 95 atomic %.

11. The device of claim 9 wherein the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.

12. The device of claim 9 wherein the boron doped silicon germanium portion has a fixed germanium concentration, and the device further comprises a buffer between the boron doped silicon germanium portion and the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 1E20 cm^{-3}.

13. The device of claim 9 wherein the transistor has a Rext value of less than 100 Ohm*um.

14. A transistor device, comprising:

a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode;

source and drain regions formed in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 2E20 cm^{-3}; and

metal-germanide source and drain contacts.

15. The device of claim 14, the device further comprising:

a buffer between the substrate and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in

excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}.

16. The device of claim 14 wherein the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon.

17. The device of claim 16 wherein the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a germanium concentration in excess of 95 atomic %.

18. The device of claim 17 wherein the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}.

19. The device of claim 16 wherein the boron doped silicon germanium portion has a fixed germanium concentration, and the device further comprises a thin buffer between the boron doped silicon germanium portion and the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 2E20 cm^{-3}, the buffer having a thickness of less than 100 Angstroms.

20. A method for forming a transistor device, comprising:

providing a substrate having a channel region;

providing a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode; and

forming source and drain regions in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 1E20 cm^{-3}.

21. The method of claim 20, further comprising:

providing a buffer between the substrate and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.

22. The method of claim 20 wherein the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon.

23. The method of claim 22 wherein the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a germanium concentration in excess of 95 atomic %.

24. The method of claim 22 wherein the boron doped silicon germanium portion has a fixed germanium concentration, and the method further comprises providing a buffer between the boron doped silicon germanium portion and the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 1E20 cm^{-3}.

25. The method of claim 24 wherein the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.

CLAIMS

What is claimed is:

1. A transistor device, comprising:
a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode;

source and drain regions formed in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions and corresponding tip regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 1E20 cm^{-3}; and

a buffer between the substrate and the boron doped germanium layer;

wherein the buffer has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.

2. The device of claim 1 wherein the device is one of a planar or FinFET PMOS transistor.

3. The device of claim 1 further comprising metal-germanide source and drain contacts.

4. The device of claim 1 further comprising an interlayer dielectric over the source and drain regions.

5. The device of claim 1 wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 95 atomic %.

6. The device of claim 5 wherein the high concentration reflects pure germanium.

7. A transistor device, comprising:
a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode; and

source and drain regions formed in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or

a corresponding one of the spacers, wherein the source and drain regions and corresponding tip regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 1E20 cm^{-3};

wherein the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon; and

wherein the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.

8. The device of claim 7 wherein the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a germanium concentration in excess of 95 atomic %.

9. The device of claim 7 wherein the device is one of a planar or FinFET PMOS transistor.

10. The device of claim 7 further comprising metal-germanide source and drain contacts.

11. The device of claim 7 further comprising an interlayer dielectric over the source and drain regions.

12. The device of claim 7 wherein the transistor has a Rext value of less than 100 Ohm*um.

13. A transistor device, comprising:
a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode; and

source and drain regions formed in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions and corresponding tip regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 1E20 cm^{-3};

wherein the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon; and

wherein the boron doped silicon germanium portion has a fixed germanium concentration, and the device further comprises a buffer between the boron doped silicon germanium portion and

the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 1E20 cm^{-3}.

14. The device of claim 13 wherein the transistor has a Rext value of less than 100 Ohm*um.

15. The device of claim 13 wherein the device is one of a planar or FinFET PMOS transistor.

16. The device of claim 13 further comprising metal-germanide source and drain contacts.

17. The device of claim 13 further comprising an interlayer dielectric over the source and drain regions.

18. The device of claim 13 wherein the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a germanium concentration in excess of 95 atomic %.

19. A transistor device, comprising:
a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode;

source and drain regions formed in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions and corresponding tip regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 2E20 cm^{-3};

metal-germanide source and drain contacts; and

a buffer between the substrate and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}.

20. A transistor device, comprising:

a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode;

source and drain regions formed in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions and corresponding tip regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 2E20 cm^{-3}; and

metal-germanide source and drain contacts;

wherein the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon;

wherein the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a germanium concentration in excess of 95 atomic %; and

wherein the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}.

21. A transistor device, comprising:
a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode;

source and drain regions formed in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions and corresponding tip regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 2E20 cm^{-3}; and

metal-germanide source and drain contacts;

wherein the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon; and

wherein the boron doped silicon germanium portion has a fixed germanium concentration, and the device further comprises a thin buffer between the boron doped silicon germanium portion and the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 2E20 cm^{-3}, the buffer having a thickness of less than 100 Angstroms.

22. A method for forming a transistor device, comprising:
providing a substrate having a channel region;

providing a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode;

forming source and drain regions in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions and corresponding tip regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 1E20 cm^{-3}; and

providing a buffer between the substrate and the boron doped germanium layer, wherein the buffer has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.

23. The method of claim 22 wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 95 atomic %.

24. A method for forming a transistor device, comprising:
providing a substrate having a channel region;

providing a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode; and

forming source and drain regions in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions and corresponding tip

regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 1E20 cm^{-3};

wherein the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon; and

wherein the boron doped silicon germanium portion has a fixed germanium concentration, and the method further comprises providing a buffer between the boron doped silicon germanium portion and the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 1E20 cm^{-3}.

25. The method of claim 24 wherein the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.