

FAULT PROTECTION USING MICROPROCESSOR POWER UP RESET

This invention relates to fault detection circuits for television receivers having a run mode in which run mode power supplies
5 are active, and a standby mode in which power is provided only to selected load circuits.

Various potentially dangerous or potentially damaging faults may occur in television receivers as a result of open circuits, short
10 circuits, failures of components and the like. One example of a potentially dangerous fault condition is emission of X-rays due to excessive electron beam current or overvoltage conditions in the high voltage ultor power supply. Another example of a
15 potentially damaging fault is an open circuit in the vertical deflection winding which prevents electron beam scanning and causes the electron beam to burn the screen phosphors along a line or at a spot, permanently damaging the phosphors. It is known to detect fault conditions such as these, and to respond by disabling the power supply to selected run mode load circuits of
20 the television receiver to alleviate the dangerous or damaging aspects of the fault.

Many television receivers include microprocessor controllers which, among other functions, control switching of the television
25 receiver between the run mode in which all the power supplies and circuits are operational, and the standby mode in which power is supplied only to those circuits which are needed for switching back into the run mode when appropriate, i.e., the standby loads. In connection with a television receiver having an
30 infrared remote control signal receiver, only the remote control receiver and the microprocessor servicing the remote control receiver need to remain powered in the standby mode, awaiting a signal from the user to switch back into the run mode. The remaining circuits, which are the run mode loads, are not powered
35 in the standby mode.

Some run mode loads are powered as a function of horizontal deflection energization. For example, the high voltage supply for



screen, focus and final anode electrodes, and certain other run mode supplies, are coupled to secondary windings of the horizontal output or flyback transformer. The primary winding of the horizontal output transformer is energized by flyback or retrace pulses generated by the horizontal output transistor.

In addition to generating power through the flyback transformer, a television receiver may also have a switched mode power supply that supplies and regulates power to run mode loads by adjusting the pulse width of pulses applied to the primary winding of a power transformer having secondary windings coupled to the respective run mode loads. Various DC supply voltages, may be developed to power run mode loads, including standby loads such as the microprocessor controller.

In the standby mode, the horizontal oscillator or the B+ power supply to the flyback transformer may be disabled, removing the supply of power to the run mode loads; whereas the microprocessor is powered as long as voltage is available at the AC mains. The microprocessor continues to execute its stored program in the standby mode, including input/output functions such as monitoring the remote control receiver, holding a run/standby output at a level that indicates a standby condition, etc.

A hold or save input may also be provided on the microprocessor for signalling impending loss of AC mains power. The hold input is activated immediately upon loss of power and signals the microprocessor, for example by interrupt, to store memory information respecting operational parameters at the time of the hold signal generation.

The microprocessor must be reset when the television receiver is initially coupled to the AC mains or upon restoration of AC mains power. A reset input is provided in order to clear or initialize certain internal registers in the microprocessor, for example the program counter, by means of a reset circuit which holds the reset input true for a short time after power is applied to the



microprocessor. Program execution does not begin after power up until the reset input has been activated.

After the reset line has been activated, further microprocessor
5 operations are disabled so long as the reset input is true, the
microprocessor is unable to monitor its inputs, to place data on its
outputs, or otherwise to execute instructions while the reset input
is held true. The reset line must then be released to resume
normal microprocessor programmed operation. Hence, it is not
10 desirable to latch the reset input of the microprocessor upon
detection of a fault, since this renders the microprocessor
inoperative.

The microprocessor is programmed such that when commencing
15 operation after a reset, the television receiver initially assumes
the standby mode. It is thus necessary for the user to signal via
the remote controller in order to switch from the standby mode to
operation in the run mode.

20 It is known to couple a fault detection circuit having a latched
output to a data input pin of a microprocessor, which by virtue of
control programing, disables horizontal scanning as a protective
measure, thus forcing the television receiver into the standby
mode. However, it is desirable to avoid devoting an
25 microprocessor input pin solely to this one function.

A power supply can be switched between a standby mode of
operation and a run mode of operation. A microprocessor has a
reset input for resetting the microprocessor and an output coupled
30 to the power supply for switching between the operating modes.
A reset signal generator is connected to the reset input and is
responsive to a fault in either the power supply or a load
connected thereto. Thus a fault condition initiates a
microprocessor reset condition which, via the control output,
35 causes the power supply to assume the standby mode of operation

Another inventive feature is to disable the horizontal deflection
circuits upon overvoltage in a power supply coupled to the



horizontal deflection circuits and/or upon detection of an open or short circuit in the television receiver deflection circuits, initiating a power-up reset sequence for resetting the microprocessor controller.

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FIGURE 1 is a schematic block diagram of a partial television receiver incorporating microprocessor controlled fault protection, according to the invention.

FIGURE 2 is a detailed schematic diagram of FIGURE 1, using
10 reference numerals corresponding to those appearing in FIGURE 1 to identify corresponding elements.

A microprocessor 22 as shown in FIGURE 1, controls switching of the television receiver between the run mode and the standby
15 mode, providing an output STBY which in the run mode enables operation of the horizontal deflection circuits of a deflection IC 30, for example type M52043SP. Microprocessor 22 may be responsive to keyboard inputs or to remote control signals received by a remote control receiver, not shown, to initiate
20 switching between modes. Microprocessor 22 may also control the television RF tuner, operate an on-screen display, and provide other functions as required.

In the run mode, generation and deflection of the electron beam
25 of the television receiver cathode ray tube, not shown, is enabled when, for example, the STBY output of the microprocessor is logical low, and is disabled when STBY is logical high. When STBY is low, a SMPS voltage is coupled, via switch transistors (not shown), to power the horizontal oscillator 130 at pin 11 of
30 deflection IC 30.

Horizontal oscillator 130 is coupled to a driver stage 45 (shown in Figure 2) which drives a horizontal output stage 44, including a
35 horizontal output transistor TH, a damper diode DC, a retrace capacitor CR, a horizontal deflection winding YH and an S-shaping capacitor CS. The primary winding W1 of a flyback transformer FBT is coupled to horizontal output stage 44 at the collector of transistor TH.

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Secondary windings, partially shown, of the flyback transformer are coupled to various run mode power supplies. The voltages on the secondary windings tend to vary together, with variations in B+ input voltage and loading. Accordingly, the voltage level on one of the secondary windings may be sensed and compared to a reference, for detecting voltage variations on all the transformer secondaries.

10 The ultor voltage supply U (shown in Figure 2) is a run mode load generated from the secondary windings of transformer FBT. In the event that the ultor voltage amplitude becomes excessive X ray radiation may be produced. In accordance with an inventive feature, in the event of overvoltage, a fault detector 28 monitors the voltage level of one of the secondary windings of transformer FBT, winding W2, and produces an output which is coupled to a reset circuit 26 of microprocessor 22. A reset to the microprocessor causes the receiver to assume the standby mode which removes power to the horizontal reference oscillator, which in turn removes the counted down drive signal from the horizontal output transistor, ceasing generation of the flyback derived voltages.

As a further inventive feature, in connection with a vertical deflection circuit 46, fault detector 28 is also arranged to trigger a microprocessor reset when the current in the vertical deflection winding YV is such as to indicate a potentially dangerous or damaging fault. In the event of a short or open circuit in either vertical deflection winding YV or circuitry, drive from vertical output stage 32, coupled to vertical oscillator and driver 230 of deflection integrated circuit 30, could become excessive; or the lack of vertical deflection could result in the electron beam burning the screen phosphors. Accordingly, the current in the deflection yoke YV, is sensed by the voltage across a current sensing resistor RS, which also provides the vertical feedback signal VFB. The current sense signal is supplied to fault detector 28 to initiate microprocessor reset upon detection of vertical deflection circuit fault. Resetting the microprocessor places the

receiver in the standby mode wherein power to the horizontal oscillator section of IC30 is inhibited, terminating the reference oscillator signal that is counted down to produce the vertical rate drive signal.

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Advantageously, the power-up reset input to the microprocessor provides a dual function, to reset the television receiver circuitry when the television receiver is initially connected to the AC mains or when AC mains power is restored after interruption, and to
10 place the television receiver in a standby mode when a fault condition is detected. Microprocessor 22 is thus programmed to initiate operation in the standby mode following a reset, which can be generated by the power-up reset circuit 26 or by the fault detector 28.

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The microprocessor must remain powered in both the run mode and the standby mode, since in the standby mode the microprocessor must monitor its inputs to detect a run mode command. A switched mode power supply 34, coupled to a
20 voltage regulator 24, produces at least one output voltage A+, which is available in both the run mode and standby mode. Output voltage, A+ is regulated by transistor TR08, to provide voltage +V2 coupled to the VCC pin of microprocessor 22.

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The A+ voltage supply is also coupled to hold circuit 25 which detects a loss of power and signals to the microprocessor that a power failure has occurred. As long as sufficient voltage remains at the microprocessor VCC pin to continue operation (e.g., during discharge of storage capacitors, reserve batteries and the like
30 coupled to the VCC pin), the microprocessor responds to the HOLD signal at its input by storing present operating parameter data and otherwise performing an orderly power-down sequence. When power is restored, the television receiver can resume operation using these stored operating parameters. The hold
35 input uses an input line of the microprocessor, such as an interrupt, for signalling loss of power.



By storing a record of the HOLD signal and checking for the record when initializing after a reset, the microprocessor can determine whether it is initializing after a fault detection or after a power loss and take appropriate action. For example upon occurrence of a predetermined number of successive fault detections, the microprocessor can shut down permanently and not respond to a further commands to switch into the run mode. This condition requiring that the television receiver be serviced, or decoupled temporarily from the AC mains supply, before the microprocessor will implement run commands and enter the run mode.

A more detailed embodiment is shown in FIGURE 2. The output +V2, of series pass voltage regulator 24, is coupled to microprocessor 22 through a series diode DR01 and a choke LR02. A capacitor CR86 is coupled between the VCC pin and ground to provide noise suppression. In the event that voltage supply A+ fails, the VCC supply, to microprocessor 22, is sustained by current supplied by capacitor CR20, and battery XR01 coupled via resistor RR43. Under failure conditions, diode DR01 is reversed biased by battery DR01 voltage, thus preventing the powering of loads other than microprocessor 22. Diode DR23 couples the regulated +5 volts DC output of regulator 24 to additional loads, not shown.

The reference level of series regulator 24 is defined by a zener diode DR05, coupled to the base of a series pass transistor TR08 through a resistor RR56. The cathode of zener DR05 is coupled to the unregulated A+ supply, through a resistor RR50. A capacitor CR21 is coupled to the junction of resistor RR50 and the cathode of zener diode DR05. A resistor RR81, is coupled between the anode of zener diode DR05 and ground. Thus the voltage across resistor RR81 represents the current through zener diode DR05, and is present only when the voltage applied to zener diode DR05 exceeds the zener reference level, for example 6.2 volts.

After a power failure of the AC mains, or when the television receiver is initially coupled to the AC mains supply, series regulator 24 starts to conduct due to the A+ voltage coupled to the base transistor TR08 through resistors RR50 and RR56. However,





until the voltage at the cathode of zener diode DR05 reaches the zener reference level, the voltage at the emitter of transistor TR08 is unregulated.

5 Assume a situation where battery XR01 is discharged or missing. The microprocessor becomes operational before VCC reaches its regulated level of 5 volts, e.g., at a threshold level for VCC of about 3 volts DC.

10 In order to ensure that microprocessor 22 initiates operation in a predetermined manner, a power-up reset signal is generated after the VCC voltage has reached a level adequate to reset internal registers in the microprocessor, including the program counter which defines the memory location of the instruction to be
15 executed by the central processor. To create this sequence of events, capacitor CR21 is coupled to the cathode of zener diode DR05 and to the emitter of a PNP transistor TR06. The base of transistor TR06 is coupled to the emitter of transistor TR06 through a resistor RR46. The base of transistor TR06 is coupled to
20 the collector of an NPN transistor TR07. The base of transistor TR07 is bypassed by a capacitor CR19, and coupled via a resistor RR93, to the collector of transistor TR06. The junction of zener diode DR05 anode and resistor RR81 is coupled to the base of transistor TR07 by a resistor RR89.

25 Initially when power appears at voltage terminal A+, capacitor CR21 begins to charge via resistor RR50. When capacitor CR21 has charged to 4 or 5 volts, sufficient VCC voltage is available to power microprocessor 22. Zener diode DR05 does not begin to
30 conduct until a later time when the voltage across capacitor CR21 reaches 6.2 volts. After the voltage VC developed across capacitor CR21 exceeds 6.9 volts, transistor TR07 turns on, thereby turning on transistor TR06.

The collector of transistor TR06 is coupled via resistor RR84 to the HOLD input of microprocessor 22, which is also coupled through resistor RR70 and capacitor CR80, connected in parallel, to ground.

35 With transistor TR07 conducting, voltage VC is applied via series coupled capacitor CR14 and resistor RR63 to the base of a reset transistor TR12 in reset circuit 26. A parallel arrangement of a capacitor CR15 and a resistor RR64 is coupled between the base of

transistor TR12 and ground. The collector of transistor TR12 is coupled to the microprocessor reset pin, and to VCC via a resistor RR65.

- 5 Initially capacitors CR14 and CR15 of reset circuit 26 are discharged. When transistor TR06 turns on, both capacitors are charged by voltage VC. When the voltage across capacitor CR15 reaches 0.7 volt, transistor TR12 is turned on. When transistor TR12 conducts, the RESET input to microprocessor 22 is pulled
10 down, thereby resetting the microprocessor. However, program execution will not commence until the reset line is released.

- Capacitor CR14 continues to charge to the point where the capacitor blocks current from transistor TR06 to the base of
15 transistor TR12. Transistor TR12 then turns off after holding the reset input to microprocessor 22 low for about 20 milliseconds. In this way, a negative going, momentary reset pulse, of fixed duration is generated at the RESET input.

- 20 When the reset line is released the microprocessor is initialized and program execution starts. One of the first instructions designates the status of the I/O ports and in particular makes pin 20 (STBY) an output with a high state following a reset operation. As described earlier, when STBY is high, the supply to the
25 horizontal oscillator is inhibited which prevents generation of scanning waveforms and flyback derived power supplies. A high STBY signal also inhibits coupling of horizontal rate flyback pulses to synchronize the SMPS 34. With STBY high the receiver is placed in the standby mode with the microprocessor waiting to
30 receive a run command from either the keyboard switches or the remote control receiver.

- Transistors TR06 and TR07 are also part of a hold circuit 25 which signals microprocessor 22 at its HOLD input that AC mains power
35 has been lost. When the A+ voltage has decreased to the point that voltage VC is less than 6.9 volts, transistor TR06 and TR07 turn off, causing the microprocessor HOLD line to decay to zero volts. A low level on the Hold line causes a program interrupt to



initiate a routine to store in the appropriate registers, operational parameters needed when power is restored. Since VCC to the microprocessor is sustained (as previously described), the HOLD interrupt will be processed before the VCC voltage has decreased
5 below the minimum level needed to sustain operation of the microprocessor.

In accordance with an inventive feature, reset circuit 26 is also activated under television receiver fault conditions. For this
10 purpose, the base of transistor TR12 is coupled to fault detection circuit 28, whereby the power-up reset signal is generated in the event of a detected fault.

A zener diode DR21, is coupled to the junction of a voltage divider
15 defined by resistors RR94 and RR95, which are coupled in series between ground and the output of a peak rectified retrace pulse from a secondary winding W2 of flyback transformer FBT. The retrace pulse is coupled from winding W2 and is coupled via a diode DR22, and filtered by a capacitor
20 CR95 to generate the peak rectified retrace pulse voltage sense signal VX, at the junction of voltage divider resistors RR95 and RR94.

Zener diode DR21 forms a threshold comparator conducting only
25 when the voltage across the diode exceeds its breakdown voltage, for example 10 volts. Transistor TR12 is turned on when the peak rectified signal VX, from winding W2 exceeds the predetermined level defined by the voltage divider and zener breakdown voltage.

30 In this manner a reset signal is generated when the voltage on the power supplies coupled to the secondary windings of flyback transformer FBT are being overdriven. In the reset mode, microprocessor 22 places the television receiver in standby operation by disabling horizontal oscillator 130 of IC 30. With
35 horizontal oscillator 130 stopped, the generation of flyback voltages ceases, resulting in the cessation of power supplies generated therefrom, hence providing the required overvoltage protection.





As an added advantageous feature, placing the television receiver in standby automatically releases the reset line of the microprocessor due to the disappearance of flyback pulse sense
5 voltage VX and consequently, turning off of reset transistor TR12.

In addition to detection of overvoltage conditions in the secondaries of transformer FBT, fault detection circuit 28 detects
10 potentially dangerous or damaging conditions in vertical deflection circuit 46.

The voltage across current sensing resistor RF01 in vertical output stage 32 is rectified by a diode DF06 and filtered by a capacitor CF16. The current in vertical deflection winding YV is an
15 alternating current sawtooth. Diode DF06 and capacitor CF16 define a negative peak rectifier coupled to the AC voltage on the current sensing resistor RF01. In normal operation, the voltage at the cathode of diode DF06 has a negative peak of about -2.5 volts, DC

20 The peak rectified voltage, -VS, at the anode of diode DF01, is coupled to the base of transistor TR12 through series resistors RF28 and RR99. At the junction of resistors RF28 and RR99, a positive reference voltage, of e.g. +5.4 volts, derived from a zener
25 diode DP55, is summed with the negative voltage -VS. The reference voltage is generated by a zener diode DP55 coupled to a flyback generated positive supply, +V1, through a resistor RP56 and decoupled by a capacitor CP55. Resistors RF28 and RF29 are
30 chosen such that normally the negative voltage at the anode of diode DF06 and the positive voltage at the anode of zener DP55 balance each other to keep transistor TR12 cut off.

In the event of short or open circuits in deflection winding YV or DC blocking capacitor CF01, the negative sense voltage -VS
35 disappears or becomes positive. Thus no offset bias is available against the voltage from zener diode DP55 in order to keep transistor TR12 nonconductive. Transistor TR12 turns on and generates a reset to microprocessor 22. The television receiver is

placed in the standby mode, disabling IC30 and its internal vertical oscillator. The reset thus prevents vertical output IC32 or the power supply from being damaged or allowed to overheat when the vertical output load is open or short circuited. The
5 assumption of the standby mode disables the run mode power supplies thus preventing the possibility of the electron beam burning the phosphor surface of the display tube.

Following a reset generated by fault detection circuit 28,
10 microprocessor 22 continues to operate in the normal manner in the standby mode, monitoring its inputs for a command, from the keyboard or remote, to initiate operation in the run mode. The microprocessor 22 may include in the initialization routine a conditional jump as a function of whether or not the reset
15 condition followed a power loss or a fault detection. The microprocessor may also be programmed to discriminate between a condition wherein it is possible to resume operation in the same manner as before reset, i.e., loss of AC mains power without fault, and a condition where the reset was generated by a fault.

20 The control program of microprocessor 22 may determine if a reset is generated due to a fault condition or as a consequence of powering up. Fault generated resets may be counted over some time period, and if some predetermined number is exceeded, the
25 microprocessor may cease executing an inputted run mode command, thus inhibiting operation in run mode. If the microprocessor permanently inhibits run operation, the television receiver must be disconnected from the AC power mains, or serviced, before the microprocessor will permit selection of the
30 run mode of operation.

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WHAT IS CLAIMED IS:

1. A fault protection apparatus, comprising:
a digital control (22) circuit having an output and a reset input;
means for generating (25) a first reset signal coupled to said input for resetting the digital control circuit and placing said output in a standby mode state;
a deflection circuit (44) and a run mode power supply (u) coupled to the deflection circuit (44) and to a run mode load, the deflection circuit being responsive to the output (STBY) of the digital control circuit to enable deflection circuit operation in a run mode and to disable deflection circuit operation in a standby mode; characterized by
a fault detection circuit (28) having a sensing input coupled to detect a fault in one of said deflection (44) and said load, and having an output coupled to the reset input of the digital control circuit for generating a second reset signal responsive to fault detection.
2. The apparatus according to claim 1, characterized in that said reset signal generating means (26) is responsive to power appearance.
3. The apparatus according to claim 2, characterized in that said digital control circuit (22) has programming to determine the source of the reset signal and to count fault generated reset signals, inhibiting execution of run mode commands when a predetermined fault signal count is exceeded.
4. The apparatus according to Claim 1, characterized in that the digital control circuit (22) is a microprocessor operable to control operation of a television apparatus in the standby mode after reset.
5. The apparatus according to Claim 2, characterized in that the reset signal generator (26) is a delay circuit coupled between the reset input and a power supply voltage.





6. The apparatus according to Claim 4, characterized in that the microprocessor (22) includes a nonvolatile memory, a hold input (pin 34) coupled to a power supply of a television apparatus, and further comprising means (XR01) for providing a delay in loss of power to the microprocessor after loss of power at said power supply coupled to the hold input, the microprocessor being operable during said delay to store at least one operational parameter in said nonvolatile memory, and to initiate operation upon resumption of power as a function of said operational parameter.

7. The apparatus according to Claim 1, characterized in that the deflection circuit (44) includes a horizontal rate output stage and a horizontal oscillator (130) coupled to the output stage, the run mode power supply (W3) being coupled to the horizontal output stage.

8. The apparatus according to Claim 7, characterized in that the horizontal output stage (44) includes a flyback transformer (FBT) having a secondary winding (W3) coupled to the run mode power supply to generate a plurality of voltage supplies.

9. The apparatus according to Claim 1, characterized in that the fault detection circuit (28) includes a voltage comparator coupled to said run mode load, the voltage comparator (DR21) triggering the reset signal upon a voltage at the run mode load passing at least one predetermined limit voltage representing a fault condition.

10. The apparatus according to Claim 9, characterized in that the predetermined limit voltage defines an overvoltage condition, whereby overvoltage at the run mode power supply (W2) occurs together with overvoltage at said screen electrode such that disabling the deflection circuit provides X-ray protection.





11. The apparatus according to Claim 1, characterized in that the fault detection circuit (28) is coupled to a vertical deflection circuit (46) of the television apparatus, the fault detection circuit being operable to detect at least one of a short circuit condition and an open circuit condition in the vertical deflection circuit.

12. The apparatus according to Claim 11, characterized in that the vertical deflection circuit includes a deflection current sensing resistor (RF01), the fault detection circuit (28) being coupled to the current sensing resistor.

13. The apparatus according to Claim 12, characterized in that the fault detection circuit (28) includes a negative peak rectifier (DF01) coupled to the current sensing resistor, and a positive voltage reference (DP55) supply coupled to an output of the negative peak rectifier, a switching transistor (TR12) being coupled to the reset input (pin 38) and to sum of outputs of the negative peak rectifier (DF01) and the positive voltage reference (DP55), whereby the fault detection circuit is operable to detect said open circuit and short circuit conditions by positive displacement of said sum of outputs.

14. An apparatus, comprising:

a digital control circuit (22) having a reset input (pin 33) and control means for controlling a television apparatus; a reset signal generated by one of at least two reset signal generating means, coupled the reset input to reset the digital control circuit to assume operation of the television apparatus in a predetermined mode; a first one of two reset signal generating means responsive to the application of power; and a second one of two reset signal generating means being responsive to a detected fault condition; characterized by

the digital control circuit having programming to determine the source of the reset signal and to count fault generated reset signals, inhibiting execution of run commands when a predetermined fault signal count is exceeded.



15. A power supply apparatus, comprising :

a power supply having a control input for switching between a standby mode and a run mode of operation;

a microprocessor having a reset input and an output coupled to the power supply control input, said microprocessor output being switchable between standby and run mode states; characterized by

a reset signal generator coupled to the reset input for initiating a reset mode of operation by said microprocessor including the switching of said output to said standby mode state;

and responsive to a fault in one of a power supply and load circuit energized therefrom, and having an output coupled to reset the microprocessor for placing said power supply in a standby mode of operation.

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