FIG. 1

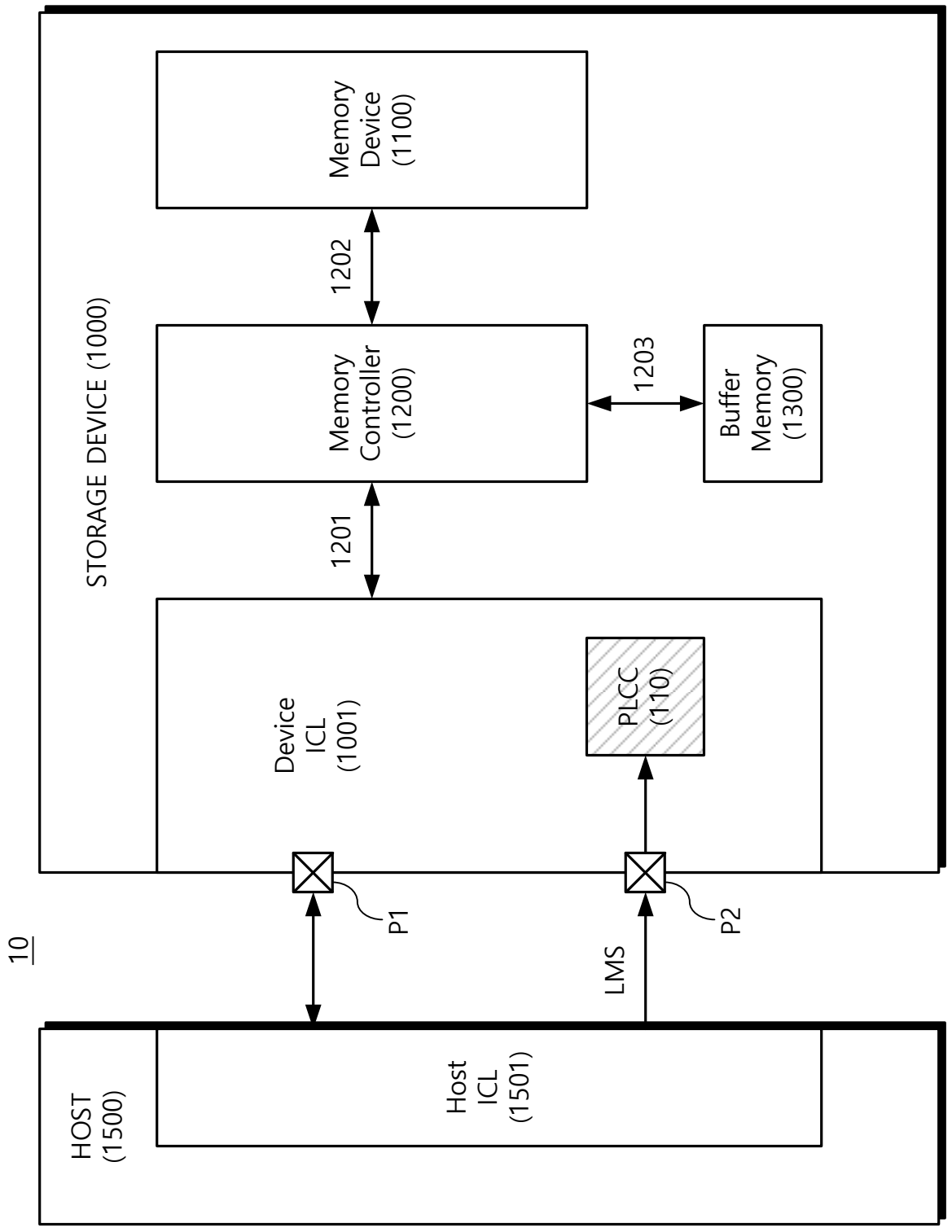

10
HOST (1500)
Host ICL (1501)
LMS
P1
P2
STORAGE DEVICE (1000)
Device ICL (1001)
PLCC (110)
1201
Memory Controller (1200)
1203
Buffer Memory (1300)
1202
Memory Device (1100)

FIG. 2

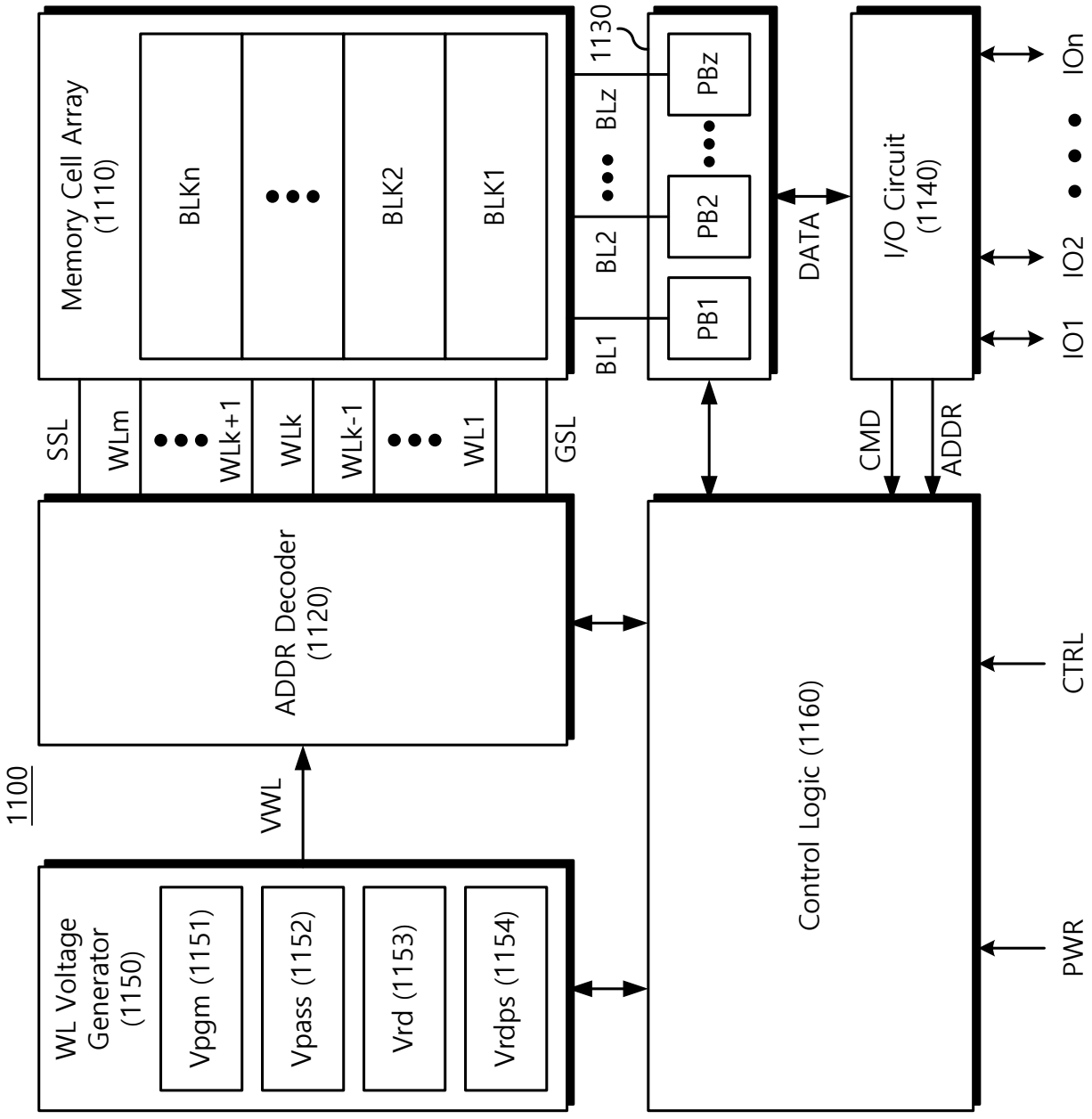

1100
WL Voltage Generator (1150)
Vpgm (1151)
Vpass (1152)
Vrd (1153)
Vrdps (1154)
VWL
ADDR Decoder (1120)
SSL
WLm
WLk+1
WLk
WLk-1
WL1
GSL
Memory Cell Array (1110)
BLKn
BLK2
BLK1
1130
BLz
BL2
BL1
PBz
PB2
PB1
DATA
I/O Circuit (1140)
IOn
IO2
IO1
CMD
ADDR
Control Logic (1160)
CTRL
PWR

FIG. 3

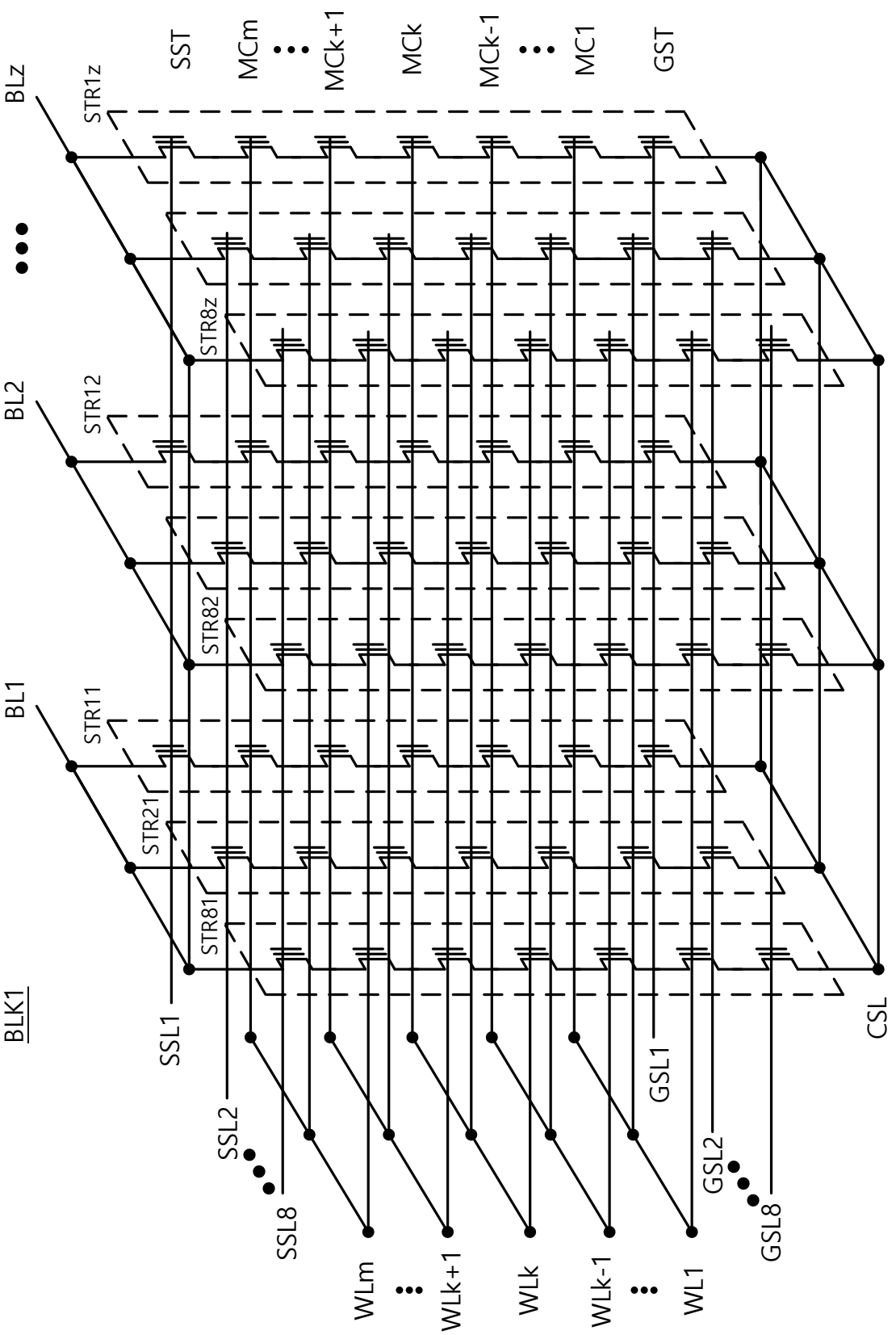

BLK1
BL1
BL2
BLz
STR11
STR21
STR81
STR12
STR82
STR8z
STR1z
SST
MCm
MCk+1
MCk
MCk-1
MC1
GST
SSL1
SSL2
SSL8
WLm
WLk+1
WLk
WLk-1
WL1
GSL1
GSL2
GSL8
CSL

FIG. 4

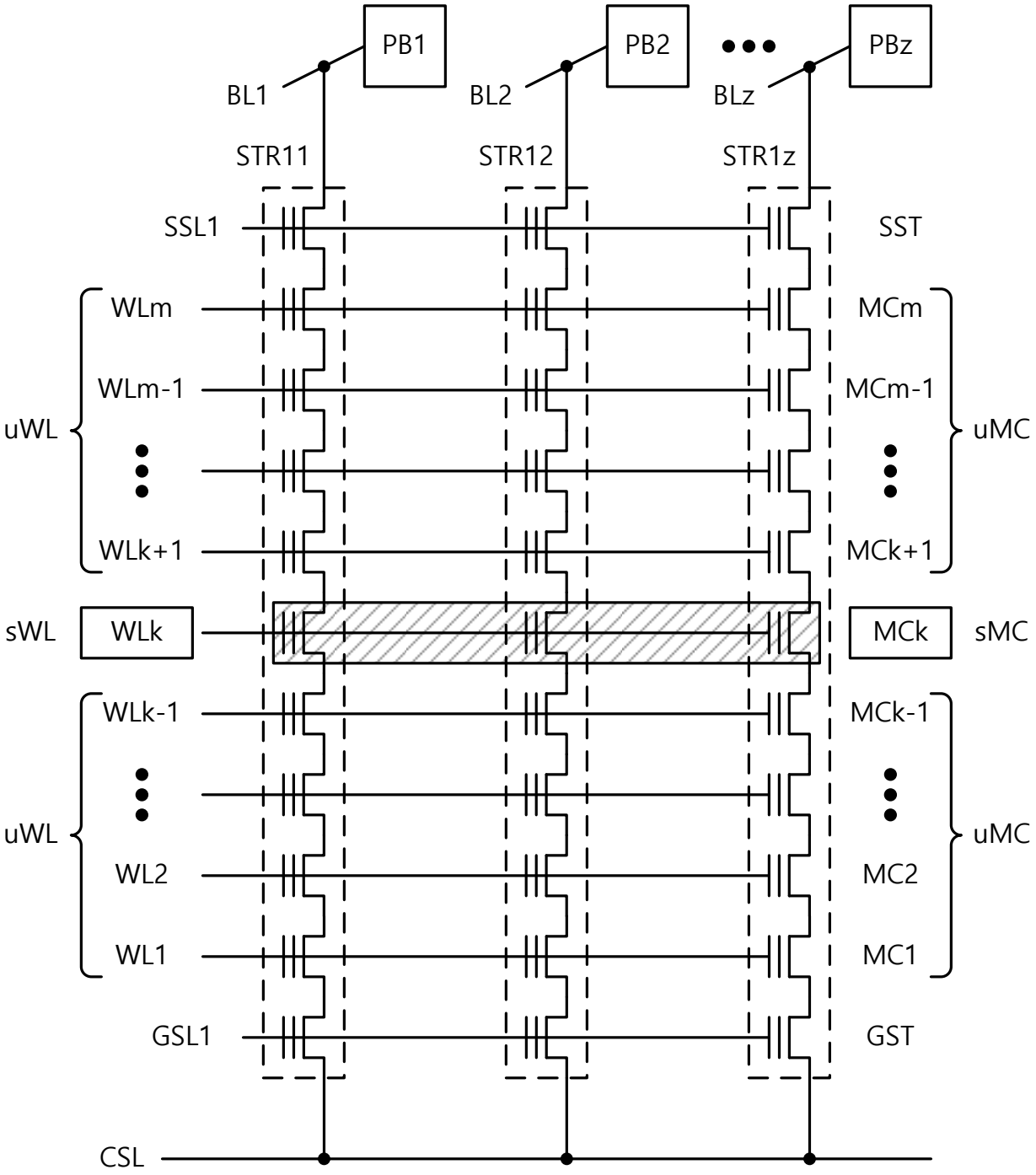

PB1
PB2
PBz
BL1
BL2
BLz
STR11
STR12
STR1z
SSL1
SST
WLm
MCm
WLm-1
MCm-1
uWL
uMC
WLk+1
MCk+1
sWL
WLk
MCk
sMC
WLk-1
MCk-1
uWL
uMC
WL2
MC2
WL1
MC1
GSL1
GST
CSL

FIG. 5

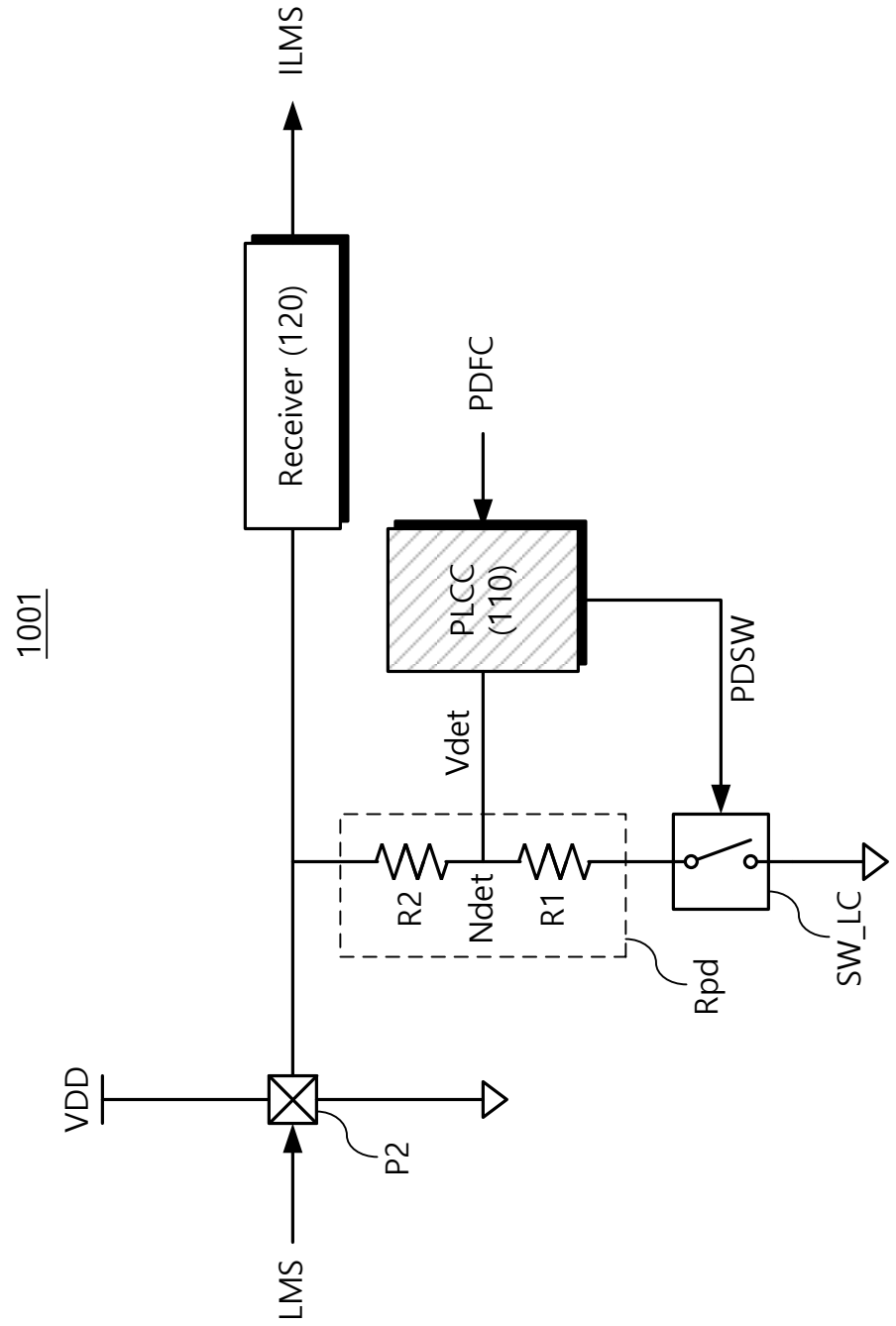

1001
ILMS
Receiver (120)
PDFC
PLCC (110)
PDSW
Vdet
R2
Ndet
R1
Rpd
SW_LC
VDD
P2
LMS

FIG. 6

Level Control Mode	PDFC	LMS	Vdet	PDSW	Link Startup Mode
Automatic mode	L	L	L	H	LSM1
	L	H	H	L	LSM2
Manual mode	H	L	L	H	
	H	H	H	H	

FIG. 7

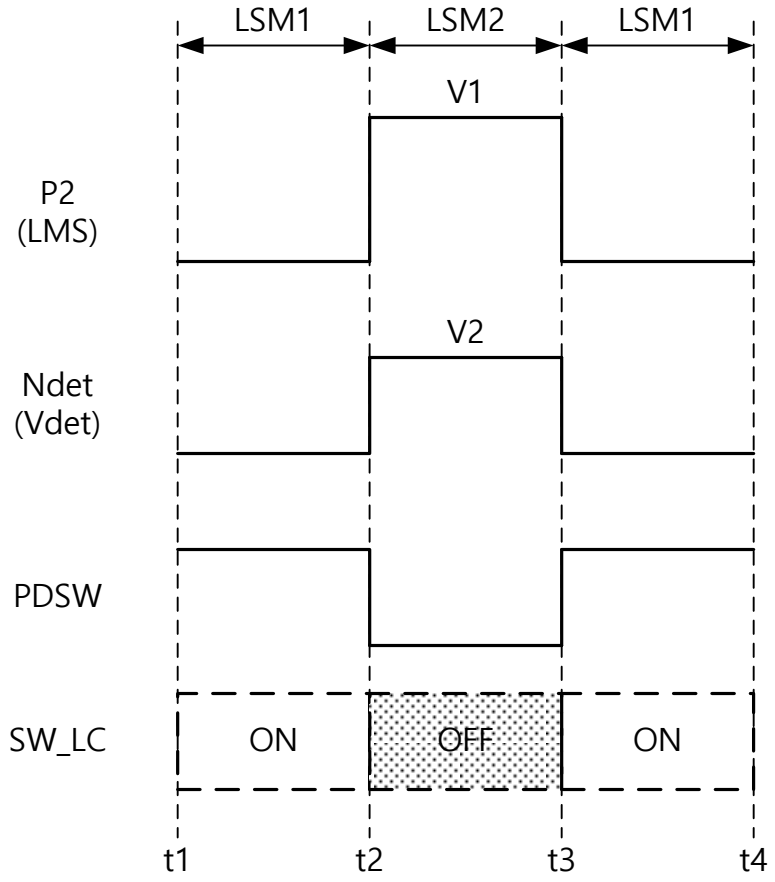

LSM1
LSM2
LSM1
V1
P2
(LMS)
V2
Ndet
(Vdet)
PDSW
SW_LC
ON
OFF
ON
t1
t2
t3
t4

FIG. 8

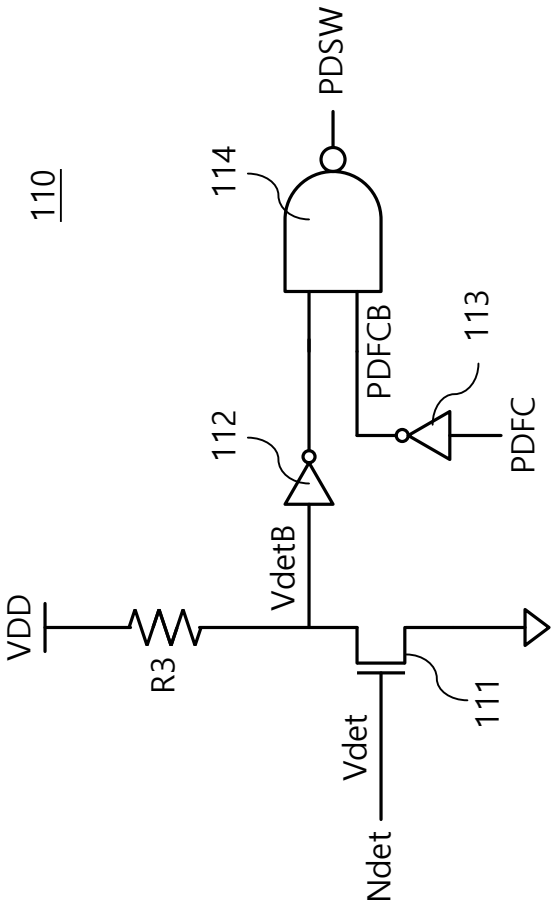


FIG. 9

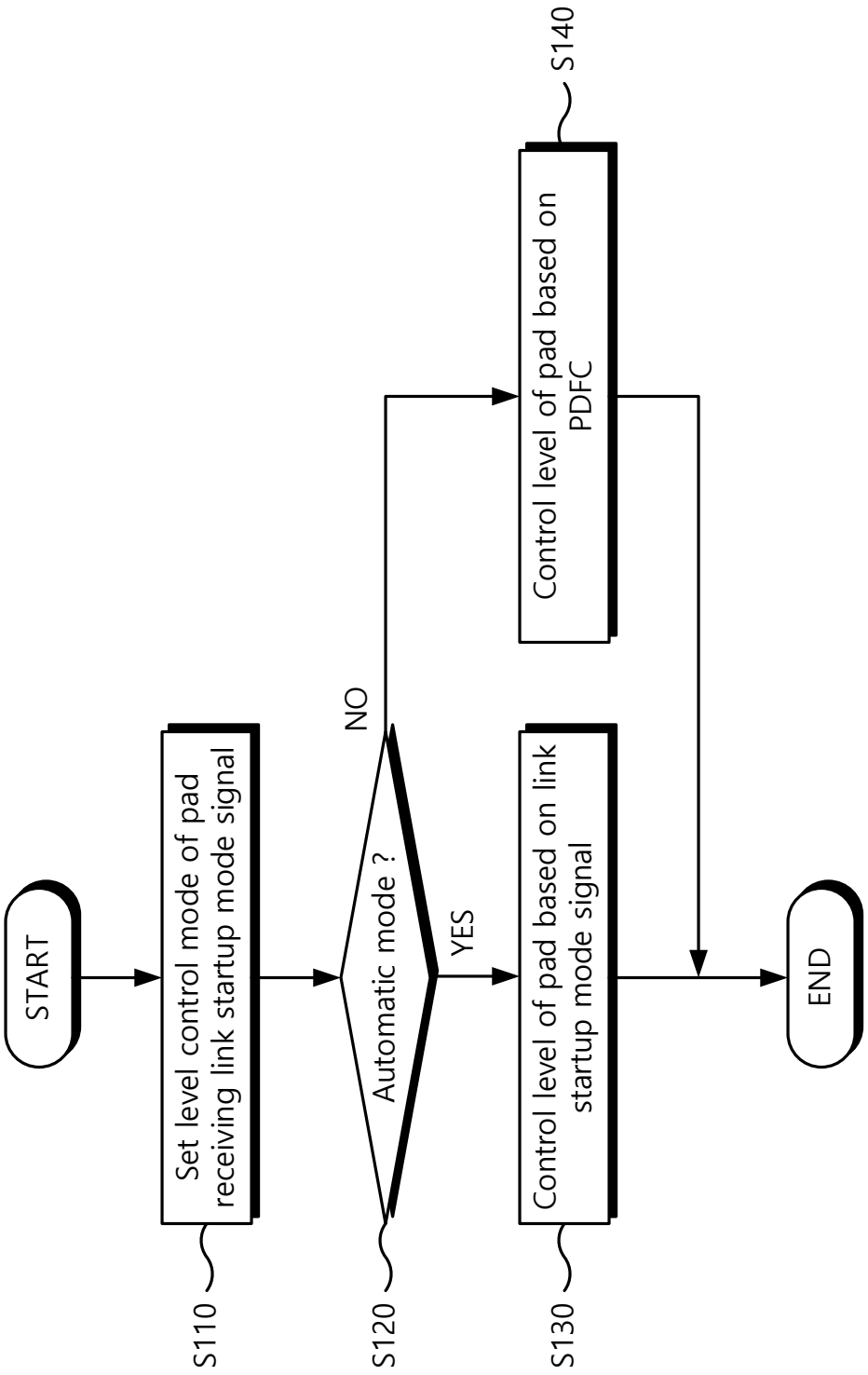

START
Set level control mode of pad receiving link startup mode signal
S110
Automatic mode ?
S120
NO
YES
Control level of pad based on PDFC
S140
Control level of pad based on link startup mode signal
S130
END

FIG. 10

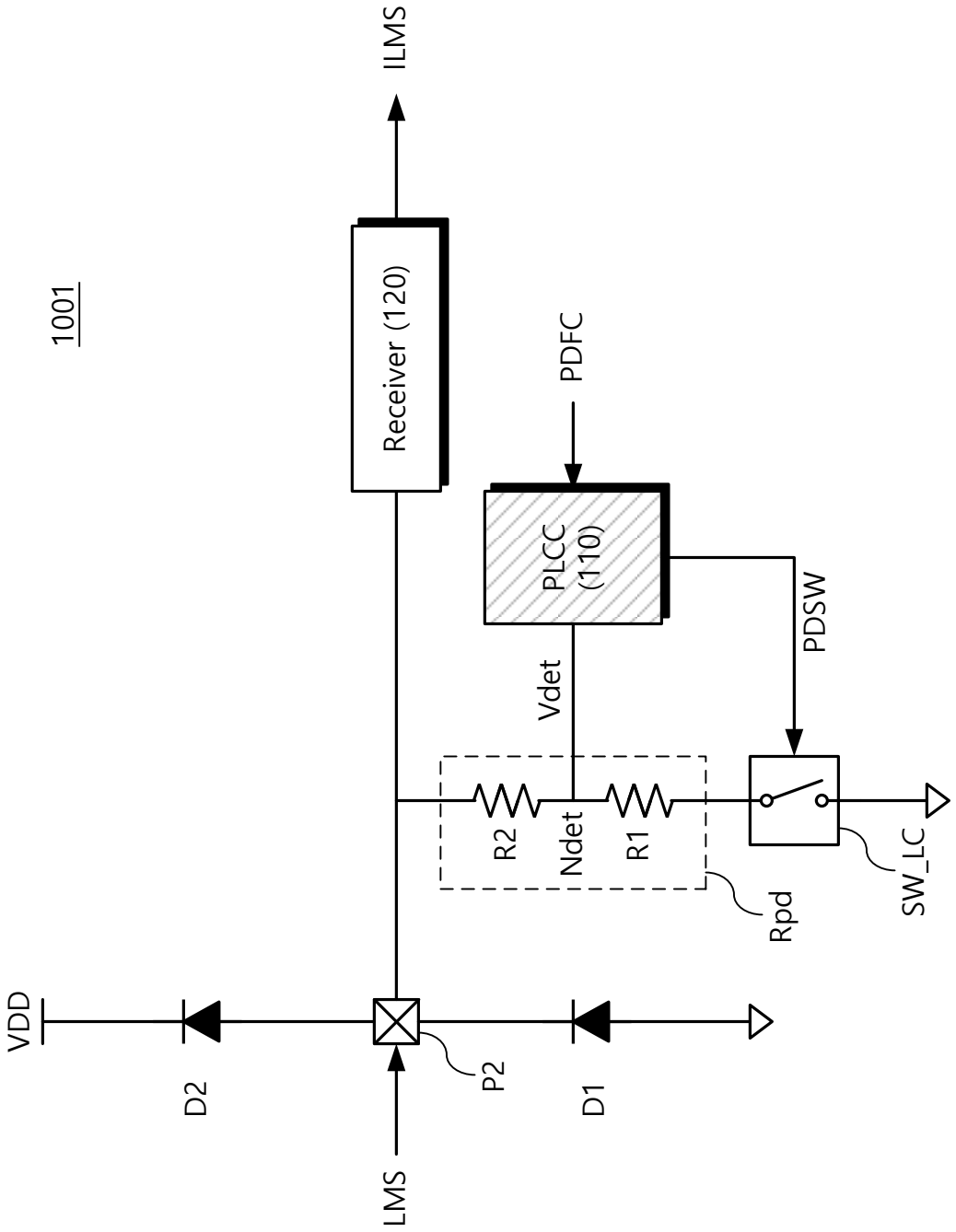

1001
ILMS
Receiver (120)
PDFC
PLCC (110)
PDSW
Vdet
R2
Ndet
R1
Rpd
SW_LC
VDD
D2
P2
D1
LMS

FIG. 11

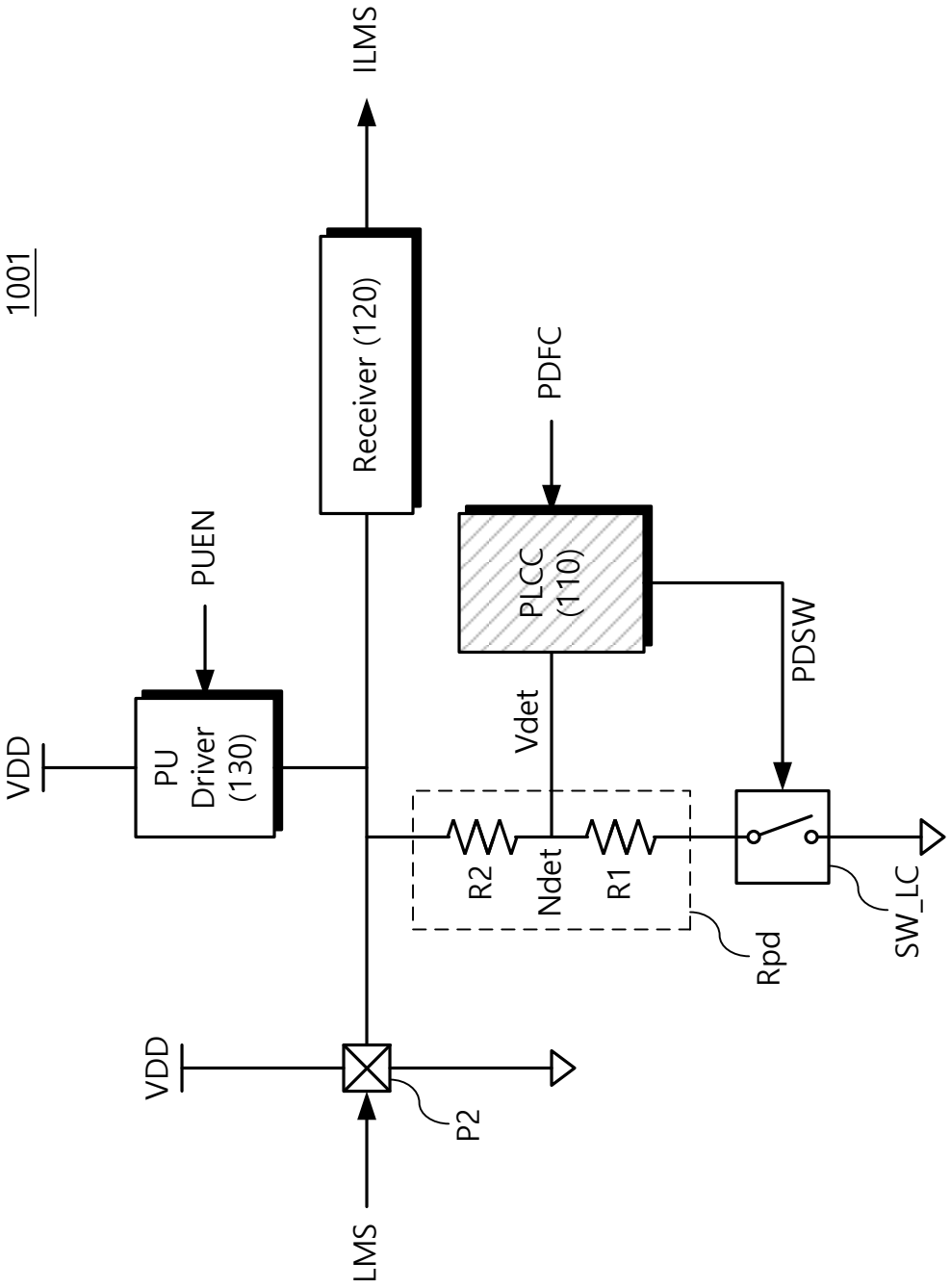
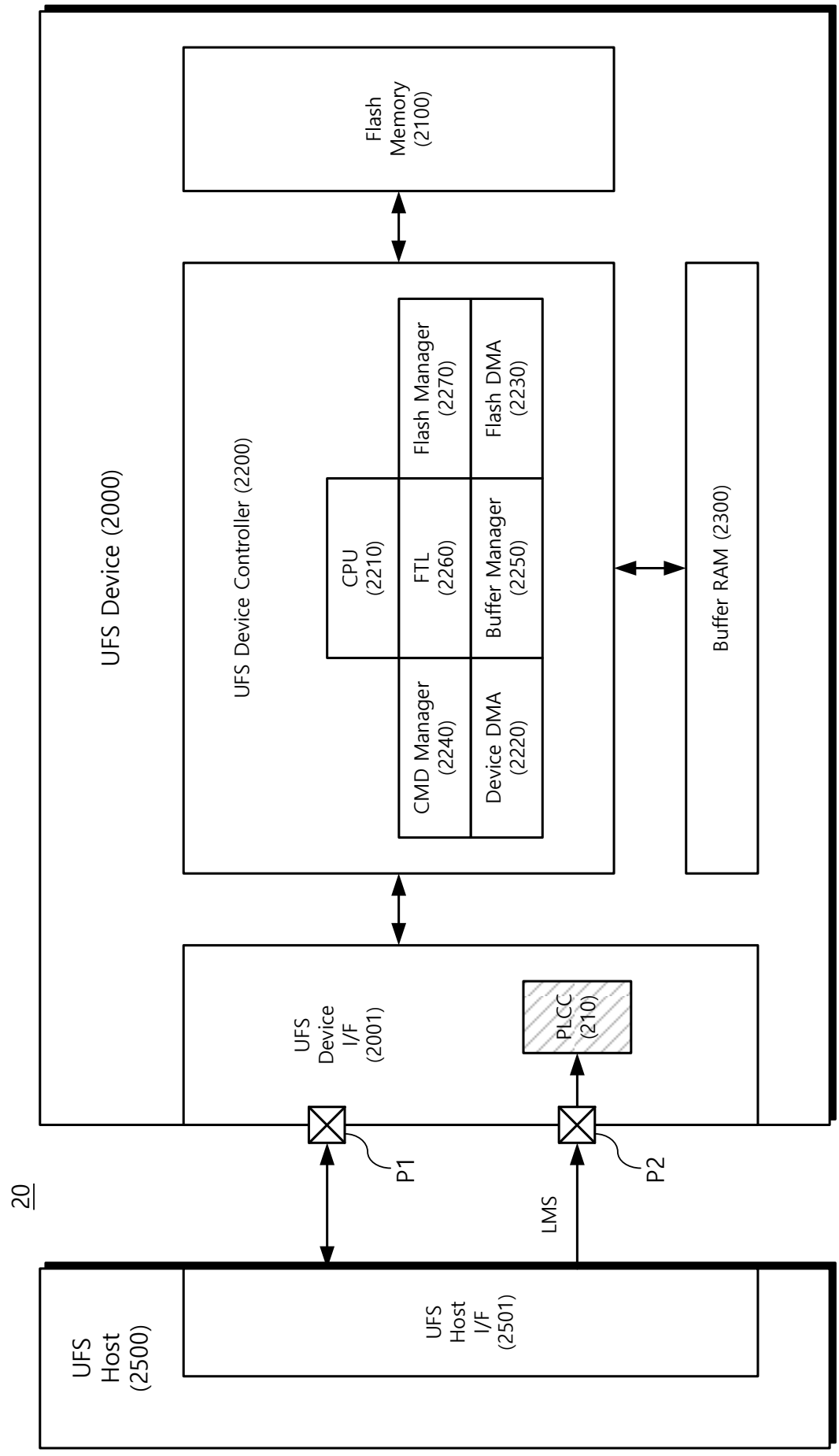

1001
ILMS
Receiver (120)
PDFC
PLCC (110)
PUEN
PU Driver (130)
VDD
Vdet
PDSW
R2
Ndet
R1
Rpd
SW_LC
VDD
P2
LMS

FIG. 12


20
UFS Host (2500)
UFS Host I/F (2501)
LMS
P1
P2
UFS Device (2000)
UFS Device I/F (2001)
PLCC (210)
UFS Device Controller (2200)
CPU (2210)
FTL (2260)
Buffer Manager (2250)
Flash Manager (2270)
Flash DMA (2230)
CMD Manager (2240)
Device DMA (2220)
Buffer RAM (2300)
Flash Memory (2100)