

DATA BUS CONTROL OF NON-BUS CONTROLLABLE VIDEO DISPLAY
DEVICES

This invention relates to a video display, and in particular to the provision of microcomputer control of non-bus controllable display subsystems.

5 An existing NTSC receiver design is controlled by a microcomputer which communicates with various receiver subsystems via a data bus. A particular NTSC receiver is modified to display signals conforming to synchronizing standards other than the NTSC standard. Cost and production considerations may dictate that such a multi-standard video display be engineered for minimal changes to the basic NTSC receiver design.

10 The existing NTSC receiver design may include a multi-function integrated circuit which provides most of the subsystems required in NTSC TV receiver. Such sub-systems include, for example, IF amplification, video demodulation, chrominance demodulation and decoding, audio demodulation, sync separation and pulse and waveform generation etc. The multiple sub-systems of the integrated circuit are controlled by a microcomputer via a data bus. Hence, to facilitate the display signals other than those conforming to the NTSC synchronizing standard the multi-standard circuit design must be controllable by the existing data bus and microcomputer system. Furthermore the multi-standard design must be interfaced to the existing IC sub-subsystems for signal extraction, and must generate compatible output signals for reinsertion into the existing receiver video and synchronizing systems. However, cost and device availability preclude the use of additional bus controllable multi-standard integrated circuits. Thus, an additional requirement of a multi-standard design is the retention of microcomputer controllability without the use of additional data bus controlled devices.

25 A video display has microcomputer control via a data bus and comprises a first sync generator coupled to the data bus for control by data thereon. A second sync generator is without controllable coupling to the data bus. An amplifier is coupled to an inductance for generating a current therein. A means for controlling the second sync generator is coupled to the first sync

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generator and is responsive to a digitally controlled signal therefrom. The second generator output signal is coupled to the amplifier for current generation responsive to the digitally controlled signal.

5 FIGURE 1 shows a simplified block diagram of a TV receiver incorporating an inventive control arrangement.

FIGURE 2 is an electronic schematic drawing showing vertical deflection waveform generation.

10 FIGURE 3 is an electronics schematic drawing showing an inventive embodiment.

FIGURE 4 shows waveforms occurring within the sync generator control circuit of FIGURE 1.

15 FIGURE 1 is a block diagram of a TV receiver employing a microcomputer 200, for control of various sub-systems via a data bus 250. The data bus is connected to an RF tuner 210, and to a multi function NTSC TV receiver integrated circuit IC 100. Integrated circuit 100 provides the following receiver sub-systems, IF amplification, video demodulation 101, video source selection 104, chrominance demodulation and
20 decoding, audio demodulation, sync separation 105 and pulse and waveform generation (110 - 120) etc. In FIGURE 1, IC 100 is depicted with some of the multiple circuit functions provided therein. The data bus 250, is shown illustratively extended within IC 100 to indicate specific circuit functions controlled by data
25 from the microcomputer 200.

Integrated circuit 100 contains a switch 102 which permits selection of video for display. The selection is made by a remote control unit command sent to the microcomputer 200 and then via the data bus 250 to IC 100. Video may originate from
30 outside the receiver, in the form of a base band video input signal or may be received by the RF tuner 220, and input as an IF signal for demodulation by demodulator 101. The selected video source is connected to a sync separator 105 which separates the synchronizing pulses from the selected video signal. The
35 separated sync are coupled to synchronizing generator 110, the separated horizontal sync signal is coupled to a phase detector 111 which controls the frequency of an oscillator 112. The oscillator signal is divided by 32 in a divider 113, to generate a

horizontal rate signal which is applied to the phase detector 111. The horizontal rate signal is also applied to a phase shifter 116 together with a retrace signal RT from the horizontal deflection amplifier 600. The phase shifter output determines the horizontal phase of a horizontal drive signal generator 117. Prior to multi-standard modification output signal CHD, from horizontal drive signal generator 117 was connected to a horizontal deflection amplifier 600, and switch mode run power supply 650. Similarly, prior to modification, a vertical deflection signal is generated and coupled to a vertical deflection amplifier 700. Various other correction waveform signals are generated from the locked oscillator 112 and synchronizing generator 110. A vertical frequency sawtooth shaped signal is generated by generator 114 and is coupled to a squaring circuit 115. Circuit 115 performs a mathematical squaring function that converts the vertical rate sawtooth shaped signal into a parabolic waveform. The parabolic signal is then coupled to the parabolic signal amplifier 120 for control.

Multi-standard operation is facilitated by circuitry of module 400 which is coupled to the chassis and IC 100 via a connector J1. Various signals generated by IC 100 are intercepted and coupled to connector J1, similarly multi-standard deflection signals, generated by the circuitry of module 400, are returned to the main chassis via connector J1. Module 400 comprises a sync pulse generator 450, a vertical deflection waveform generator 410, and an inventive sync generator control 500. A detailed description of module 400 will be given with reference to FIGURES 2 and 3.

Microcomputer 200 receives and transmits data from the bidirectional data bus 250, and in addition control data is received from the remote control receiver 210. Thus virtually all the receiver setup and user operational controls are provided via microcomputer 200 and bidirectional data bus 250. For example, a user may employ remote control 210 to turn the receiver on, in fact the receiver will be switched from a stand-by low power dissipation condition to an operating run condition. The power on command is received by microcomputer 200, processed and transmitted to IC 100 via the data bus 250. The power on

instruction starts oscillator 112 within IC 100, which following a short stabilization period is counted down by divider 113, to produce horizontal drive and vertical deflection signals in conjunction with a sync generator 110. As described earlier
5 prior to multi-standard modification, horizontal drive was coupled to the horizontal deflection amplifier 600. The horizontal deflection amplifier 600, may be considered to be biased in a class C condition where, in the absence of a horizontal drive signal, the amplifier is turned off. Thus, the appearance of horizontal drive
10 from IC 100 causes horizontal deflection amplifier 600, to conduct and generate both deflection current and switching current for a switch mode run power supply 650 which may include a conventional horizontal flyback transformer. Thus, the run power supply 650 starts up and produces power for various
15 supplies which activate the complete receiver.

The run power supply may be shut down by the termination of the horizontal drive signal coupled to horizontal deflection amplifier 600. Run power supply shut down may, for example, be responsive to any of three separate conditions, a user
20 determined off command, an X ray protection shut down, or a microcomputer determined power on reset. These commands are communicated from microcomputer 200 via data bus 250 to IC 100 where they are received, decoded and implemented. As described above, horizontal deflection amplifier 600 operates in a
25 class C mode. However, merely terminating horizontal drive signal may result in the destruction of the amplifier. Thus, responsive to a data bus shut down command, originated from any of the three sources, the horizontal drive signal coupled to the horizontal deflection amplifier, assumes a positive potential. The
30 cessation of horizontal drive and positive potential ensure non-destructive turn off of the deflection amplifier and thus termination of run power supply generation, placing the receiver in a stand by condition.

As described earlier, vertical and horizontal drive
35 signals generated by vertical generator 114 and controlled horizontal drive generator CHD 117 of IC 100 are not used in multi-standard receiver operation. Thus the multiple standard sync pulse generator 450, which generates horizontal drive signals

appropriate to the various standards, must emulate the controlled horizontal drive signal CHD generated by circuit 117. Hence sync pulse generator 450, must be responsive to microcomputer generated data bus communicated commands. However, cost and device availability may preclude the use of a bus controlled multiple standard sync pulse generator.

FIGURE 2 shows in electronic schematic form, the circuitry of vertical deflection waveform generator 410. A ramp signal is generated by charging capacitors C4 and C5 from a selectable constant current source CS50 or CS60. The appropriate source being selected by a control signal generated by control signal 50/60 mode logic 456 responsive to the vertical frequency detector 455, shown in FIGURE 3. The ramp formed across capacitors C4 and C5 is coupled to a buffer amplifier and reset switch 460, within IC U2. The reset switch of 460, is driven with a vertical rate signal, derived from the selected video signal by sync separator 454 of FIGURE 3. Thus, the vertical reset switch 460 rapidly discharges capacitors C4 and C5 forming a ramp signal having the same frequency as the separated vertical sync. The ramp signal is coupled from the buffer amplifier to an amplitude control network which determines vertical raster size. The wiper of the size control R11 is AC coupled via a capacitor C6, to a non-inverting input of an amplifier U1B which is configured as a voltage follower. Vertical centering of the raster is facilitated by a DC potential from a potentiometer R12 connected to the non-inverting input of amplifier U1B. The output ramp signal from amplifier U1B is returned to the main chassis via connector J1 for coupling to vertical deflection amplifier 700. The ramp from the buffer amplifier U2 is also fed back via a resistor R7, to generate a linearizing component to correct the differentiating effects of AC coupling capacitor C6. The vertical ramp signal is "S" corrected by an integrated vertical rate parabolic shaped signal which is coupled to the junction of ramp capacitors C4 and C5. The parabolic shaped signal is amplified by amplifier U1A and coupled via an integrator formed by resistor R6 and the combination of capacitors C4 and C5. The vertical rate parabolic signal is generated by squaring circuit 115 and parabola amplifier 120 of IC100, of FIGURE 1. The parabola is coupled via connector J1 to a

selectively controlled filter and amplitude correction circuit operable in 50 Hz field rates. The filter and amplitude corrector couple the parabolic signal to an input of amplifier U1A.

Synchronizing generator 110, of IC 100, is
 5 synchronized by a horizontal rate signal from divider 113 which is frequency locked to separated horizontal sync from separator 105. Separator 105 is fed selected video from switch 102 of IC 100. However, sync generator 110 and divider 113 function by the count down method, based on divisors determined by the NTSC
 10 standard, thus to provide operation in multiple synchronizing standards requires the use of a second synchronizable multi-standard sync generator. A synchronizable multi-standard sync generator U2, is shown in FIGURE 3, for example IC type TEA 2130. Selected video from switch 102, of IC 100, is coupled via
 15 connector J1 to a capacitor C109 which is connected to pin 19 of sync generator IC U2. The video signal is coupled to sync separator 454, of IC U2, for sync separation. The horizontal sync separator employs a slicing method where sync pulses are detected at a 50 % sync amplitude value determined by a
 20 capacitor C110, connected between pin 18 and ground. The separated horizontal rate pulses are used in a first control loop 453, to synchronize the frequency of a voltage controlled oscillator 451 within IC U2. A ceramic resonator X1 with a resonant
 25 frequency of 32 times the horizontal frequency, approximately 500 KHz, is employed as a reference for oscillator 451. The oscillator signal and is counted down by divider 452, to produce synchronizing signals appropriate to various synchronizing standards. The first control loop 453, has a low pass filter
 30 comprising a capacitor C108 coupled from IC U2 pin 3 to ground and a second capacitor C107 connected from pin 3 to a positive DC potential developed at the junction of a resistive divider formed by resistors R106 and R107. Horizontal retrace pulses RT, from horizontal deflection amplifier 600, are coupled via connector J1 to a high frequency roll off filter formed by a series resistor R24
 35 and a shunt connected capacitor C117. The filtered retrace pulses are applied to pin 13 of IC U2 to provide a horizontal phase reference for a second phase locked loop 485. The second PLL 485, is coupled to a monostable multivibrator 459, which

generates a horizontal drive signal HD, at pin 11 of U2. A 1.3 volt internally generated reference is coupled to the monostable multivibrator 459, which in addition has a timing capacitor connected between pin 10 and ground. The 1.3 volt reference is also coupled to ground via a resistor R112 connected to pin 9. The horizontal drive signal HD, is phase locked to the retrace pulse RT and may be adjusted in horizontal phase by a potentiometer R116. The wiper of potentiometer R116 is coupled via a low pass filter formed by a series resistor R114 and a shunt connected capacitor C113 and applied to pin 14 of U2. Potentiometer R116 develops a positive DC potential which is added to the PLL output signal for coupling to multivibrator 459. Multivibrator 459 generates horizontal drive signal HD, which is coupled via a series connected resistor R113 to the junction of a resistor R115 and a high frequency roll off capacitor C116. The junction of capacitor C116 and resistor R115 is connected via connector J1 to deflection amplifier 600 on the main chassis. At cessation of horizontal drive generation, the HD output signal assumes a positive potential due to the pull-up action of resistor R115 which is coupled to the 12 volt stand by power supply.

The voltage controlled oscillator signal is counted down further by counter 452, to generate timing or gating windows which occur between specific counts, or field line numbers. These gating windows provide enhanced noise immunity for separation of vertical sync pulses from the selected video signal. The separated vertical sync pulses are processed by vertical reset pulse generator 460 to generate a reset pulse which discharges the vertical rate ramp forming capacitors C4 and C5. The reset switch part of generator 460 is depicted in a section of U2 shown in FIGURE 2. The timing windows generated by counter 452 are also employed to for automatic vertical frequency determination. For example, a timing window is generated between line counts of 247 - 277 and coupled to a gate together with separated vertical sync pulses. Vertical sync pulses occurring within the line counted window are thus assumed to be from a field of approximately 262 lines duration which thus has a 60 Hz rate. The repetitively occurrence of vertical sync pulses between line counts of 247 - 277 is indicated to be a 60 Hz field

rate signal which sets 50 / 60 mode control logic 456 to generate an output signal having nominal value of 6 volts. Similarly a vertical sync pulse occurring between line counts of 277 - 361 is assumed to be from an approximately 312 line field which
 5 indicates a 50 Hz field rate and sets the 50 / 60 mode control logic output control signal, to a nominal value of 11 volts. When the selected video signal is absent, for example during tuning, breaks in transmission etc., the vertical frequency gating logic sets the 50 / 60 mode control logic output to nominally zero volts thus
 10 grounding the vertical rate parabola signal at U1A in FIGURE 2.

Although the vertical frequency gating logic can indicate either 50 Hz or 60 Hz vertical frequencies, operation of the sync generator U2 is not limited to these two rates. For example, sync generator U2 may be synchronized, both
 15 horizontally and vertically, with a video signal comprising 655 lines, with a field frequency of 48 Hz.

Integrated circuit sync generator U2 also includes circuitry for sync pulse noise level detection for the detection of VCR replayed video signals to enable automatic selection of time
 20 constants for the first VCO loop. A voltage equal to half the Vcc supply is output at pin 1 and decoupled to ground via a capacitor C100. This voltage is coupled to pin 20, via a resistor R104 and is decoupled to ground at pin 20 by a capacitor C104. The voltage is also coupled to pin 2 via a resistor R108 and is decoupled to
 25 ground at pin 2 by a capacitor C105.

Various other circuitry is included within IC U2 which is not specifically utilized in this multi-standard display use.

As described earlier, the switch mode run power supply 650 is controlled responsive to various on / off commands
 30 processed and transmitted by the microcomputer 200 via the data bus 250. However, horizontal drive generated by multi-standard sync generator U2, has no provision for data bus control. Thus, the microcomputer on / off commands must be communicated to sync generator U2, and control means provided to enable the
 35 multi-standard horizontal drive signal HD to be generally similar to the controllable horizontal drive signal CHD. The two control states of controllable horizontal drive signal CHD must be

emulated to provide control of the run power supply responsive microcomputer commands.

The controllable horizontal drive signal CHD, generated by phase shifter 116 and monostable multivibrator 117 is responsive to on / off commands transmitted via the data bus. Signal CHD is coupled via connector J1 to inventive control circuit 500 of FIGURE 3 where it is coupled via a resistor R100 to the base of a transistor Q100. The emitter of transistor Q100 is connected to ground and the collector is connected to a resistor R101. Resistor R101 is connected to the junction of a capacitor C100 and a resistor R102 connected in series, with the capacitor connected to ground and the resistor connected to a 12 volt stand by power supply. The base of a transistor Q101 is also connected to the junction of capacitor C100 and a resistor R102. The emitter of transistor Q101 is held at a potential of 6.2 volts by a zener diode D100 which is coupled to the 12 volt stand by supply via a resistor R105. Resistors R103 and R104 are connected in series between the 12 volt stand by supply and the collector of transistor Q101. The junction of resistors R103 and R104 is connected to the base of a PNP transistor Q102 which has the emitter connected to the 12 volt stand by supply and the collector connected to the Vcc supply pin 5 of IC U2. The collector of transistor Q102 is decoupled to ground by capacitors C102 and C103.

The controllable horizontal drive signal CHD, has a square waveform shape with a non-symmetrical mark space ratio as illustrated in FIGURE 4 (A). When signal CHD is positive transistor Q100 conducts drawing current from capacitor C100 and the 12 volt standby supply via resistor R102. When signal CHD is low transistor Q100 is turned off allowing capacitor C100 to be charged from the 12 volt supply via resistor R102. Since signal CHD is non-symmetrical, with a longer low level interval, a positive DC potential V100, is established across capacitor C100 and coupled to the base of transistor Q101. The emitter of transistor Q101 is held at 6.2 volts, thus when potential V100 exceeds approximately 6.9 volts, transistor Q101 conducts, drawing current from the 12 volt supply via resistors R104 and R103. The resistors R104 and R103 form a potential divider with

junction connected to the base of PNP transistor Q102. Current flow via resistors R103 and R104 generates a potential across resistor R104 which turns on and saturates the series pass transistor Q102 coupling the 12 volt stand by supply to the provide a Vcc supply for multi-standard sync generator U2. Thus the application of the 12 volt Vcc supply to sync generator U2 causes the internal oscillator 451 to start, and generate the various signals described earlier.

5 In Figure 4 (B) horizontal drive signal CHD, from CHD generator 117 is depicted about time t1. The interval prior to time t1 corresponds to an on or first control condition and the time subsequent to t1 corresponds to a data bus communicated off command. In responsive to the off command, controllable horizontal drive signal CHD assumes a positive potential of approximately 6 volts. This positive DC value is coupled via connector J1 and causes transistor Q100 to conduct discharging potential V100 across capacitor C100 as depicted in FIGURE 4(C). At time interval t2, depicted in FIGURE 4(D), potential V100 has decayed sufficiently for transistor Q101 to turn off and cease current flow in series connected resistors R104 and R103. Hence when transistor Q101 turns off, series pass transistor Q102 is also turned off which terminates the Vcc supply to sync generator U2.

10 After termination of the Vcc supply, operation of sync generator U2 is sustained for approximately 2.75 milliseconds by decoupling capacitor C102. At time interval t3 of FIGURE 4 (E), sync generator U2 ceases operation and the horizontal drive output signal HD assumes a positive potential emulating the second controlled condition of signal CHD. Thus, inventive control circuit 500 controllably couples a signal responsive to data bus commands to the non-data bus controllable multi-standard sync generator U2.



What is claimed is:

1. A video display having microcomputer(200) control via a data bus (250) comprising:

 a first sync generator(IC100) coupled to said data bus (250) for control by data thereon;

 an amplifier (600) coupled to an inductance for generating a current therein;

 a second sync generator (U2) without controllable coupling to said data bus (250); and

 characterized by means (500) for controlling said second sync generator (U2) coupled to said first sync generator(IC100) and responsive to a digitally controlled signal (CHD) therefrom, said second generator (U2) having an output signal (HD) coupled to said amplifier (600) for synchronized current generation in said inductance responsive to said digitally controlled signal (CHD).

2. The display of claim 1, characterized in that said amplifier comprises a deflection amplifier(600).

3. The display of claim 1, characterized in that said amplifier comprises a switched mode power supply (650) type.

4. The display of claim 1, characterized in that said controlling means (500) further comprises a switch (Q100, Q101, Q102) controllably coupled to said digital control signal(CHD) for controlling said second generator(U2).

5. The display of claim 1, characterized in that said digital control signal (CHD) has a first condition and a second condition determined by said microcomputer.

6. The display of claim 1, characterized in that said current is generated and responsive to said first condition.



7. The display of claim 1, characterized in that said current is terminated responsive to said second condition.
8. The display of claim 5, characterized in that said first condition said signal comprises a horizontal frequency signal.
9. The display of claim 5, characterized in that said second condition said signal comprises a DC potential.
10. The display of claim 4, characterized in that said switch (Q100, Q101, Q102) couples a DC power supply (+12VSTDBY) to said second generator(U2) responsive to said first condition.
11. The display of claim 10, characterized in that said switch (Q100, Q101, Q102) terminates said DC power supply (+12VSTDBY) responsive said second condition.
12. The display of claim 2, characterized in that deflection current flow in said amplifier (600) is terminated responsive to second condition.
13. The display of claim 10, characterized in that said second generator (U2) generates a drive signal (HD) responsive to said first condition, said drive signal being generally similar to said controlled signal (CHD) in said first signal condition.
14. The display of claim 10, characterized in that said second generator generates a disabling signal responsive to said second condition, and being generally similar to said controlled signal in said second condition.
15. A video display having a microcomputer (200) for control via a data bus (250) said display comprising:
 - a first sync generator(IC100)being controlled by said data bus (250), said generator generating a signal (CHD) indicative of at least two data bus control conditions;



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a second sync generator (U2) without control by said data bus (250) and generating an output signal (HD);

characterized in that a switch (500) responsive to said indicative signal (CHD), coupled to said second sync generator (U2) to control generation of an output signal (HD) responsive to said control conditions; and

a synchronizable power dissipating load (600) being coupled to said output signal (HD) for synchronization and power generation and dissipation responsive to said data bus control conditions.