METHOD FOR FORMING HIGH QUALITY MULTIPLE THICKNESS OXIDE LAYERS BY REDUCING DESCUM INDUCED DEFECTS

TECHNICAL FIELD

The present invention pertains to the field of integrated circuit devices and manufacturing processes for the same. More particularly, this invention relates to the formation of high quality multiple thickness oxide layers on a silicon wafer substrate.

BACKGROUND ART

Non-volatile memory devices are currently in widespread use in electronic components that require the retention of information when electrical power is terminated. Non-volatile memory devices include read-only-memory (ROM), programmable-read-only memory (PROM), erasable-programmable-read-only memory (EPROM), and electrically-erasable-programmable-read-only-memory (EEPROM) devices. EEPROM devices differ from other non-volatile memory devices in that they can be electrically programmed and erased. Flash EEPROM devices are similar to EEPROM devices in that memory cells can be programmed and erased electrically. However, Flash EEPROM devices enable the erasing of all memory cells in the device using a single electrical current pulse.

High voltage circuit elements such as program and erase transistors are usually formed on a wafer substrate with a relatively thick gate oxide layer. Such relatively thick gate oxide layers are usually required to prevent transistor circuit breakdown in such a high voltage environment. On the other hand, it is preferable that the low voltage circuitry is implemented with relatively thin gate oxide layers on the wafer substrate. Such thin gate oxide layers typically increase the speed of such circuit elements having relatively short gate lengths and thin oxide layers typically provide increased operation speeds.

In addition, as process technologies evolve toward shorter and shorter gate lengths it is desirable to reduce the thickness of the gate oxide layer even further in order to achieve greater operating speed. However, some circuit elements contained on such integrated circuit devices may not be scalable.

Non-volatile memory devices, such as flash EEPROMs require the formation of flash memory cells that include tunnel oxide layers on the wafer substrate. Such tunnel oxide layers may be thinner than high voltage oxide layers on the wafer substrate. However, such tunnel oxide layers usually cannot be scaled down in thickness in the same manner as low voltage oxide layers. Such flash memory cells, for example, typically suffer from significant endurance and data retention problems if the tunnel oxide layers are too thin.

Therefore, non-volatile memory devices can usually benefit from the formation of differing oxide thicknesses on the same wafer substrate. Transistors with relatively thick select gate oxide layers can accommodate high voltage program and erase operations while logic transistors with relatively thin gate oxide layers can yield speed advantages as process technologies evolve toward smaller circuit element dimensions. In addition, the thickness of tunnel oxide layers for flash memory cells can be scaled for reliability independent of the gate dimensions and oxide thickness of the high and low voltage transistors.

One method of forming high quality multiple thickness oxide layers involves multiple masking and oxide formation steps. For example, a first oxide layer, usually the thickest oxide layer, is initially grown on the wafer substrate. Thereafter, a layer of photoresist is formed on the first oxide layer. A pattern is formed

on the photoresist layer by exposing the photoresist through a mask. The photoresist is then developed and removed, leaving a portion of the oxide layer exposed. Subsequently, the first oxide layer is etched and the remaining photoresist is stripped. A second layer of oxide is then grown on the wafer substrate. The second oxide layer forms a thin oxide layer on the wafer substrate while a thicker oxide layer is formed by the combination of the first and second oxide layers. This process can be repeated to form additional oxide layers with various thicknesses throughout the process flow.

During and after development of the photoresist layer, the unmasked or exposed portion of the oxide layer may become contaminated. For example, a thin film, undetectable on visual inspection, may form on the exposed portion of the oxide layer. This film may consist of photoresist residue such as dried developer and undissolved pieces of photoresist. Thus, it is usually necessary to subject the unmasked portion of the oxide layer to a cleaning or descumming process to remove the resist residue. The unmasked or exposed portion of the oxide layer is often descummed or cleaned with O_2, O_2/N_2 or O_2/N_2-H_2 chemistries in a barrel asher or a downstream single wafer asher.

Although the descum process is relatively short in order to avoid any surface damage to the exposed oxide layer, the descum process itself leaves contaminants on the oxide layer. The contaminants appear as dark spots on the oxide layer under a high-resolution scanning electron microscope (SEM) as shown in FIG. 1. An analysis of the dark spots shows that they consist of sulfur compounds and small hydrocarbons, most likely photo active compound, left over from the development of the photoresist. These dark spots or defects on the surface of the exposed oxide layer interact with subsequent processing steps, which creates processing problems and degrades reliability and yield.

For example, when a wet oxide etch is carried out after descum to remove the exposed portion of an oxide layer, the oxide layer under the dark spots cannot be completely removed. Thus, the dark spots act as a micromask on the exposed portion of the oxide layer. As a result of the dark spots, a subsequently grown oxide layer may not be uniform because the initial oxide layer is not completely removed.

Therefore, it would be desirable to have a process for removing these dark spots or defects when forming multiple thickness gate and tunnel oxide layers in order to achieve a higher overall yield of acceptable wafers.

DISCLOSURE OF INVENTION

A method of forming uniform oxide layers by reducing descum induced defects is disclosed. The method comprises reactive ion etching (RIE) a semiconductor substrate, which includes a wafer, an oxide layer on the wafer and a developed photoresist mask on the oxide layer. After reactive ion etching the substrate, the oxide layer is etched.

Other features and advantages of the present invention will be apparent from the detailed description of the invention.

BRIEF DESCRIPTION OF SEVERAL VIEWS OF THE DRAWINGS

FIG. 1 is a photograph of the unwanted dark spots or defects on a wafer substrate after descum;

FIG. 2 is a partial cross-sectional view of an oxide layer formed on a wafer substrate;

FIG. 3 is a partial cross-sectional view of the substrate after the formation of a photoresist layer on the oxide layer;

FIG. 4 is a partial cross-sectional view of the wafer substrate after the photoresist has been developed and the substrate has been descummed;

FIG. 5 is a partial cross-sectional view of the wafer substrate after the oxide layer has been etched;

FIG. 6 is a partial cross-sectional view of the wafer substrate after the photoresist layer has been stripped;

FIG. 7 is a partial cross-sectional view of the wafer substrate after a new layer of oxide has been grown;

FIG. 8 is a partial cross-sectional view of a wafer substrate after the formation of a floating gate on the first and second oxide layers;

FIG. 9 is a partial cross-sectional view of a wafer substrate after formation and development of a photoresist layer and after the substrate has been descummed;

FIG. 10 is a partial cross-sectional view of a wafer substrate after the oxide layers have been etched; and

FIG. 11 is a partial cross-sectional view of the wafer substrate after a third layer of oxide has been grown.

It should be appreciated that for simplicity and clarity of illustration, elements shown in the Figures have not necessarily been drawn to scale. For example, dimensions of some of the elements are exaggerated relative to each other for clarity.

MODES FOR CARRYING OUT THE INVENTION

Referring to FIG. 2, first oxide layer 2, the select gate oxide layer, is formed to overlie the surface of semiconductor substrate 4. Preferably, semiconductor substrate 4 is a single crystal silicon substrate. Semiconductor substrate 4 has an upper surface 6 previously processed to remove debris and native oxides. Preferably, the select gate oxide layer 2 is formed by thermally oxidizing surface 6 at an elevated temperature in the presence of ambient dry oxygen or steam. Preferably, the oxidation process is carried out at a temperature of about 700 to about 1400°C. The oxidation process forms a silicon oxide layer preferably having a thickness of about 50 to about 150 angstroms, and more preferably a thickness of about 90-100 angstroms. The oxidation process may be carried out in a batch-type thermal oxidation furnace.

After forming the first oxide layer 2, the substrate is processed to remove any impurities, and a photoresist layer 8 is formed to overlie the first oxide layer as illustrated in FIG. 3. Preferably, photoresist layer 8 is ultraviolet sensitive and is a positive resist. Selected portions of the photoresist layer 8 are then exposed through a mask. The exposed photoresist is then developed and removed leaving a portion 10 of the oxide layer exposed. The photoresist layer may be developed by methods generally known in the art including but not limited to, immersion, spray and puddle techniques. FIG. 4 illustrates the exposed portion 10 of the oxide layer 2.

After the resist is developed and removed, the exposed portion of the oxide layer 10 is subjected to a low power reactive ion etch to remove any organic residue such as dried developer or undissolved photoresist which may appear on the surface of the oxide layer. Preferably, the reactive ion etch is with RF bias. In order to maintain the integrity of the photoresist layer and ensure pattern quality, the descum process is relatively

short and not more than 30 nm of the photoresist layer and 1nm of the oxide layer are removed. The reaction ion etch process variables are as follows:

(1) Time duration of RIE 3-25 seconds;

(2) O_2/N_2, O_2/N_2-H_2, or O_2/He/Ar chemistries;

(3) RF power level 50-200W;

(4) Pressure 25-300mTorr; and

(5) Wafer temperature 20-60°C.

More specific examples of the RIE process conditions are listed in Table 1 below.

Table 1

Temperature of Wafer (°C)	Power Level (Watts)	Pressure (mTorr)	Chemistry (sccm)	Time of Etch (secs.)
25	200	50	O_2/N_2 200/200	5
40	200	2500	O_2/He/Ar 75/225/100	3
60	50	25	O_2 150	10
60	100	200	O_2/He 180/180	20

It has been discovered that use of a low power reactive ion etch satisfactorily removes any residue left over from the development of the photoresist. However, unlike a down-stream descum process, which is normally used to remove excess dried developer and/or undissolved photoresist. The reactive ion etching process has the advantage of directional etching with the bottom electrode biased, which effectively removes resist residue, but does not leave any dark spots on the exposed portion 10 of the oxide layer. Thus, use of a reactive ion etch eliminates any potential micromasking which occurs when a conventional O_2 descum process is used.

After the reactive ion etching has been completed, the exposed portion of oxide layer 10 is etched or stripped away as illustrated in FIG. 5. The oxide layer may be etched by conventional dry and wet methods that are well known in the art for etching oxide layers. Dry etch methods that can be used to etch the exposed portion of the oxide layer include plasma etching, ion milling etching, and reactive ion etching. Wet etch methods include using hydrofluoric acid. Preferably, a standard buffered oxide etch of hydrofluoric acid, ammonium fluoride and water is used to etch the exposed portion of the oxide layer.

After the exposed portion 10 of the oxide layer 2 is etched, the remaining photoresist 8 is stripped as shown in FIG. 6. Both wet and dry methods that are well-known in the art of semiconductor fabrication can be used to strip the remaining photoresist layer 8. Such methods include but are not limited to use of sulfuric acid and oxidant solutions and conventional O_2 plasma stripping. A new oxide layer 14 is then grown on the wafer substrate 4 as shown in FIG. 7 to produce two oxide layers having different thicknesses. The tunnel oxide layer forms a thin oxide layer while the combination of the select gate oxide layer and the tunnel gate oxide layer form a thicker oxide layer.

The process described above may be repeated to create additional oxide layers with various thicknesses. For example, after growing the tunnel oxide layer 14, a floating gate16 is formed over oxide layers 2 and 14 as shown in FIG. 8. A photoresist layer 18 is then formed to overlie oxide layers 2 and 14 and gate structure 16. As shown in FIG. 9, the photoresist layer 18 is exposed through a mask, and the exposed

photoresist is then developed and removed leaving a portion 15 of oxide layers 2 and 14 exposed. After the resist is developed and removed, the substrate is descummed using reactive ion etching at low power. Then, the exposed portion 15 of oxide layers 2 and 14 is etched away and the remaining photoresist is stripped away as shown in FIG. 10. As illustrated in Figure 11, a third oxide layer 20, the peripheral gate oxide layer, having a thickness different than oxide layers 2 and 14 is grown on the surface of wafer substrate 4.

Thus, there has been disclosed in accordance with the invention a process for fabricating multiple thickness uniform oxide layers in a semiconductor device that fully provides the advantages set forth above. The disclosed method can double the yield of acceptable wafers for further processing. Although the invention has been described and illustrated with reference to specific illustrative embodiments thereof, it is not intended that the invention be limited to those illustrative embodiments. Those skilled in the art will recognize that variations and modifications can be made without departing from the spirit of the invention. It is therefore intended to include within the invention all such variations and modifications that fall within the scope of the appended claims and equivalents thereof.

CLAIMS

1. A method for forming a semiconductor structure, comprising:

reactive ion etching a substrate at a power from 50 to 200W initially to remove organic residue from said substrate, said substrate, comprising:

(a) a wafer (4);

(b) a first oxide layer (2) on the wafer; and

(c) a developed photoresist mask (8) on said first oxide layer, wherein said reactive ion etching to remove organic residue from said substrate causes descum induced defect formation on said substrate;

reactive ion etching said substrate to mitigate descum induced defects on said substrate; and

etching the oxide layer subsequent to reactive ion etching the substrate.

2. The method of claim 1, wherein the oxide layer is etched by plasma etching, ion milling etching, or etching with hydrofluoric acid.

3. The method of claim 1, further comprising stripping the photoresist layer.

4. The method of claim 3, wherein the photoresist is stripped by plasma prepared from a gas comprising O_2, or wet etching with sulphuric acid.

5. The method of claim 3, further comprising growing a second layer of oxide on the substrate.

6. The method of claim 1, wherein the reactive ion etching is carried out with an RF bias for between 3 and 25 seconds.

7. A method of making a semiconductor device comprising:

forming a semiconductor structure by the method of claim 1; and

fabricating a semiconductor device from said semiconductor structure.

8. The method of claim 7, wherein said semiconductor device is a non-volatile memory device.

9. A method of making an electronic device, comprising:
fabricating a semiconductor device by method of claim 8; and
forming an electronic device comprising said semiconductor device.

10. A method of making an electronic device, comprising:
fabricating a semiconductor device by the method of claim 7; and
forming an electronic device comprising said semiconductor device.

11. In a method of fabricating a semiconductor device, including growing an oxide layer over a semiconductor substrate, depositing a layer of photoresist over the oxide layer, exposing and developing the photoresist layer, ashing he substrate to remove any photoresist residue, ashing the substrate to remove any photoresist residue, ashing the substrate to remove descum induced defects formed on the oxide layer;

etching the oxide layer subsequent to ashing the substrate, stripping the remaining photoresist and growing a new oxide layer, the improvement comprising:

reactive ion etching the substrate instead of ashing the substrate.

12. The method of claim 11, wherein the reactive ion etching is carried out with an RF bias for between 3 to 25 seconds.

13. A method of making an electronic device, comprising:
fabricating a semiconductor structure by the method of claim 11; and
forming an electronic device comprising said semiconductor structure.

14. A method for forming a semiconductor structure, comprising:

reactive ion etching a substrate at a power from 50 to 200W to initially remove remaining organic residue from said substrate, said substrate, comprising:

(a) a wafer (4);

(b) a first patterned oxide layer (2) on the wafer;

(c) a second oxide layer on the first oxide layer; and

(d) a developed photoresist mask on the second oxide layer, wherein said reactive ion etching to remove organic residue from said substrate causes descum induced defect formation on said substrate;

reactive ion etching said substrate to mitigate descum induced defects on said substrate;

etching the second oxide layer subsequent to reactive ion etching the substrate;

stripping the photoresist mask; and

growing a third layer of oxide on the substrate.

15. The method of claim 14, wherein the reactive ion etching is carried out with an RF bias for between 3 to 25 seconds.

16. A method of making an electronic device, comprising:

fabricating a semiconductor structure by the method of claim 14; and

forming an electronic device comprising said semiconductor structure.

17. A method of making an electronic device comprising:

fabricating a semiconductor structure by the method of claim 1; and

forming an electronic device comprising said semiconductor structure.

18. A method of forming a semiconductor structure comprising:

(a) providing a semiconductor substrate;

(b) growing a first gate oxide layer on the substrate;

(c) depositing a layer of photoresist over the first gate oxide layer;

(d) exposing and developing the photoresist layer;

(e) reactive ion etching the substrate with RF bias to remove any remaining photoresist residue, wherein said reactive ion etching to remove the remaining photoresist residue from said substrate causes descum induced defect formation on said substrate;

reactive ion etching said substrate to mitigate descum induced defects on said substrate;

(f) etching the first gate oxide layer subsequent to (e) reactive ion etching the substrate;

(g) stripping the remaining photoresist layer;

(h) growing a second gate oxide layer on the wafer substrate;

(i) depositing a layer of photoresist over the second gate oxide layer and the first gate oxide layer;

(j) exposing and developing the photoresist layer;

(k) reactive ion etching the substrate with RF bias to remove any remaining photoresist residue, wherein said reactive ion etching to remove the remaining photoresist residue from said substrate causes descum induced defect formation on said substrate;

reactive ion etching said substrate to mitigate descum induced defects on said substrate;

(l) etching the second gate oxide subsequent to (k) reactive ion etching the substrate;

(m) stripping the remaining photoresist layer; and

(n) growing a tunnel oxide layer on the wafer substrate.

19. A method of forming a semiconductor structure comprising:

providing a semiconductor substrate;

forming a gate oxide layer over the semiconductor substrate;

forming a photoresist layer over the gate oxide layer;

selectively exposing portions of the photoresist layer using a mask;

removing the portions of the photoresist layer leaving a portion of the gate oxide layer;

removing remaining residue from the portion of the gate oxide layer by utilising a reactive ion etch, wherein said reactive ion etching to remove the remaining residue from the gate oxide layer causes descum induced defect formation on the gate oxide layer;

reactive ion etching the gate oxide layer to mitigate descum induced defects on the gate oxide layer;

etching and removing the portion of the gate oxide layer;

removing remaining portions of the photoresist layer; and

forming a second oxide layer over the substrate and the gate oxide layer.