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BIASED, TRIPLE-WELL FULLY DEPLETED SOI STRUCTURE, AND VARIOUS METHODS OF MAKING AND OPERATING SAME

TECHNICAL FIELD

This invention relates generally to semiconductor fabrication technology, and, more particularly, to a biased, triple-well fully depleted SOI structure, and various methods of making and operating same.

BACKGROUND ART

There is a constant drive within the semiconductor industry to increase the operating speed of integrated circuit devices, *e.g.*, microprocessors, memory devices, and the like. This drive is fueled by consumer demands for computers and electronic devices that operate at increasingly greater speeds. This demand for increased speed has resulted in a continual reduction in the size of semiconductor devices, *e.g.*, transistors. That is, many components of a typical field effect transistor (FET), *e.g.*, channel length, junction depths, gate insulation thickness, and the like, are reduced. For example, all other things being equal, the smaller the channel length of the transistor, the faster the transistor will operate. Thus, there is a constant drive to reduce the size, or scale, of the components of a typical transistor to increase the overall speed of the transistor, as well as integrated circuit devices incorporating such transistors.

As transistors are continually scaled in keeping with the requirements of advancing technology, device reliability dictates an associated reduction in the power supply voltage. Hence, every successive technology generation is often accompanied by a reduction in the operating voltage of the transistor. It is known that transistor devices fabricated on silicon-on-insulator (SOI) substrates exhibit better performance at low operating voltages than do transistors of similar dimensions fabricated in bulk silicon substrates. The superior performance of SOI devices at low operating voltage is related to the relatively lower junction capacitances obtained on an SOI device as compared to a bulk silicon device of similar dimensions. The buried oxide layer in an SOI device separates active transistor regions from the bulk silicon substrate, thus reducing junction capacitance.

Figure 1 depicts an example of an illustrative transistor 10 fabricated on an illustrative silicon-on-insulator substrate 11. As shown therein, the SOI substrate 11 is comprised of a bulk substrate 11A, a buried oxide layer 11B, and an active layer 11C. The transistor 10 is comprised of a gate insulation layer 14, a gate electrode 16, sidewall spacers 19, a drain region 18A, and an source region 18B. A plurality of trench isolation regions 17 are formed in the active layer 11C. Also depicted in Figure 1 are a plurality of conductive contacts 20 formed in a layer of insulating material 21. The conductive contacts 20 provide electrical connection to the drain and source regions 18A, 18B. As constructed, the transistor 10 defines a channel region 12 in the active layer 11C beneath the gate insulating layer 14. The bulk substrate 11A is normally doped with an appropriate dopant material, *i.e.*, a P-type dopant such as boron or boron difluoride for NMOS devices, or an N-type dopant such as arsenic or phosphorous for PMOS devices. Typically, the bulk substrate 11A will have a doping concentration level on the order of approximately 10^{15} ions/cm^3. The buried oxide layer 11B may be comprised of silicon dioxide, and it may have a thickness of approximately 200-360 nm (2000-3600 Å). The active layer 11C may be comprised of a doped silicon, and it may have a thickness of approximately 5-30 nm (50-300 Å).

Transistors fabricated in SOI substrates offer several performance advantages over transistors fabricated in bulk silicon substrates. For example, complementary-metal-oxide-semiconductor (CMOS) devices fabricated in SOI substrates are less prone to disabling capacitive coupling, known as latch-up. In addition, transistors fabricated in SOI substrates, in general, have large drive currents and high transconductance values. Also, the

sub-micron SOI transistors have improved immunity to short-channel effects when compared with bulk transistors fabricated to similar dimensions.

Although SOI devices offer performance advantages over bulk silicon devices of similar dimensions, SOI devices share certain performance problems common to all thin-film transistors. For example, the active elements of an SOI transistor are fabricated in the thin-film active layer 11C. Scaling of thin-film transistors to smaller dimensions requires that the thickness of the active layer 11C be reduced. However, as the thickness of the active layer 11C is reduced, the electrical resistance of the active layer 11C correspondingly increases. This can have a negative impact on transistor performance because the fabrication of transistor elements in a conductive body having a high electrical resistance reduces the drive current of the transistor 10. Moreover, as the thickness of the active layer 11C of an SOI device continues to decrease, variations in the threshold voltage (V_T) of the device occur. In short, as the thickness of the active layer 11C decreases, the threshold voltage of the device becomes unstable. As a result, use of such unstable devices in modern integrated circuit devices, *e.g.*, microprocessors, memory devices, logic devices, etc., becomes very difficult if not impossible.

Additionally, off-state leakage currents are always of concern in integrated circuit design, since such currents tend to, among other things, increase power consumption. Such increased power consumption is particularly undesirable in many modern portable consumer devices employing integrated circuits, *e.g.*, portable computers. Lastly, as device dimensions continue to decrease in fully depleted SOI structures, increased short channel effects may occur. That is, in such fully depleted devices, at least some of the field lines of the electric field of the drain 18A tend to couple to the channel region 12 of the transistor 10 through the relatively thick (200-360 nm) buried oxide layer 11B. In some cases, the electric field of the drain 18A may act to, in effect, turn on the transistor 10. Theoretically, such problems may be reduced by reducing the thickness of the buried oxide layer 11B and/or increasing the doping concentration of the bulk substrate 11A. However, such actions, if taken, would tend to increase the junction capacitance between the drain and source regions 18A, 18B and the bulk substrate 11A, thereby negating one of the primary benefits of SOI technology, *i.e.*, reducing such junction capacitance.

The present invention is directed to a device and various methods that may solve, or at least reduce, some or all of the aforementioned problems.

DISCLOSURE OF INVENTION

The present invention is generally directed to a biased, triple-well fully depleted SOI structure, and various methods of making and operating same. In one illustrative embodiment, the device comprises a transistor formed above a silicon-on-insulator substrate comprised of a bulk substrate, a buried insulation layer and an active layer, the bulk substrate being doped with a first type of dopant material, and a first well formed in the bulk substrate, the first well being doped with a second type of dopant material that is of a type opposite the first type of dopant material. The device further comprises a second well formed in the bulk substrate within the first well, the second well being doped with a dopant material that is the same type as the first type of dopant material, the transistor being formed in the active layer above the second well, an electrical contact for the first well and an electrical contact for said second well. In further embodiments, the transistor further comprises a plurality of source/drain regions and a source/drain well is formed in the bulk substrate within the second well under each of the source/drain regions. The source/drain wells are comprised of a dopant material that is of the same type as the first type of dopant material, but the source/drain wells have a dopant concentration level of the first type of

dopant material that is less than a dopant concentration level of the first type of dopant material in the second well.

In one illustrative embodiment, a method of forming a transistor above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, the bulk substrate being doped with a first type of dopant material is disclosed. The method comprises performing a first ion implant process using a second type of dopant material that is of a type opposite the first type of dopant material to form a first well region within the bulk substrate, performing a second ion implant process using a dopant material that is the same type as the first type of dopant material to form a second well region in the bulk substrate within the first well, the transistor being formed in the active layer above the second well, forming a conductive contact to the first well and forming a conductive contact to the second well. In further embodiments, the method further comprises a plurality of source/drain regions and wherein said method further comprises performing a third ion implant process using a dopant material that is of a type opposite the first type of dopant material to result in a source/drain well in the bulk substrate under each of a plurality of source/drain regions of the transistor, the source/drain wells having a dopant concentration level of the first type of dopant material that is less than a dopant concentration level of the first type of dopant material in the second well.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figure 1 is a cross-sectional view of an illustrative prior art semiconductor device formed above an SOI substrate;

Figures 2A-2F are cross-sectional views depicting one illustrative method of the present invention for forming portions of an illustrative NMOS semiconductor device above an SOI substrate; and

Figures 3A-3F are cross-sectional views depicting one illustrative method of the present invention for forming portions of an illustrative PMOS semiconductor device above an SOI substrate.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

MODE(S) FOR CARRYING OUT THE INVENTION

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

The present invention will now be described with reference to the attached figures. Although the various regions and structures of a semiconductor device are depicted in the drawings as having very precise, sharp configurations and profiles, those skilled in the art recognize that, in reality, these regions and structures are not as precise as indicated in the drawings. Additionally, the relative sizes of the various features and doped regions

depicted in the drawings may be exaggerated or reduced as compared to the size of those features or regions on fabricated devices. Nevertheless, the attached drawings are included to describe and explain illustrative examples of the present invention. The words and phrases used herein should be understood and interpreted to have a meaning consistent with the understanding of those words and phrases by those skilled in the relevant art. No special definition of a term or phrase, *i.e.*, a definition that is different from the ordinary and customary meaning as understood by those skilled in the art, is intended to be implied by consistent usage of the term or phrase herein. To the extent that a term or phrase is intended to have a special meaning, *i.e.*, a meaning other than that understood by skilled artisans, such a special definition will be expressly set forth in the specification in a definitional manner that directly and unequivocally provides the special definition for the term or phrase.

In general, the present invention is directed to a biased, triple-well fully depleted SOI structure, and various methods of making and operating same. Although the present invention will be initially disclosed in the context of the formation of an illustrative NMOS transistor, those skilled in the art will understand after a complete reading of the present application that the present invention is not so limited. More particularly, the present invention may be employed with respect to a variety of technologies, *e.g.*, NMOS, PMOS, CMOS, etc., and it may be employed with a variety of different type devices, *e.g.*, memory devices, microprocessors, logic devices, etc.

Figure 2A depicts an illustrative NMOS transistor 32 formed in accordance with one embodiment of the present invention. As shown therein, the transistor 32 is formed above an SOI substrate 30. In one illustrative embodiment, the SOI substrate 30 is comprised of a bulk substrate 30A, a buried insulation layer 30B, and an active layer 30C. Of course, Figure 2A only depicts a small portion of an entire substrate or wafer. In the illustrative embodiment where an NMOS device is formed, the bulk substrate 30A may be doped with a P-type dopant material, *e.g.*, boron, boron difluoride, etc., and it my have a dopant concentration of approximately 10^{15} ions/cm^3. The buried insulation layer 30B may have a thickness that, in one embodiment, varies from approximately 5-50 nm (50-500 Å), and it may be comprised of, for example, silicon dioxide. The active layer 30C may have a thickness that varies from approximately 5-30 nm (50-300 Å), and, in the case of an NMOS device, it may be doped with a P-type dopant material. Those skilled in the art will appreciate that the thickness ranges for the buried insulation layer 30B is significantly less than the corresponding thickness of a buried insulation layer on traditional SOI structures, such as those described in the background section of the application. However, the recited details of the construction of the SOI substrate 30 should not be considered a limitation of the present invention unless such limitations are specifically set forth in the appended claims.

As shown in Figure 2A, the transistor 32 is comprised of a gate insulation layer 36, the gate electrode 34, sidewall spacers 44 and source/drain regions 42. Also depicted in Figure 2A are isolation regions 48 formed in the active layer 30C, a plurality of conductive contacts 46 formed in a layer of insulating material 31, and additional contacts 60, 62 and 63. As will be recognized by those skilled in the art, the contacts 46 provide a means for establishing electrical contact with the source/drain regions 42 of the transistor 32.

According to the present invention, a plurality of doped wells are formed in the bulk substrate 30A. More particularly, as depicted in Figure 2A, for an illustrative CMOS device, the bulk substrate 30A is typically manufactured with a P-type dopant material, such as boron or boron difluoride, at a concentration level of approximately 10^{12}-10^{16} ions/cm^3. A first well 50, a second well 52, a plurality of source/drain wells 54, and a plurality of contact wells 56, 58 are formed in the bulk substrate 30A in accordance with the methods disclosed herein. In the case of an illustrative NMOS transistor, the first well 50 may be doped with an N-type dopant

material, such as arsenic or phosphorous, at a dopant concentration level of approximately 10^{16}-10^{19} ions/cm^3. Again, in the case of an NMOS device, the second well 52 may be doped with a P-type dopant material, *e.g.*, boron or boron difluoride, at a dopant concentration level of approximately 10^{17}-10^{20} ions/cm^3. The source/drain wells 54 may be formed by various counter doping methods to be described more fully herein wherein the resulting concentration of the source/drain wells 54 ranges from approximately 10^{14}-10^{17} ions/cm^3 of a P-type dopant material for an NMOS device. The contact well 56 may be doped with a P-type dopant material at a relatively high concentration, *e.g.*, 2×10^{20} or greater ions/cm^3. Similarly, the N-type contact well 58 may be doped with a similar concentration level of N-type dopant atoms, *e.g.*, arsenic, phosphorous, etc. As will be recognized by those skilled in the art after a complete reading of the present application, the various components of the transistor, *e.g.*, the gate electrode 34 and the gate insulation layer 36, including the manner in which they are made and the materials of construction, are well-known to those skilled in the art and, thus, should not be considered a limitation of the present invention unless such limitations are specifically set forth in the appended claims.

One illustrative method for forming the illustrative NMOS transistor 32 depicted in Figure 2A will now be described with reference to Figures 2B-2F. Initially, as shown in Figure 2B, a masking layer 37 is formed above the active layer 30C of the substrate 30. The masking layer 37 may be comprised of a variety of materials, such as photoresist. Thereafter, an ion implant process 35 may be performed to form the first well 50 in the bulk substrate 30A. The first well 50 may have a depth 50d that varies from approximately 50-150 nm. Again, in the context of the formation of an NMOS device, the ion implant process 35 may be performed using an N-type dopant material, such as arsenic, phosphorous, etc., at a dopant dose of approximately $5e^{10}$-$1.5e^{14}$ ions/cm^2. The resulting first well 50 has a dopant concentration level that ranges from approximately 10^{16}-10^{19} ions/cm^3. The implant energy used during the ion implant process 35 will vary depending upon the species of dopant atoms implanted. In the illustrative embodiment where phosphorous is the dopant material, the implant energy may vary from approximately 20-100 keV.

Next, the masking layer 37 depicted in Figure 2B is removed and another masking layer 41 is formed above the active layer 30C of the substrate 30, as shown in Figure 2C. Thereafter, another ion implant process, as indicated by arrows 39, is performed to form the second well 52 in the bulk substrate 30A. The second well 52 is doped with a second type of dopant material that is a type opposite to that of the dopant material used in the first well 50. In the case of an illustrative NMOS transistor, the second well 52 may be doped with a P-type dopant material, such as boron, boron difluoride, etc. The second well 52 may have a depth 52d that varies from approximately 40-100 nm. In one illustrative embodiment, the second well 52 has a dopant concentration of approximately 10^{17}-10^{20} ions/cm^3. In the context of the formation of an NMOS device, the ion implant process 39 may be performed with a P-type dopant material, *e.g.*, boron, boron difluoride, etc., at a dopant dose of approximately $4e^{11}$-$1e^{15}$ ions/cm^2. The implant energy used during the implant process 39 will vary depending upon the species of the dopant atoms implanted. In the illustrative embodiment where boron is the dopant material, the implant energy may vary from approximately 5-30 keV.

Next, the masking layer 41 depicted in Figure 2C is removed and another masking layer 45 is formed above the substrate 30 as depicted in Figure 2D. As shown therein, an ion implant process, as indicated by arrows 43, is performed to form a contact well 58 for the first well 50. In the illustrative example of an NMOS transistor, the contact well 58 may be doped with an N-type dopant material, such as arsenic or phosphorous, and it may be doped at a relatively high concentration level, *e.g.*, approximately $2e^{20}$ ions/cm^3. This may be

accomplished by using an implant dose of approximately $2e^{15}$-$5e^{15}$ ions/cm^2. As with the other implant processes, the implant energy will vary depending upon the dopant material implanted during the implant process 43. In the illustrative situation where arsenic is implanted during the implant process 43, the implant energy may vary from approximately 10-20 keV.

The masking layer 45 may then be removed and another masking layer 49 may be formed as indicated in Figure 2E. Thereafter, another ion implant process 47 is performed to form contact well 56 in the second well 52. In the case of an illustrative NMOS transistor, the contact well 56 may be comprised of a P-type dopant material, such as boron, boron difluoride, etc. Moreover, the contact well 56 may have a dopant concentration level of approximately $2e^{20}$ ions/cm^3. This may be accomplished by using an implant dose of approximately $2e^{15}$-$5e^{15}$ ions/cm^2. As with the other implant processes, the implant energy will vary depending upon the dopant material implanted during the implant process 43. In the illustrative situation where boron is implanted during the implant process 43, the implant energy may vary from approximately 3-10 keV. As those skilled in the art will recognize after a complete reading of the present application, the contact wells 56, 58 may be formed after the first and second wells have been formed, and they may be formed in either order.

Then, as depicted in Figure 2F, a transistor 32 is formed in the active layer 30C of the substrate 30. The illustrative transistor 32 depicted in Figure 2F is comprised of a gate insulation layer 36, a gate electrode 34, sidewall spacers 40 and source/drain regions 42. A variety of known techniques and materials may be used in forming the various components of the illustrative transistor 32 depicted in Figure 2F. For example, the gate insulation layer 36 may be comprised of silicon dioxide, the gate electrode 34 may be comprised of a doped polysilicon and the sidewall spacers 40 may be comprised of silicon dioxide or silicon nitride. In the case of an illustrative NMOS transistor, the source/drain regions 42 may be doped with an appropriate N-type dopant material, such as arsenic or phosphorous, and they may be formed using traditional extension implants and source/drain implants. Thus, the particular materials and methodologies used in forming the illustrative transistor 32 should not be considered limitations of the present invention unless such limitations are clearly set forth in the appended claims. Moreover, Figure 2F does not depict all of the components of such a transistor. For example, the source/drain regions 42 may have elevated portions (not shown) formed above the active layer 30C, and/or metal silicide regions 42 formed on the source/drain regions 42 and the gate electrode 34. However, such details are not depicted for purposes of clarity.

Next, as shown in Figure 2F, an ion implant process, as indicated by arrows 51, is performed through the masking layer 53 to form source/drain wells 54 in the bulk substrate 30A within the second well 52. The source/drain wells 54 have a depth 54d that may vary from approximately 10-90 nm. At the completion of the implant process, the source/drain wells 54 will be comprised of a dopant material that is the same type as the dopant material used for the second well 54, but the concentration level of dopant material in the source/drain wells 54 will be less than the concentration level of dopant material in the second well 52. In the case of an illustrative NMOS transistor, the source/drain wells 54 may be formed by a counter-doping technique. More particularly, in one embodiment, the source/drain wells 54 may be formed by implanting N-type dopant atoms, *e.g.*, arsenic or phosphorous, at a dopant dose ranging from approximately $4e^{11}$-$1e^{15}$ ions/cm^2 into the P-type doped second well 52. The implant energy for the implant process 51 will vary depending upon the particular dopant species implanted. In the illustrative example where phosphorous is the dopant material, the implant energy for the implant process 51 may vary between approximately 15-90 keV. This will result in the source/drain wells 54 having a P-type dopant concentration of approximately 10^{15}-10^{17} ions/cm^3.

The purpose of the source/drain wells 54 is to reduce the dopant concentration in the bulk substrate 30A in the areas underneath the source/drain regions 42 of the transistor 32 to thereby decrease the junction capacitance of the source/drain regions 42. The implant process 51 used to form the source/drain wells 54 may be performed at any time after the gate electrode 34 of the device is formed. However, typically the implant process 51 will be performed after one or more sidewall spacers 40 are formed adjacent the gate electrode 34. Performing the implant process 51 after the sidewall spacers 40 are formed helps to insure that the bulk substrate 30A in the area under the channel region 44 of the transistor 32 remains at a relatively high dopant concentration level, *e.g.*, approximately the same as that of the second well 52. Moreover, performing the implant process 51 after spacer formation also helps to insure that the source/drain wells 54, having lower dopant concentration levels (as compared to the second well 52), are positioned under the source/drain regions 42 of the transistor 32 and somewhat spaced away from the channel region 44. The dopant concentration level of the source/drain wells 54 should be as low as possible, and the doping level of the wells 54 can be greater than, less than, or equal to the dopant concentration level in the bulk substrate 30A.

Thereafter, the masking layer 53 of Figure 2F is removed and traditional processing techniques may be performed to complete the formation of the transistor 32. For example, as shown in Figure 2A, a layer of insulating material 31 may be formed above the active layer 32 and a plurality of source/drain contacts 46 may be formed to provide electrical connection to the source/drain regions 42. An additional contact 60 may be formed to provide electrical connection to the first well 50, and another contact 62 may be formed to provide electrical connection to the second well 52.

As described herein, some of the various doped regions may be doped with the same type of dopant material, *i.e.*, N-type or P-type. For example, for an illustrative NMOS transistor, the second well 52, the bulk substrate 30A and the source/drain wells 54 are all doped with a P-type dopant material. However, the various doped regions need not be doped with the same species of dopant material, although in some cases they may be. For example, in the case of an NMOS device, the bulk substrate 30A and the second well 52 may be doped using boron difluoride, while the source/drain wells 54 may be doped with boron. Thus, the particular species used in forming the various implant regions depicted herein should not be considered as a limitation of the present invention unless such limitations are expressly recited in the appended claims. Moreover, the various implant regions depicted herein may be subject to standard anneal processes after the implantation processes are performed, or a lower temperature anneal process may be performed in an effort to limit movement of the implanted dopant materials.

The construction of a transistor 32 in accordance with the present invention provides many useful benefits. For example, when the transistor 32 is off, a negative voltage on the order of approximately -0.1 – -2.0 volts may be applied to the second well 52 via contact 62, thereby reducing leakage current when the device 32 is off. Alternatively, when the transistor 32 is on, the second well 52 may be positively biased by applying a voltage of approximately 0.1-1.0 volts via contact 62. By applying this positive bias to the well 52, the drive current of the transistor 32 may be increased, thereby tending to increase overall operating speed of the transistor 32 and integrated circuit incorporating such a transistor. This ability to modulate the same transistor to have low leakage current and high drive current is well-suited for incorporation into low-power, high-performance integrated circuit designs.

Figures 3A-3F depict the present invention in the illustrative embodiment of a PMOS transistor 32 device. In the description of the PMOS device, corresponding reference numbers will be used for similar

components previously described. The PMOS transistor 32 depicted in Figures 3A-3F may be formed by, in general, performing similar implant processes to those described for the NMOS device depicted in Figures 2A-2F using a corresponding opposite type of dopant material. More particularly, the PMOS transistor 32 is comprised of a gate insulation layer 36, the gate electrode 34, sidewall spacers 44 and source/drain regions 43. Also depicted in Figure 3A are isolation regions 48 formed in the active layer 33, a plurality of conductive contacts 46 formed in a layer of insulating material 31, and additional contacts 60 and 62. As depicted in Figure 3A, for an illustrative PMOS device, the bulk substrate 30A may be doped with an N-type dopant material, such as arsenic or phosphorous, at a concentration level of approximately 10^{12}-10^{16} ions/cm^3. A first well 150, a second well 152, source/drain wells 154, and contact wells 156, 158 are formed in the bulk substrate 30A in accordance with the methods disclosed herein. In the case of an illustrative PMOS transistor, the first well 150 may be doped with a P-type dopant material, such as boron or boron difluoride, at a dopant concentration level of approximately 10^{17}-10^{20} ions/cm^3. Again, in the case of a PMOS device, the second well 152 may be doped with an N-type dopant material, *e.g.*, arsenic or phosphorous, at a dopant concentration level of approximately 10^{16}-10^{19} ions/cm^3. The source/drain wells 154 may be formed by various counter doping methods to be described more fully herein wherein the resulting concentration of the source/drain wells 54 ranges from approximately 10^{14}-10^{17} ions/cm^3 of an N-type dopant material for a PMOS device. The contact well 156 may be doped with an N-type dopant material at a relatively high concentration, *e.g.*, 2×10^{20} or greater ions/cm^3. Similarly, the P-type contact well 158 may be doped with a similar concentration level of P-type dopant atoms, *e.g.*, boron, boron difluoride, etc. As will be recognized by those skilled in the art after a complete reading of the present application, the various components of the transistor 32, including the manner in which they are made and the materials of construction, are well-known to those skilled in the art and, thus, should not be considered a limitation of the present invention unless such limitations are specifically set forth in the appended claims.

One illustrative method for forming the illustrative PMOS transistor 32 depicted in Figure 3A will now be described with reference to Figures 3B-3F. Initially, as shown in Figure 3B, a masking layer 137 is formed above the active layer 30C of the substrate 30. Thereafter, an ion implant process 135 may be performed to form the first well 150 in the bulk substrate 30A. The first well 150 may have a depth 150d that varies from approximately 50-150 nm. Again, in the context of the formation of a PMOS device, the ion implant process 135 may be performed using a P-type dopant material, such as boron, boron difluoride, etc., at a dopant dose of approximately $5e^{10}$-$1.5e^{14}$ ions/cm^2. The resulting first well 150 has a dopant concentration level that ranges from approximately 10^{16}-10^{19} ions/cm^3. The implant energy used during the ion implant process 135 will vary depending upon the species of dopant atoms implanted. In the illustrative embodiment where boron is the dopant material, the implant energy may vary from approximately 10-45 keV.

Thereafter, as shown in Figure 3C, another ion implant process, as indicated by arrows 139, is performed through the masking layer 141 to form the second well 152 in the bulk substrate 30A. The second well 152 is doped with a dopant material that is a type opposite to that of the dopant material used in the first well 150. In the case of an illustrative PMOS transistor, the second well 152 may be doped with an N-type dopant material, such as arsenic, phosphorous, etc. The second well 152 may have a depth 152d that varies from approximately 40-100 nm. In one illustrative embodiment, the second well 152 has a dopant concentration of approximately 10^{17}-10^{20} ions/cm^3. In the context of the formation of a PMOS device, the ion implant process 139 may be performed with an N-type dopant material, *e.g.*, arsenic, phosphorous, etc., at a dopant dose of approximately $4e^{11}$-$1e^{15}$ ions/cm^2. The implant energy used during the implant process 139 will vary depending upon the species of the dopant

atoms implanted. In the illustrative embodiment where arsenic is the dopant material, the implant energy may vary from approximately 10-35 keV.

Next, as depicted in Figure 3D, another ion implant process, as indicated by arrows 143, is performed through the masking layer 145 to form a contact well 158 for the first well 150. In the illustrative example of a PMOS transistor, the contact well 158 may be doped with a P-type dopant material, such as boron or boron difluoride, and it may be doped at a relatively high concentration level, *e.g.*, approximately $2e^{20}$ ions/cm^3. This may be accomplished by using an implant dose of approximately $2e^{15}$-$5e^{15}$ ions/cm^2. As with the other implant processes, the implant energy will vary depending upon the dopant material implanted during the implant process 143. In the illustrative situation where boron is implanted during the implant process 143, the implant energy may vary from approximately 3-10 keV.

Thereafter, as shown in Figure 3E, another ion implant process 147 is performed through a masking layer 149 to form contact well 156 in the second well 152. In the case of an illustrative PMOS transistor, the contact well 156 may be comprised of an N-type dopant material, such as arsenic, phosphorous, etc. Moreover, the contact well 156 may have a dopant concentration level of approximately $2e^{20}$ ions/cm^3. This may be accomplished by using an implant dose of approximately $2e^{15}$-$5e^{15}$ ions/cm^2. As with the other implant processes, the implant energy will vary depending upon the dopant material implanted during the implant process 143. In the illustrative situation where arsenic is implanted during the implant process 143, the implant energy may vary from approximately 10-20 keV. As those skilled in the art will recognize after a complete reading of the present application, the contact wells 156, 158 may be formed in either order.

Then, as depicted in Figure 3F, a transistor 32 is formed in the active layer 30C of the substrate 30 using traditional manufacturing techniques and materials. In the case of an illustrative PMOS transistor, the source/drain regions 42 may be doped with an appropriate P-type dopant material, such as boron or boron difluoride, and they may be formed using traditional extension implants and source/drain implants.

Next, as shown in Figure 3F, an ion implant process, as indicated by arrows 151, is performed through the masking layer 153 to form source/drain wells 154 in the bulk substrate 30A within the second well 152. The source/drain wells 154 have a depth 154d that may vary from approximately 10-90 nm. At the completion of the implant process, the source/drain wells 154 will be comprised of a dopant material that is the same type as the dopant material used for the second well 154, but the concentration level of dopant material in the source/drain wells 154 will be less than the concentration level of dopant material in the second well 152. In the case of an illustrative PMOS transistor, the source/drain wells 54 may be formed by a counter-doping technique. More particularly, in one embodiment, the source/drain wells 154 may be formed by implanting P-type dopant atoms, *e.g.*, boron or boron difluoride, at a dopant dose ranging from approximately $4e^{11}$-$1e^{15}$ ions/cm^2 into the N-doped second well 152. The implant energy for the implant process 151 will vary depending upon the particular dopant species implanted. In the illustrative example where boron is the dopant material, the implant energy for the implant process 151 may vary between approximately 10-25 keV. This will result in the source/drain wells 154 having an N-type dopant concentration level of approximately 10^{15}-10^{17} ions/cm^3. Similar to the NMOS device, the implant process 151 used to form the source/drain wells 154 may be performed at any time after the gate electrode 34 of the device is formed. However, typically the implant process 151 will be performed after one or more sidewall spacers 40 are formed adjacent the gate electrode 34. Thereafter, the masking layer 153 of Figure 3F is removed and traditional processing techniques may be performed to complete the formation of the transistor 32.

In this embodiment, when the PMOS transistor 32 is off, a positive voltage on the order of approximately 0.1-2.0 volts may be applied to the second well 152 via contact 162, thereby reducing leakage current when the device 32 is off. Alternatively, when the PMOS transistor 32 is on, the second well 152 may be negatively biased by applying a voltage of approximately -0.1 – -1.0 volts via contact 162. By applying this negative bias to the well 152, the drive current of the PMOS transistor 32 may be increased, thereby tending to increase overall operating speed of the PMOS transistor 32 and integrated circuit incorporating such a transistor.

The present invention is generally directed to a biased, triple-well fully depleted SOI structure, and various methods of making and operating same. In one illustrative embodiment, the device comprises a transistor formed above a silicon-on-insulator substrate comprised of a bulk substrate, a buried insulation layer and an active layer, the bulk substrate being doped with a first type of dopant material, and a first well formed in the bulk substrate, the first well being doped with a second type of dopant material that is of a type opposite the first type of dopant material. The device further comprises a second well formed in the bulk substrate within the first well, the second well being doped with a dopant material that is the same type as the first type of dopant material, the transistor being formed in the active layer above the second well, an electrical contact for the first well and an electrical contact for said second well. In further embodiments, the transistor further comprises a plurality of source/drain regions and a source/drain well is formed in the bulk substrate within the second well under each of the source/drain regions. The source/drain wells are comprised of a dopant material that is of the same type as the first type of dopant material, but the source/drain wells have a dopant concentration level of the first type of dopant material that is less than a dopant concentration level of the first type of dopant material in the second well.

In one illustrative embodiment, a method of forming a transistor above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, the bulk substrate being doped with a first type of dopant material is disclosed. The method comprises performing a first ion implant process using a second type of dopant material that is of a type opposite the first type of dopant material to form a first well region within the bulk substrate, performing a second ion implant process using a dopant material that is the same type as the first type of dopant material to form a second well region in the bulk substrate within the first well, the transistor being formed in the active layer above the second well, forming a conductive contact to the first well and forming a conductive contact to the second well. In further embodiments, the method further comprises a plurality of source/drain regions and wherein said method further comprises performing a third ion implant process using a dopant material that is of a type opposite the first type of dopant material to result in a source/drain well in the bulk substrate under each of a plurality of source/drain regions of the transistor, the source/drain wells having a dopant concentration level of the first type of dopant material that is less than a dopant concentration level of the first type of dopant material in the second well.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

CLAIMS

1. A device, comprising:

a transistor (32) formed above a silicon-on-insulator substrate (30) comprised of a bulk substrate (30A), a buried insulation layer (30B) and an active layer (30C), said bulk substrate (30A) being doped with a first type of dopant material;

a first well (50) formed in said bulk substrate (30A), said first well (50) being doped with a second type of dopant material that is of a type opposite said first type of dopant material;

a second well (52) formed in said bulk substrate (30A) within said first well (50), said second well (52) being doped with a dopant material that is the same type as said first type of dopant material, said transistor (32) being formed in said active layer (30C) above said second well (52);

an electrical contact (60) for said first well (50); and

an electrical contact (62) for said second well (52),

characterized in that said transistor (32) is formed within a part of the active layer (30C) which lies over an area defined by said second well (52) so that, in use, the leakage current and the drive current of the transistor (32) may be modulated by a voltage applied to said electrical contact (62) for said second well (52).

2. A device as claimed in claim 1, further comprising a contact well (58) formed in said bulk substrate (30A) within said first well (50), said contact well (58) being comprised of a dopant material that is of the same type as said second type of dopant material, said contact well (58) within said first well (50) having a dopant concentration level of said second type of dopant material that is greater than a dopant concentration level of said second type of dopant material in said first well (50).

3. A device as claimed in claim 1 or claim 2, further comprising a contact well (56) formed in said bulk substrate (30A) within said second well (52), said contact well (56) being comprised of a dopant material that is of the same type as said first type of dopant material, said contact well (56) within said second well (52) having a

dopant concentration level of said first type of dopant material that is greater than a dopant concentration level of said first type of dopant material in said second well (52).

4. A device as claimed in any one of claims 1 to 3, wherein said transistor (32) further comprises a plurality of source/drain regions (42) and the device further comprises a source/drain well (54) formed in said bulk substrate (30A) within said second well (52) under each of said source/drain regions (42), said source/drain wells (54) being comprised of a dopant material that is of the same type as said first type of dopant material, said source/drain wells (54) having a dopant concentration level of said first type of dopant material that is less than a dopant concentration level of said first type of dopant material in said second well (52).

5. A device as claimed in any one of claims 1 to 4, wherein said bulk substrate (30A) is comprised of silicon, said buried insulation layer (30B) is comprised of silicon dioxide and said active layer (30C) is comprised of silicon.

6. A device as claimed in any one of claims 1 to 5, wherein said bulk substrate (30A) has a dopant concentration level that ranges from approximately 10^{12}-10^{16} ions/cm.

7. A device as claimed in any one of claims 1 to 6, wherein said first well (50) has a dopant concentration level that ranges from approximately 10^{16}-10^{19} ions/cm.

8. A device as claimed in any one of claims 1 to 7, wherein said second well (52) has a dopant concentration level that ranges from approximately 10^{17}-10^{20} ions/cm.

9. A device as claimed in claim 2, wherein said contact well (58) within said first well (50) has a dopant concentration level of approximately $2e^{20}$ ions/cm.

10. A device as claimed in claim 3, wherein said contact well (56) within said second well (52) has a dopant concentration level of approximately $2e^{20}$ ions/cm.

11. A device as claimed in claim 4, wherein said source/drain wells (54) have a dopant concentration level that ranges from approximately 10^{14}-10^{17} ions/cm.

12. A device as claimed in any one of claims 1 to 11, wherein said first well (50) has a depth that ranges from approximately 50-150 nm.

13. A device as claimed in any one of claims 1 to 12, wherein said second well (52) has a depth that ranges from approximately 40-100 nm.

14. A device as claimed in claim 4, wherein said source/drain wells (54) have a depth that ranges from approximately 10-90 nm.

15. A method of forming a device in a silicon-on-insulator substrate (30) comprised of a bulk substrate (30A), a buried insulation layer (30B) and an active layer (30C), said bulk substrate (30A) being doped with a first type of dopant material, the method comprising:

performing a first ion implant process (35) using a dopant material that is of a type opposite said first type of dopant material to form a first well region (50) within the bulk substrate (30A);

performing a second ion implant process (39) using a dopant material that is the same type as said first type of dopant material to form a second well region (52) in said bulk substrate (30A) within said first well (50);

forming a transistor (32) in said active layer (30C) above said second well (52);

forming an electrical contact (60) for said first well (50); and

forming an electrical contact (62) for said second well (52),

characterized in that said transistor (32) is formed within a part of the active layer (30C) which lies over an area defined by said second well (52) so that, in use, the

leakage current and the drive current of the transistor (32) may be modulated by a voltage applied to said electrical contact (62) for said second well (52).

16. A method as claimed in claim 15, wherein said transistor (32) comprises a plurality of source/drain regions (42) and wherein said method further comprises performing a third ion implant process (51) using a dopant material that is of a type opposite said first type of dopant material to result in a source/drain well (54) in said bulk substrate (30A) under each of said source/drain regions (42), said source/drain wells (54) having a dopant concentration level of said first type of dopant material that is less than a dopant concentration level of said first type of dopant material in said second well (52).

17. A method as claimed in claim 16, wherein said transistor (32) further comprises a gate electrode (34) and wherein said third ion implant process (51) is performed after said gate electrode (34) is formed.

18. A method as claimed in claim 16, wherein said transistor (32) further comprises a gate electrode (34) and a sidewall spacer (40) and wherein said third ion implant process (51) is performed after said sidewall spacer (40) is formed.

19. A method as claimed in any one of claims 15 to 18, further comprising performing an additional ion implant process (42) to form a contact well (58) in said bulk substrate (30A) within said first well (50), said additional ion implant process (42) being performed with a second type of dopant material that is of a type opposite said first type of dopant material, said contact well (58) having a dopant concentration level of said second type of dopant material that is greater than a dopant concentration level of said second type of dopant material in said first well (50).

20. A method as claimed in any one of claims 15 to 19, further comprising performing an additional ion implant process (47) to form a contact well (56) in said bulk substrate (30A) within said second well (52), said additional ion implant process

(47) being performed with a dopant material that is of the same type as said first type of dopant material, said contact well (56) having a dopant concentration level of said first type of dopant material that is greater than a dopant concentration level of said first type of dopant material in said second well (52).