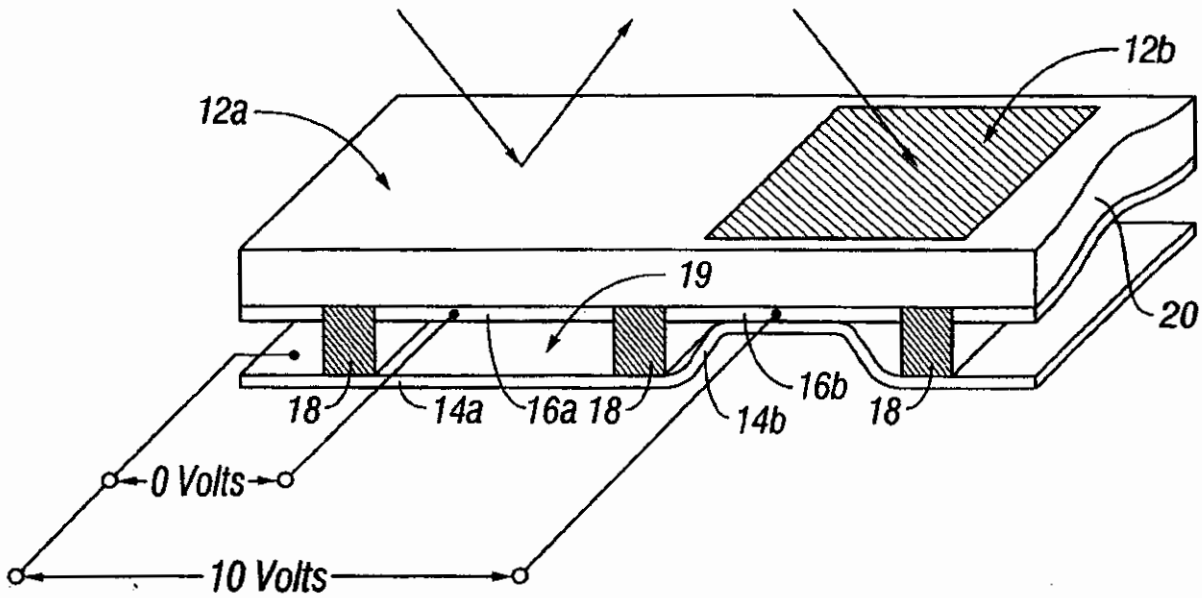

FIG. 1

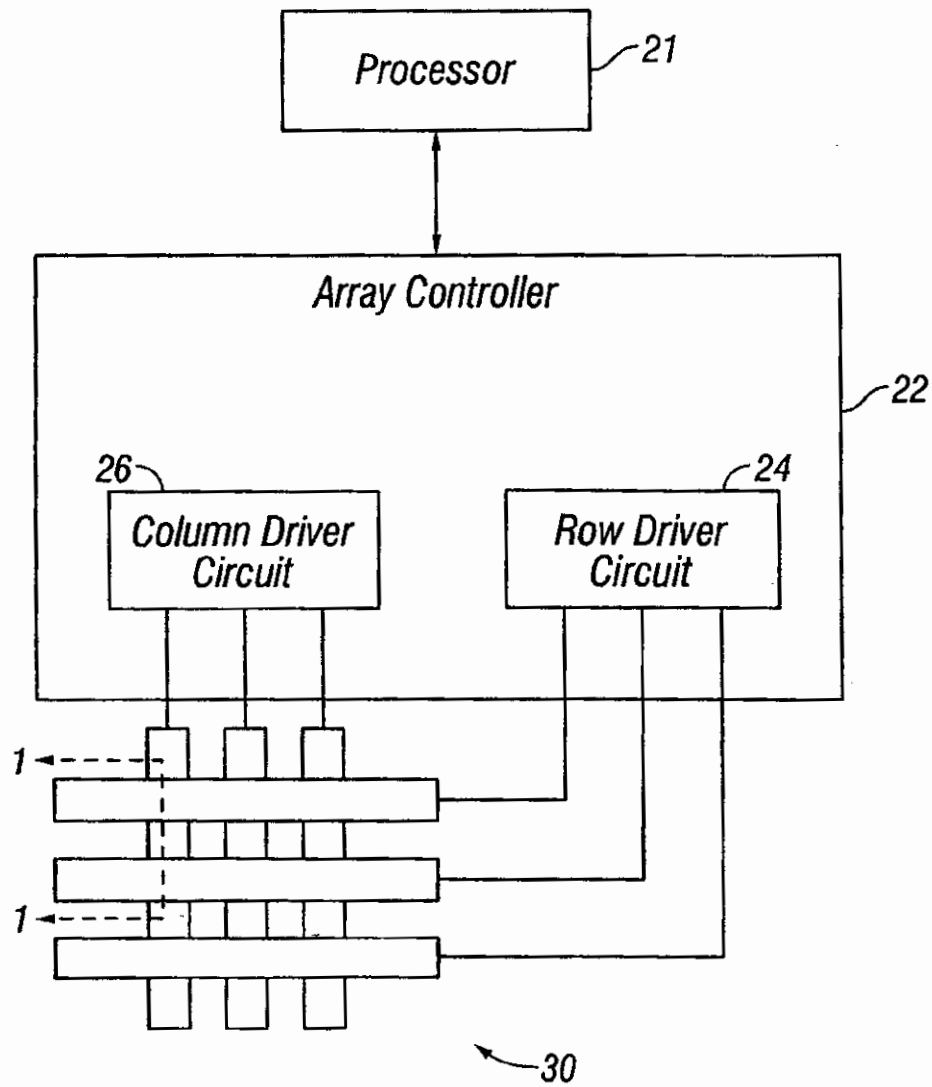
Processor
21
Array Controller
22
26
Column Driver Circuit
24
Row Driver Circuit
1
1
30

FIG. 2

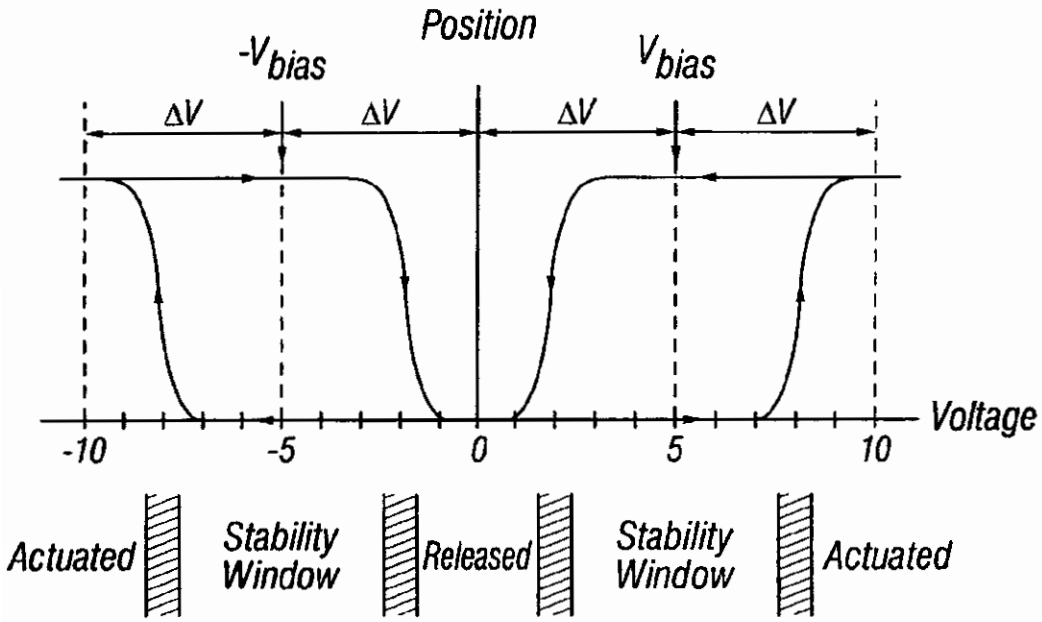

FIG. 3

Row Output Signals	Column Output Signals: $+V_{bias}$	Column Output Signals: $-V_{bias}$
0	Stable	Stable
$+\Delta V$	Release	Actuate
$-\Delta V$	Actuate	Release

FIG. 4

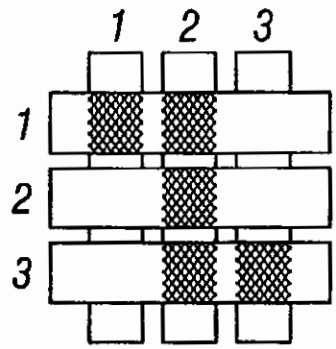
1
2
3
1
2
3

FIG. 5A

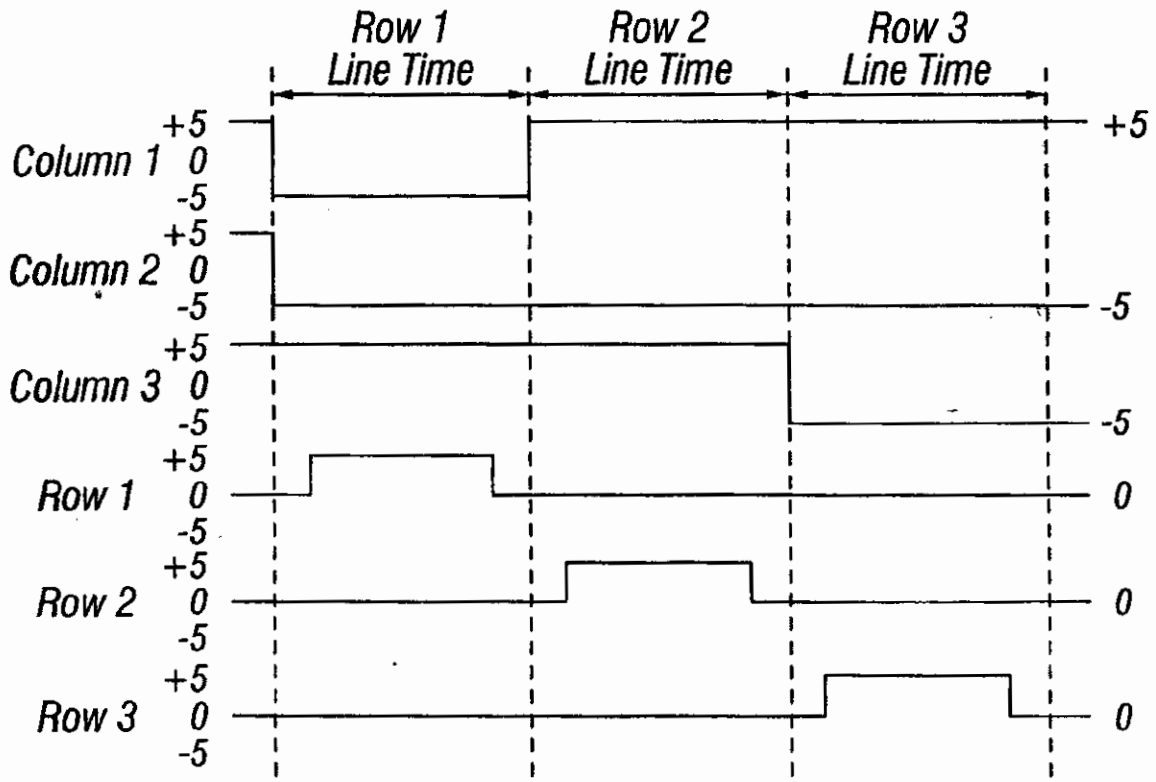
Row 1
Line Time
Row 2
Line Time
Row 3
Line Time
Column 1
Column 2
Column 3
Row 1
Row 2
Row 3
+5
0
-5
+5
-5
-5
0
0
0

FIG. 5B

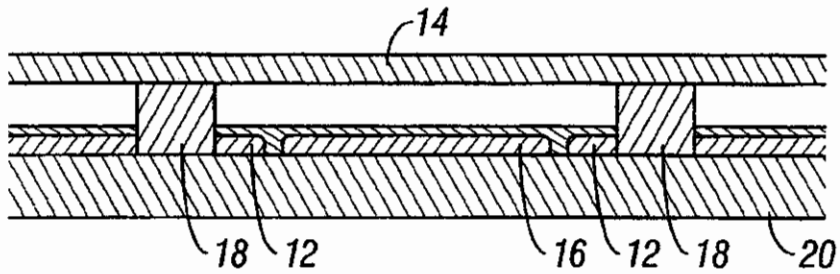

FIG. 6A

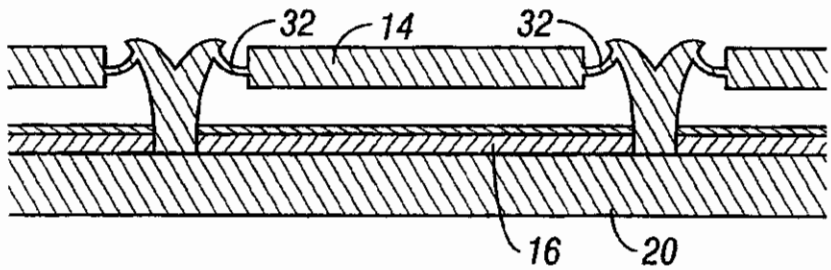

FIG. 6B

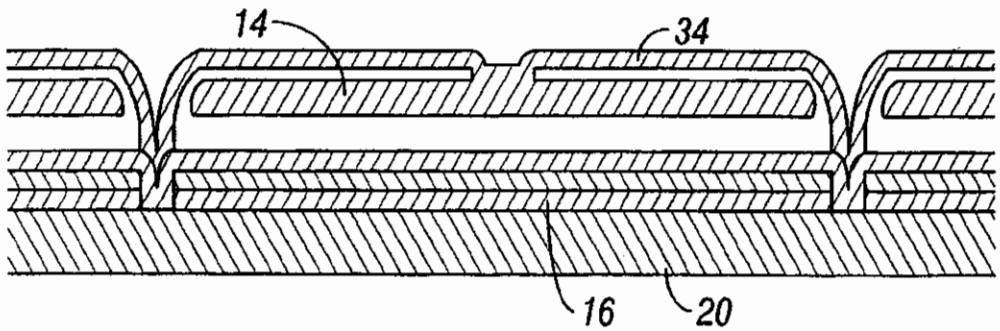

FIG. 6C

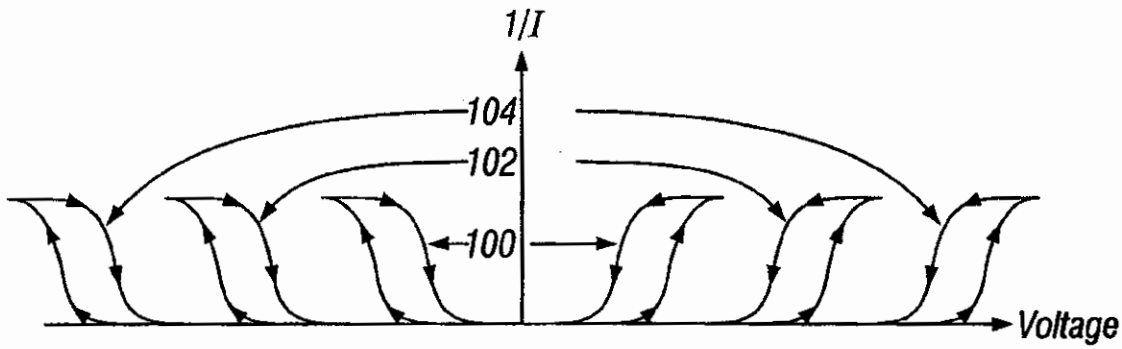

FIG. 7

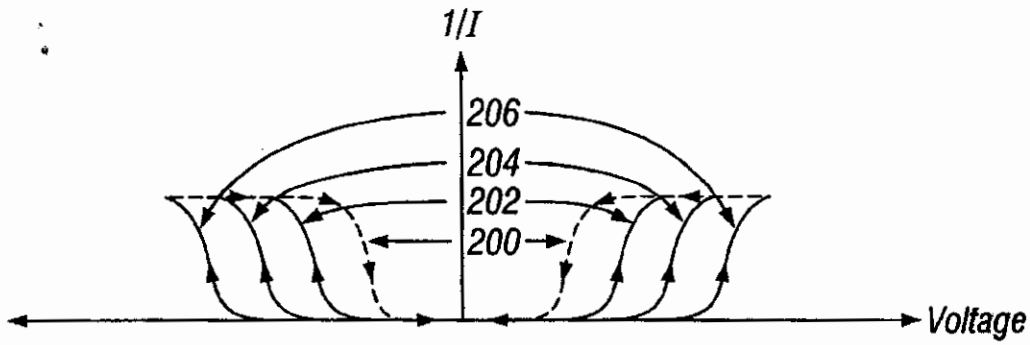

FIG. 8

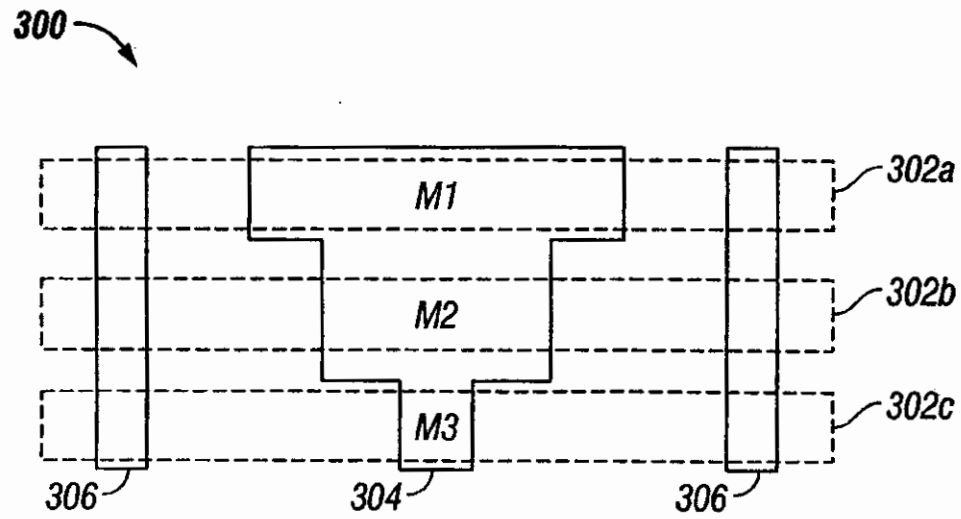
300
M1
M2
M3
302a
302b
302c
306
304
306

FIG. 9A

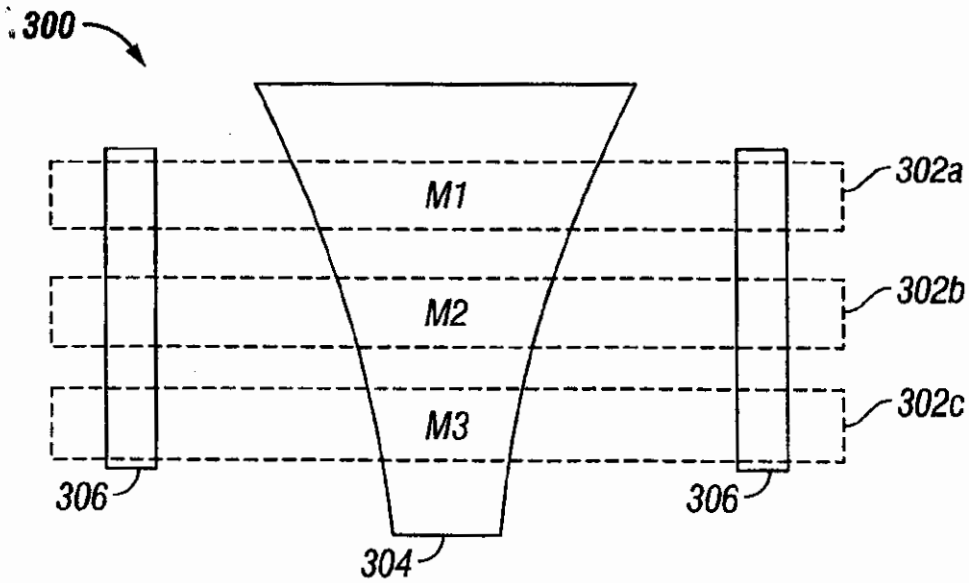
300
M1
M2
M3
302a
302b
302c
306
304
306

FIG. 9B

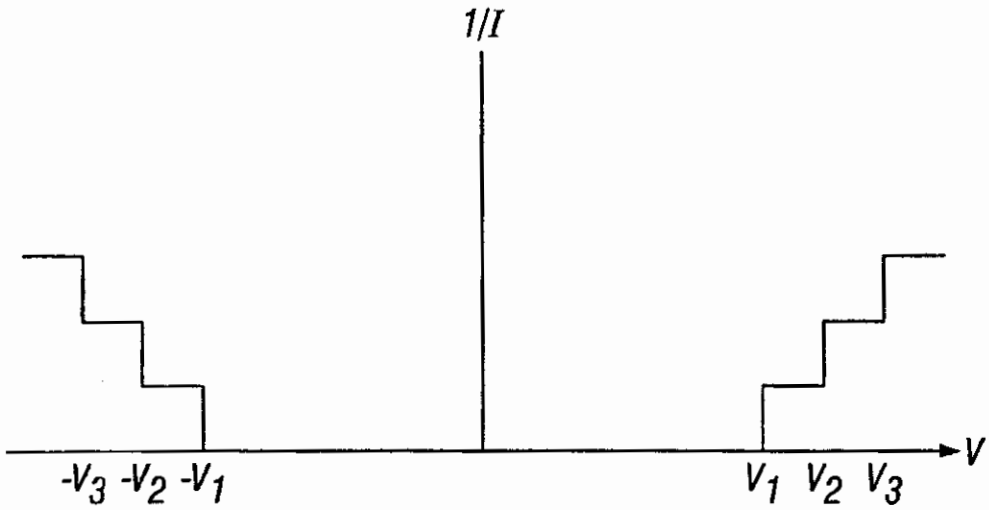
1/I
V
-V3 -V2 -V1
V1 V2 V3

FIG. 10

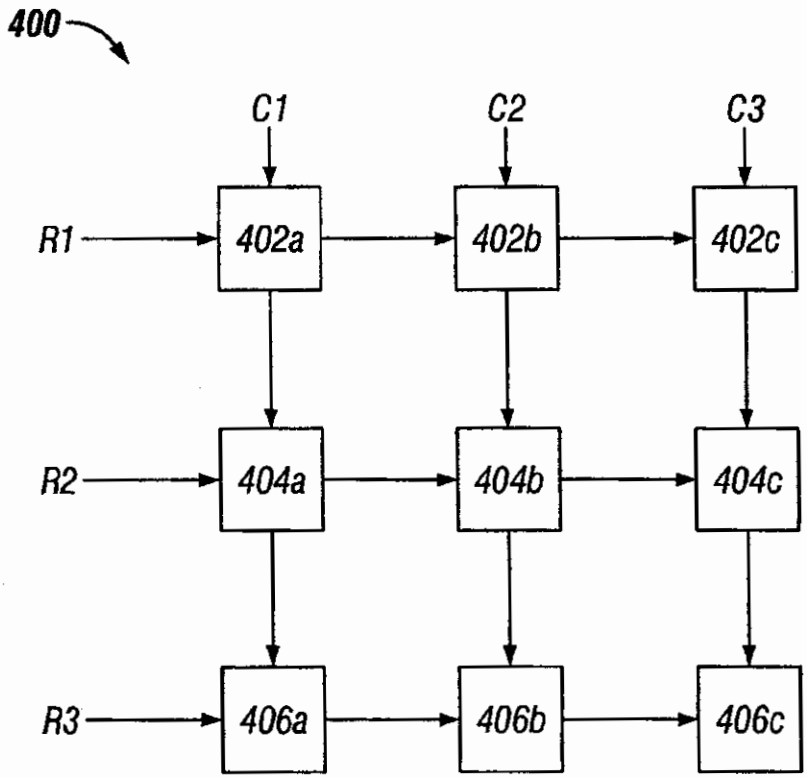
400
C1
C2
C3
R1
402a
402b
402c
R2
404a
404b
404c
R3
406a
406b
406c

FIG. 11

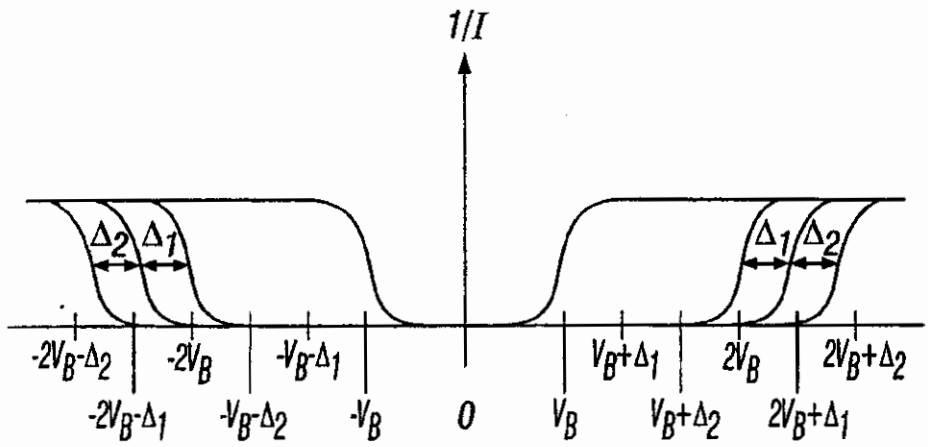

FIG. 12A

V_D \ V_C	$V_B-\Delta_2$	$V_B-\Delta_1$	V_B	V_B	$V_B+\Delta_1$	$V_B+\Delta_2$
$-V_B$	—	—	0	$2V_B$	$2V_B+\Delta_1$	$2V_B+\Delta_2$
ACTUATED	—	—	NONE	M1	M1+M2	M1+M2+M3
0	$-V_B-\Delta_2$	$-V_B-\Delta_1$	$-V_B$	V_B	$V_B+\Delta_1$	$V_B-\Delta_2$
ACTUATED	NONE	NONE	NONE	NONE	NONE	NONE
V_B	$-2V_B-\Delta_2$	$-2V_B-\Delta_1$	$-2V_B$	0	—	—
ACTUATED	M1+M2+M3	M1+M2	M1	NONE	—	—

FIG. 12B

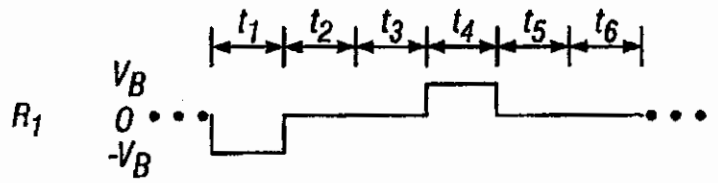

FIG. 13A



FIG. 13B



FIG. 13C

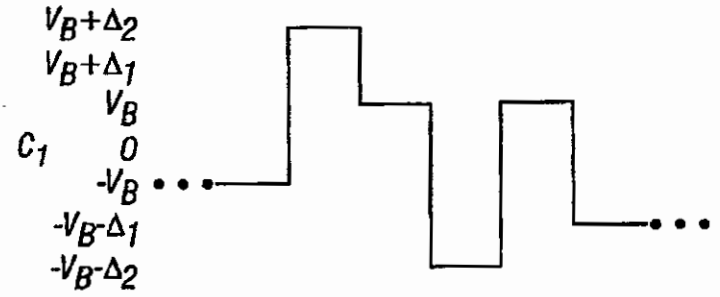

FIG. 13D

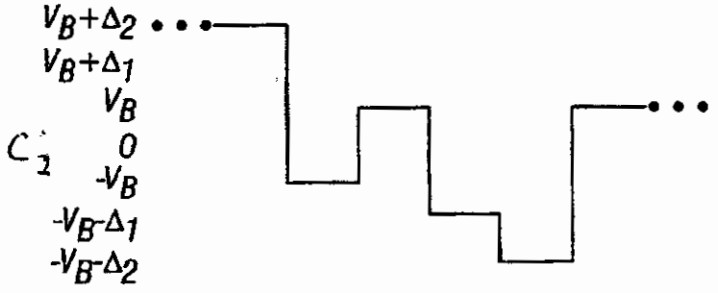

FIG. 13E

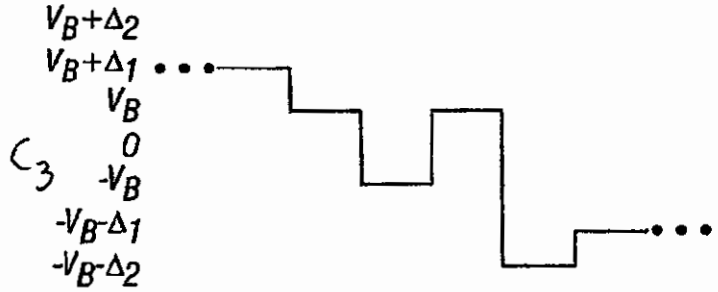

FIG. 13F

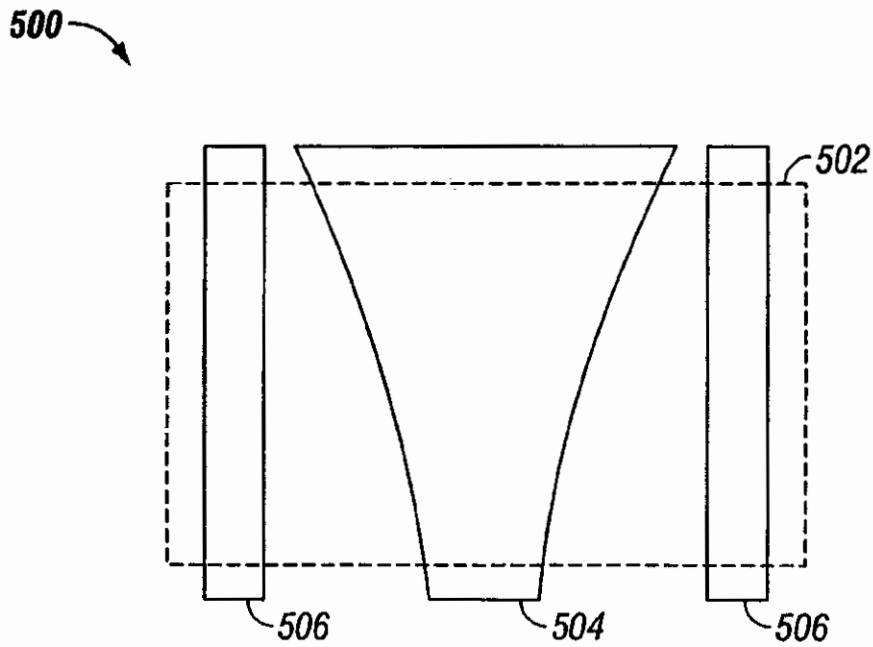

FIG. 14

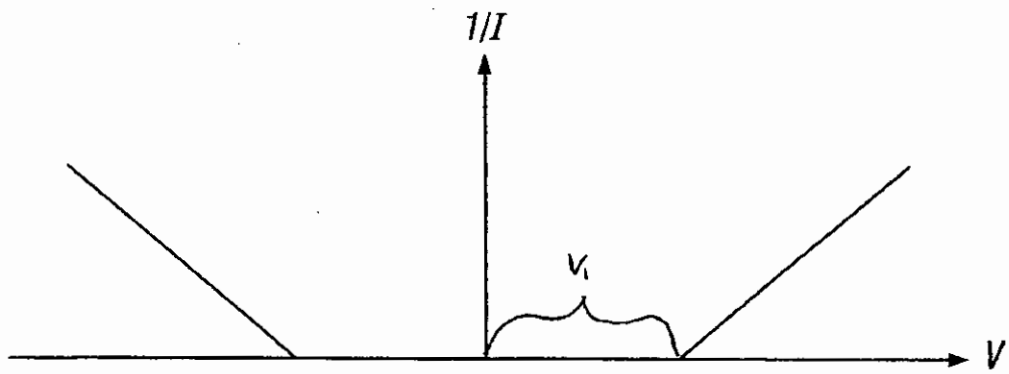

FIG. 15

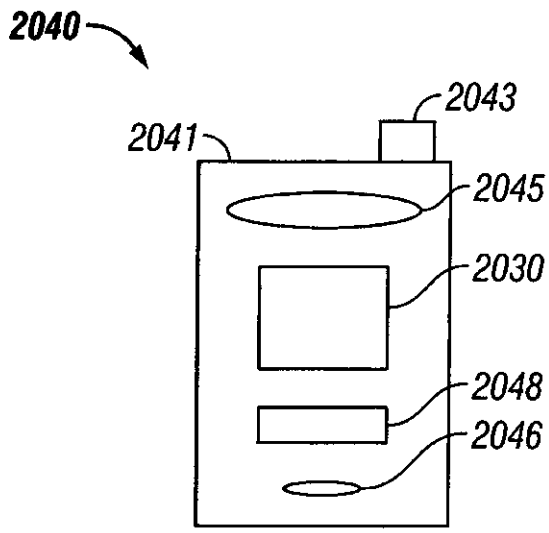

FIG. 16A

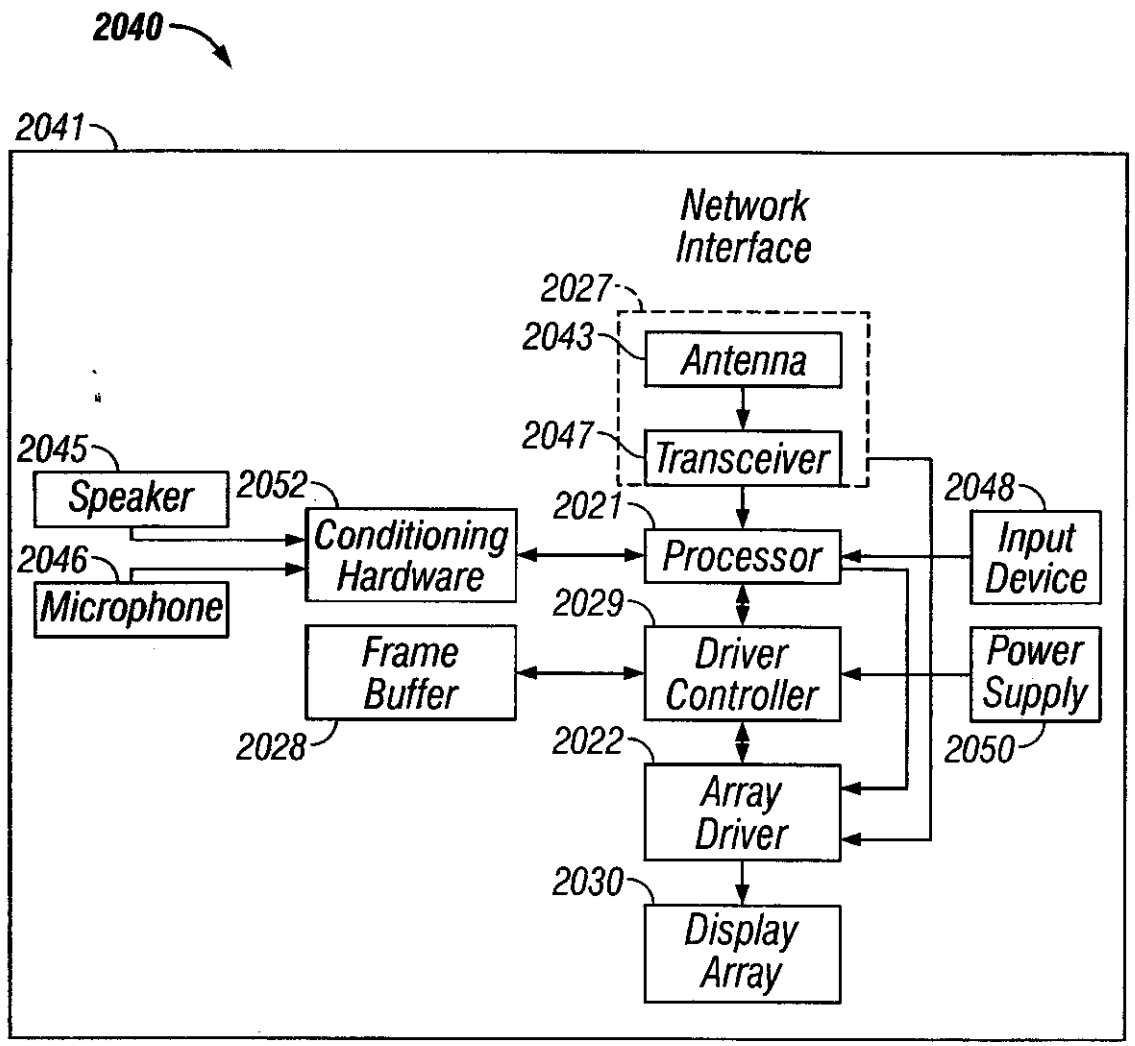

FIG. 16B