Claims

1. A wafer-level package comprising:

a substrate having electrically conductive interconnects embedded within the substrate, the substrate having a top substrate surface and a bottom substrate surface opposite to the top substrate surface, the bottom substrate surface being adapted to be provided on a printed circuit board (PCB);

a first integrated circuit die having an active surface wherein the first integrated circuit die is provided adjacent to an edge portion of a perimeter of the substrate;

a side-filling layer formed between the first integrated circuit die and the edge portion of the perimeter of the substrate to fill a gap between a side edge of the first integrated circuit die and the edge portion of the perimeter of the substrate;

a mold with a portion in contact with the side-filling layer, the mold adapted to hold the first integrated circuit die and the substrate so that the active surface of the first integrated circuit die is in a same plane as the top substrate surface;

a first redistribution layer having electrically conductive interconnects embedded within the first redistribution layer, the first redistribution layer being formed on the active surface of the first integrated circuit die and the top substrate surface; and

a second integrated circuit die provided on the first redistribution layer, the second integrated circuit die being electrically connected to the first integrated circuit die via the first redistribution layer.

2. The wafer-level package of claim 1, further comprising a third integrated circuit die provided on the first redistribution layer, the third integrated circuit die comprising a different type of integrated circuit to that of the first integrated circuit die and the second integrated circuit die.

3. The wafer-level package of claim 2, wherein the second integrated circuit die comprises an application-specific integrated circuit (ASIC) and wherein the first integrated circuit die comprises a photonic integrated circuit (PIC) and the third integrated circuit die comprises an electronic integrated circuit (EIC), or wherein the first integrated circuit die comprises an electronic integrated circuit (EIC) and the third integrated circuit die comprises a photonic integrated circuit (PIC), or wherein the first integrated circuit die comprises a passive chip that provides electrical connections between the second

integrated circuit die and the third integrated circuit die and to the bottom substrate surface.

4. The wafer-level package of claim 2, wherein the third integrated circuit die is configured to overlap with a portion of the first integrated circuit die and a portion of the substrate, or wherein the third integrated circuit die is configured to overlap with only a portion of the first integrated circuit die.

5. The wafer-level package of claim 1, wherein the second integrated circuit die provided on the first redistribution layer is configured to overlap with a portion of the first integrated circuit die.

6. The wafer-level package of claim 1, further comprising a second redistribution layer having electrically conductive interconnects embedded within the second redistribution layer, the second redistribution layer being formed on a bottom side of the wafer-level package comprising the bottom substrate surface, or primary solder bumps formed on the bottom substrate surface.

7. The wafer-level package of claim 6, further comprising secondary solder bumps formed on the second redistribution layer or the primary solder bumps.

8. The wafer-level package of claim 1, further comprising:

a plurality of integrated circuit dice provided adjacent to other edge portions of the perimeter of the substrate, wherein the mold is further adapted to hold the plurality of integrated circuit dice and the substrate so that an active surface of each of the plurality of integrated circuit dice is in the same plane as the top substrate surface.

9. The wafer-level package of claim 8, further comprising:

a plurality of side-filling layers formed between the first integrated circuit die and the edge portion of the perimeter of the substrate and between side edges of the plurality of integrated circuit dice and the other edge portions of the perimeter of the substrate,

wherein the mold is further adapted to hold the first integrated circuit die, the plurality of integrated circuit dice, the plurality of side-filling layers and the substrate so that an active surface of the first integrated circuit die and each of the plurality of integrated circuit dice are in the same plane as the top substrate surface.

10. The wafer-level package of claim 9, further comprising perimeter side-filling layers adapted to formed around other side edges of the first integrated circuit die and other side edges of the plurality of integrated circuit dice.

11. The wafer-level package of claim 10, wherein at least one of the perimeter side-filling layers is adapted to fill a gap between adjacent integrated circuit dice.

12. The wafer-level package of claim 8, wherein each of the first integrated circuit die and the plurality of integrated circuit dice comprises a photonic circuit having one or more optical couplers formed at an outer edge along a perimeter of the wafer-level package.

13. The wafer-level package of claim 12, wherein each of the first integrated circuit die and the plurality of integrated circuit dice further comprises a buffer region formed at the outer edge for protecting the one or more optical couplers from damage.

14. A method for forming a wafer-level package, the method comprising:

(i) providing a substrate having electrically conductive interconnects embedded within the substrate, the substrate having a top substrate surface and a bottom substrate surface opposite to the top substrate surface, the bottom substrate surface being adapted to be provided on a printed circuit board (PCB);

(ii) providing a first integrated circuit die having an active surface adjacent to an edge portion of a perimeter of the substrate;

(iii) providing a side-filling layer formed between the first integrated circuit die and the edge portion of the perimeter of the substrate to fill a gap between a side edge of the first integrated circuit die and the edge portion of the perimeter of the substrate;

(iv) forming a mold with a portion in contact with the side-filling layer, the mold to hold the first integrated circuit die and the substrate so that the active surface of the first integrated circuit die is in a same plane as the top substrate surface;

(v) forming a first redistribution layer having electrically conductive interconnects embedded within the first redistribution layer, the first redistribution layer being formed on the active surface of the first integrated circuit die and the top substrate surface; and

(vi) providing a second integrated circuit die on the first redistribution layer, the second integrated circuit die being electrically connected to the first integrated circuit die via the first redistribution layer.

15. The method of claim 14, further comprising:

providing a plurality of integrated circuit dice adjacent to other edge portions of the perimeter of the substrate,

wherein the step (iv) further comprises forming the mold to hold the plurality of integrated circuit dice and the substrate so that an active surface of each of the plurality of integrated circuit dice is in the same plane as the top substrate surface.

16. The method of claim 15, wherein each of the first integrated circuit die and the plurality of integrated circuit dice comprises a photonic circuit having one or more optical couplers formed at an outer edge along a perimeter of the wafer-level package.

17. The method of claim 16, further comprising: dicing the outer edge of each of the first integrated circuit die and the plurality of integrated circuit dice to expose the one or more optical couplers.

18. The method of claim 14, wherein the step (iv) further comprising:

placing the first integrated circuit die and the substrate on a mold plate, wherein the active surface of the first integrated circuit and the top substrate surface face the mold plate; and

forming the mold to hold the first integrated circuit die and the substrate on the mold plate.

19. The method of claim 18, further comprising: debonding the mold together with the first integrated circuit die and the substrate from the mold plate.