

MULTI-LEVEL DRIVE OF CONTENT ADDRESSABLE MEMORY (CAM) CELLS**1 BACKGROUND**

2 A content-addressable memory (CAM) is a storage structure that accesses stored content
3 or value by content rather than by location. In addition to the writing and reading operations which
4 memory devices such as static random access memory (SRAM) and dynamic random access
5 memory (DRAM) provide, CAM allows parallel search operations based on content stored in
6 CAM cell arrays.

7 Arrays of CAM cells are used for vector-matrix multiplications in AI and ML inference.
8 They allow a bit to be stored while simultaneously performing any Boolean single bit operation
9 (depending on the wiring of the cell). Some AI and ML problems are not amenable to low precision
10 (1 bit) computations and require multi-level encoding of the vector and matrix components.
11 However, if the desired operation of the CAM cells is for a multi-bit value, the conventional
12 approach is to encode the values in unary. The conventional approach requires 2^n CAM cells to
13 store a n -bit value. Consequently, when the CAM cells are formed in a chip, the conventional
14 approach requires a dramatic increase of cell area for multi-bit value.

15 SUMMARY

16 The disclosed invention provides a CAM circuit that enables multi-level computation with
17 a reduced number of CAM cells to both store n -bit values and input n -bit values. The CAM circuit
18 includes a word line driver that incorporates a digital-to-analog converter (DAC), which enables a
19 multi-bit input value to be applied to the CAM cell array, which enables the CAM circuit to
20 compute with n -bit inputs with n CAM cells, instead of 2^n CAM cells required in the conventional
21 approach. The CAM circuit also includes a bit line driver that incorporates digital to analog
22 converters, which enables the CAM circuit to store an n -bit value with n CAM cells, instead of 2^n
23 CAM cells required in the conventional approach. The CAM circuit of the disclosed invention
24 significantly reduces the cell area of a chip for multi-level computations, which leads to cost
25 reduction and/or larger array capacities.

26 These advantages and others are achieved, for example, by a content addressable memory
27 (CAM) circuit. The CAM circuit includes one or more of CAM cells configured to store bit values
28 and at least one word line driver coupled to word lines of the one or more CAM cells and
29 configured to supply output to drive the word lines of the one or more CAM cells. The word line

1 driver includes a first transistor, a second transistor, a current source generating a first current, a
2 third transistor, a first digital-to-analog converter (DAC) coupled to a source of the third transistor
3 and gate of the first transistor, a second DAC coupled to a drain of the third transistor, and an
4 operational amplifier (OpAmp). The drain of the second transistor is coupled to a drain of the first
5 transistor. The source of the second transistor is coupled to the current source and a gate of the
6 first transistor is coupled to the current source. The first transistor, the second transistor and the
7 current source are configured to generate a reference voltage. The OpAmp includes a first input
8 terminal coupled to the drain of the third transistor, a second input terminal coupled to the drain
9 of the second transistor, and an output terminal supplying the output to drive the word lines of the
10 CAM cells.

11 These advantages and others are also achieved, for example, by a content addressable
12 memory (CAM) circuit that includes one or more of CAM cells configured to store bit values and
13 at least one bit line driver coupled to bit lines of the one or more CAM cells and configured to
14 supply output to drive the bit lines of the one or more CAM cells. The bit line driver includes a
15 first transistor, a second transistor, a digital-to-analog converter (DAC) coupled to a source of the
16 second transistor and a gate of the first transistor, and an operational amplifier (OpAmp). The drain
17 of the second transistor is coupled to the drain of the first transistor. The OpAmp includes a first
18 input terminal coupled to the source of the second transistor, an output terminal supplying the
19 output to drive the bit lines of the CAM cells, and a second input terminal coupled to the output
20 terminal.

21 BRIEF DESCRIPTION OF THE DRAWINGS

22 The preferred embodiments described herein and illustrated by the drawings hereinafter
23 are to illustrate and not to limit the invention, where like designations denote like elements.

24 FIG. 1A is a circuit diagram of an inverter in an NMOS process.

25 FIG. 1B is a circuit diagram of an inverter in a CMOS process.

26 FIG. 1C is a circuit diagram of a pseudo-NMOS inverter in a CMOS process.

27 FIG. 1D is a circuit diagram of a pseudo-PMOS inverter in a CMOS process.

28 FIG. 1E is a circuit diagram of a pseudo-PMOS inverter with a variable source bias.

29 FIG. 2 is a circuit diagram of a static-RAM (random access memory) cell using two cross-
30 coupled pseudo-PMOS inverters of FIG. 1E.

FIG. 3 is a circuit diagram of a content addressable memory (CAM) cell of the disclosed invention, based on the pseudo-PMOS inverter of FIG. 1E.

FIG. 4 is a circuit diagram of a word line driver of the disclosed invention, which is configured to drive CAM cells shown in FIG. 3.

FIG. 5 is a circuit diagram of a bit line driver of the disclosed invention, which is configured to drive CAM cells shown in FIG. 3.

FIGS. 6A to 6C show simulation results obtained by using the CAM circuit of the disclosed invention.

FIG. 7A shows an example of achieving multi-bit input capability using unary encoding of the word lines.

FIG. 7B shows an example of achieving multi-bit input capability using binary weighted CAM cells.

FIG. 7C shows an example of achieving multi-bit input capability using of the disclosed invention using the multi-level word line driver circuit.

FIG. 8A shows an example of achieving multi-bit storage capability using unary encoding of the stored state.

FIG. 8B shows an example of achieving multi-bit storage capability using binary weighted CAM cells.

FIG. 8C shows an example of achieving multi-bit storage capability using the multi-level bit line driver of the disclosed invention.

DETAILED DESCRIPTION

The following detailed description is merely exemplary in nature and is not intended to limit the described embodiments or the application and uses of the described embodiments. All of the implementations described below are exemplary implementations provided to enable persons skilled in the art to make or use the embodiments of the disclosure and are not intended to limit the scope of the disclosure, which is defined by the claims. It is also to be understood that the drawings included herewith only provide diagrammatic representations of the presently preferred structures of the present invention and that structures falling within the scope of the present invention may include structures different than those shown in the drawings.

With reference to FIGS. 1A to 1E, shown are various implementations of digital inverters. FIG. 1A illustrates the construction of an inverter in a older NMOS type process. NMOS processes

1 have only n-channel field effect transistor (NFET) transistors **100**, **101**, but provides a depletion-
 2 mode version in addition to the conventional enhancement mode version. The depletion mode
 3 NFET has its gate terminal tied to its source terminal, so that it behaves like a constant current
 4 source. The depletion mode NFET can be used as a load (i.e. a passive pull-up) when constructing
 5 various digital logic gates. Current VLSI fabrication processes are typically CMOS type, wherein
 6 all transistors are enhancement mode, but the process provides both NFET and p-channel field
 7 effect transistor (PFET) devices. FIG. **1B** illustrates a conventional inverter in a CMOS process
 8 including PFET **102** and NFET **103**. CMOS processes have various advantages and disadvantages
 9 relative to NMOS processes. However, one can emulate the NMOS process inverter by using a
 10 PFET with a constant gate bias. FIG. **1C** illustrates this inverter construction including PFET **104**
 11 and NFET **105**, which is referred to as a pseudo-NMOS inverter. Similarly, one can apply a
 12 constant gate bias to the NFET, resulting in the pseudo-PMOS inverter including PFET **106** and
 13 NFET **107** shown in FIG. **1D**.

14 With reference to FIG. **1E**, shown is a pseudo-PMOS inverter wherein the source terminal
 15 of the NFET **109** is not connected to ground (i.e., the negative power supply), but is instead
 16 connected to an arbitrary voltage V_s . If NFET **109** is operated in the subthreshold regime and the
 17 source terminal is connected to the bulk terminal, then the current I_d in NFET **109** will be
 18 exponentially related to the voltages at the gate and source terminals of NFET **109**. That is, $I_D =$
 19 $I_0 e^{\frac{kV_{GS}}{v_t}} = I_0 e^{\frac{kV_G}{v_t}} e^{\frac{-kV_S}{v_t}}$, enabling the multiplication of the gate and source effects. Note that the
 20 current flows only when the input IN signal is low, which turns on PFET **108**, and pulls the output
 21 OUT high. When the input signal IN is high, PFET **108** is off, no current flows, and NFET **109**
 22 pulls the output OUT low.

23 With reference to FIG. **2**, shown is a static random-access memory (RAM) cell, using
 24 cross-coupled pseudo-PMOS inverters including PFET **110**, **112**. The bit lines B and $\bar{B}$ are
 25 connected to the source terminals of NFET **111**, **113** and the word line W is connected to gate
 26 terminals of the NFET **111**, **113**. The state of the RAM cell can be determined by monitoring the
 27 current flow on the bit lines. When the state is 1 (i.e. C is high and $\bar{C}$ is low), current will flow out
 28 of the source terminal of NFET **111** onto bit line B . When the stored state is 0 (i.e. C is low and $\bar{C}$
 29 is high), current will flow out of the source terminal of NFET **113** onto bit line B .

30 With reference to FIG. **3**, shown is a diagram of a content addressable memory (CAM) cell
 31 **300** of the disclosed invention. In an embodiment of the disclosed invention, each CAM cell **300**

1 includes six (6) transistors, among which transistors PFET **301** and **304** are p-channel metal-oxide
2 semiconductor (PMOS) transistors and transistors NFET **302**, **303**, **305** and **306** are n-channel
3 metal-oxide semiconductor (NMOS) transistors.

4 The transistors **301**, **302** and **303** of the CAM cell **300** are configured as pseudo-PMOS
5 inverters with input transistor **301** and dual load transistors **302** and **303**, and transistors **304**, **305**
6 and **306** are also configured as pseudo-PMOS inverters with input transistor **304** and dual load
7 transistors **305** and **306**. As shown in FIG. 3, the gate of PFET **301** is coupled to the drain of PFET
8 **304** and drains of NFETs **305** and **306**. The gate of PFET **304** is coupled to the drain of PFET **301**
9 and drains of NFETs **302** and **303**. Herein, “coupled” means that elements are capable of being
10 electrically connected.

11 When used without the word line driver of the disclosed invention, load transistors NFET
12 **302**, **303**, **305** and **306** are controlled by two mutually exclusive input word lines W **330** and $\overline{W}$
13 **331**. In other words, the first and second word lines **330**, **331** are supplied with or controlled by
14 mutually exclusive word line signals. The gates of NFETs **302** and **305** are coupled to the first
15 word line W **330** and the gates of NFETs **303**, **306** are coupled to the second word line $\overline{W}$ **331**. The
16 sources of NFETs **302**, **303**, **305**, **306** are coupled to four (4) output bit lines B11 **335**, B10 **334**,
17 B01 **333**, B00 **332**.

18 The four (4) output bit lines **332-335** respectively provide outputs representing four
19 possible Boolean AND operations B11, B10, B01 and B00 between the state of the word lines and
20 the CAM cell state: one bit line for each combination of 00, 01, 10 and 11. One output bit line
21 among the output bit lines **332-335**, which carries the unit current, is the one corresponding to the
22 current state of the word line and the cell state. For example, if the word line state and the cell state
23 are both one (1), then the output bit line B11 **335** will have the unit current and the other three will
24 have zero current. If the word line state is one (1) and the cell state is zero (0), the output bit line
25 B01 **333** will have the unit current and the other three will have zero current. If the word line state
26 is zero (0) and the cell state is one (1), the output bit line B10 **334** will have the unit current and
27 the other three will have zero current. If the word line state and the cell state are both zero (0), the
28 output bit line B00 **332** will have the unit current and the other three will have zero current.

29 When used without the word line driver of the disclosed invention, the word lines represent
30 a single bit, and therefore the word lines must be in one of two complementary states. Either W is
31 at a high voltage and $\overline{W}$ is at a low voltage, or W is at a low voltage and $\overline{W}$ is at a high voltage.

1 Furthermore, all the bit lines B00, B01, B10, B11 are at the same voltage. The disclosed invention
2 proposes a novel word line driver allowing the word lines to represent multi-level inputs and a
3 novel bit line driver allowing the stored states to represent multi-bit stored values, such that the
4 currents on the bit lines are the product of the multi-level input and multi-bit stored value.

5 With reference to FIG. 4, shown is a diagram of a word line driver 400 of the disclosed
6 invention, which is used for the CAM circuit 300 shown in FIG. 3. The disclosed invention
7 replaces the normal word line drivers with circuits incorporating digital-to-analog converters
8 (DACs) 351, 352, without altering the design or arrangement of the CAM cells 300.

9 The word line driver 400 of the disclosed invention includes PFET 307, NFETs 308 and
10 309, bias current source I_{bias} 350, DACs 351 and 352, and operational amplifier 353. The drain of
11 PFET 307 is coupled to the drain of the NFET 308, and the source of NFET 308 is coupled to the
12 bias current source I_{bias} 350. The gate of PFET 307 is coupled to the bias current source I_{bias} 350
13 and the first current DAC 351 and the sources of NFETs 308 and 309. The PFET 307, the NFET
14 308 and the bias current source I_{bias} 350 generate a reference voltage V_{ref} , which is the desired bit
15 line voltage for nominal operation.

16 The output of the first current DAC 351 is coupled to the source of NFET 309 and the
17 output of the second current DAC 352 is coupled to the drain of NFET 309. Both current DACs
18 351 and 352 generate the same amount of electrical current to set the current in NFET 309.
19 Operational amplifier 353 has its non-inverting input coupled to the drain of NFET 309 and its
20 inverting input coupled to the drain of NFET 308. The output of operational amplifier 353 drives
21 the gate terminal of NFET 309 and a word line. DACs 351 352 output a current I_{word} that is related
22 to I_{bias} . For example, the output current I_{word} might be an integer multiple of I_{bias} , with the integer
23 being the digital input to the DACs. The purpose of the circuit is to compute a word line voltage
24 which, when applied to the gates of the load transistors in the CAM cell, will produce the same
25 output current I_{word} when the bit lines are at their nominal voltage level V_{ref} . Each word line requires
26 a dedicated word line driver circuit 400.

27 With reference to FIG. 5, shown is a diagram of a bit line driver 500 of the disclosed
28 invention, which is used for the CAM circuit 300 shown in FIG. 3. The bit line driver 500 of the
29 disclosed invention includes PFET 310, NFET 311, DAC 354 and operational amplifier 355. The
30 drain of PFET 310 is coupled to the drain of NFET 311. The source of NFET 311 is coupled to
31 the output of current DAC 354 and the gate of PFET 310. Operational amplifier 355 has its non-

1 inverting input coupled to the source of NFET **311** and its inverting input coupled to its output.
 2 The output of operational amplifier **355** drives a bit line. DAC **354** outputs a current I_{bit} that is
 3 related to I_{bias} . For example, the output current I_{bit} might be an integer multiple of I_{bias} , with the
 4 integer being the digital input to the DAC. The purpose of the circuit is to compute a bit line voltage
 5 which, when applied to the sources of the load transistors in the CAM cell, will produce the same
 6 output current I_{bit} when the word lines are at their nominal voltage level V_{word} . Each bit line requires
 7 a dedicated bit line driver **500**.

8 The computation of the CAM cell output current is as follows. The current in NFET **308**
 9 of FIG. 4 is $I_{bias} = I_0 e^{\frac{kV_{word}}{v_t}} e^{\frac{-kV_{ref}}{v_t}}$, while the current in NFET **309** of FIG. 4 is $I_{word} =$
 10 $I_0 e^{\frac{kV_w}{v_t}} e^{\frac{-kV_{ref}}{v_t}}$ where V_w is the resulting voltage on the word line. The current in NFET **311** of FIG.
 11 **5** is $I_{bit} = I_0 e^{\frac{kV_{word}}{v_t}} e^{\frac{-kV_b}{v_t}}$ where V_b is the resulting voltage on the bit line. Lastly, the current in the
 12 load transistors of the CAM cell is $I_{cam} = I_0 e^{\frac{kV_w}{v_t}} e^{\frac{-kV_b}{v_t}}$. Combining these equations yields $I_{cam} =$
 13 $\frac{I_{word} I_{bit}}{I_{bias}}$. If $I_{word} = N \cdot I_{bias}$, where N is the digital input to current DACs **351** and **352**, and $I_{bit} =$
 14 $M \cdot I_{bias}$, where M is the digital input to current DAC **354**, then $I_{cam} = N \cdot M \cdot I_{bias}$.

15 With reference to FIGS. **6A** to **6C**, shown are simulation results for the combination of the
 16 word line driver circuit **400** and bit line driver circuit **500** with a bias current I_{bias} is set to 1nA. In
 17 FIG. **6A**, the horizontal axis is the word line current I_{word} that is swept from 1nA to 10nA. The
 18 vertical axis is output current I_{cam} of the CAM cell. The bit line current I_{bit} is stepped from 1nA to
 19 10nA. The product therefore ranges from 1nA to 100nA. In FIG. **6B**, an example simulation of the
 20 word line voltage from the word line driver circuit is shown as a function of the word line current
 21 I_{word} , that is swept from 1nA to 10nA. In FIG. **6C**, an example simulation of the bit line voltage
 22 from the bit line drive circuit is shown as a function of the bit line current I_{bit} , that is swept from
 23 1nA to 10nA.

24 With reference to FIGS. **7A** to **7C**, shown are various CAM cell topologies for achieving
 25 multi-bit inputs on the word lines. In FIG. **7A**, three CAM cell are used, wherein each CAM cell
 26 stores the same bit, but the 2-bit word line value is encoded in unary. That is, if the input value is
 27 1, only one of W_0 , W_1 and W_2 will be at a high voltage (typically W_0). If the input value is two
 28 (2), only two of W_0 , W_1 and W_2 will be at a high voltage (typically W_0 and W_1). If the input
 29 value is three (3), all three of W_0 , W_1 and W_2 will be at a high voltage. If the input value is zero

1 (0), then none of W_0 , W_1 and W_2 will be at a high voltage. Alternatively, in FIG. 7B, two CAM
2 cells are used, but the transistors in the second CAM cell are twice as large, so that they produce
3 twice the current for the same terminal voltages. Consequently, the 2-bit word line value can be
4 directly applied, with the least significant bit controlling W_0 and the most significant bit controlling
5 W_1 . While it may seem like this is a smaller circuit, the second CAM cell is likely to be twice the
6 area of the first, so that the total area is equivalent to the topology shown in FIG. 7A.

7 In contrast, the disclosed invention enables the use of a single CAM cell as shown in FIG.
8 7C, wherein the multi-value input is applied to the word lines using the word line driver described
9 in FIG. 4. Although the word line driver represents some overhead in area, the area is amortized
10 over all the CAM cells in a column in a CAM cell array.

11 With reference to FIGS. 8A to 8C, shown are various CAM cell topologies for achieving
12 multi-bit storage in the CAM cells. In FIG. 8A, three CAM cell are used, wherein each CAM cell
13 stores a unary encoding of a 2-bit value. That is, if the stored value is one (1), one of the CAM
14 cells will have a one (1) stored and the other two will have a zero (0) stored. If the input value is
15 two (2), two of the CAM cells will have a one (1) stored and the other will have a zero (0) stored.
16 If the input value is three (3), all three CAM cells will have a one (1) stored. If the input value is a
17 zero (0), then all three CAM cells will have a zero (0) stored. Alternatively, in FIG. 8B, two CAM
18 cells are used, but the transistors in the upper CAM cell are twice as large, so that they produce
19 twice the current for the same terminal voltages. Consequently, the 2-bit value can be directly
20 stored, with the least significant bit stored in the lower CAM cell and the most significant bit stored
21 in the upper CAM cell. As with FIG. 7B, while it may seem like this is a smaller circuit, the second
22 CAM cell is likely to be twice the area of the first, so that the total area is equivalent to the topology
23 shown in FIG. 8A.

24 In contrast, the described invention enables the use of a single CAM cell as shown in FIG.
25 8C, wherein the 2^n multi-bit value is stored directly in the n CAM cells. The bit line driver is used
26 to multiply the bit line currents according to their weights. In FIG. 8C, the upper CAM cell, which
27 stores the most significant bit of the 2-bit value, has its output current multiplied by two (2),
28 whereas the lower CAM cell, which stores the least significant bit, has its output current multiplied
29 by one (1). Although the bit line driver represents some overhead in area, the area is amortized
30 over all the CAM cells in a row in a CAM cell array.

1 In the disclosed invention, the word line driver and the bit line driver may be used
2 separately or may be used together.

3 Since many modifications, variations, and changes in detail can be made to the described
4 preferred embodiments of the invention, it is intended that all matters in the foregoing description
5 and shown in the accompanying drawings be interpreted as illustrative and not in a limiting sense.
6 Consequently, the scope of the invention should be determined by the appended claims and their
7 legal equivalents.

1 **WHAT IS CLAIMED IS:**

- 2 1. A content addressable memory (CAM) circuit, comprising:
3 one or more of CAM cells configured to store bit values; and
4 at least one word line driver coupled to word lines of the one or more CAM cells and
5 configured to supply output to drive the word lines of the one or more CAM cells, wherein the
6 word line driver comprises:
7 a first transistor;
8 a second transistor, wherein a drain of the second transistor is coupled to a drain of
9 the first transistor;
10 a current source generating a first current, wherein a source of the second transistor
11 is coupled to the current source and a gate of the first transistor is coupled to the current
12 source, and wherein the first transistor, the second transistor and the current source are
13 configured to generate a reference voltage;
14 a third transistor;
15 a first digital-to-analog converter (DAC) coupled to a source of the third transistor
16 and gate of the first transistor;
17 a second DAC coupled to a drain of the third transistor; and
18 an operational amplifier (OpAmp) comprising:
19 a first input terminal coupled to the drain of the third transistor;
20 a second input terminal coupled to the drain of the second transistor; and
21 an output terminal supplying the output to drive the word lines of the CAM
22 cells.
23 2. The CAM circuit of claim 1 wherein the first transistor of the word line driver is a p-channel
24 field effect transistor (PFET) and the second and third transistors of the word line driver are n-
25 channel field effect transistors (NFETs).
26 3. The CAM circuit of any of the preceding claims wherein the output terminal of the OpAmp
27 of the word line driver is coupled to a gate of the third transistor of the word line driver.
28 4. The CAM circuit of any of the preceding claims wherein the first DAC and the second
29 DAC of the word line driver are configured to generate the same amount of electrical current.
30 5. The CAM circuit of any of the preceding claims wherein each CAM cell comprises:
31 a first transistor;

1 a second transistor, wherein a gate of the second transistor is coupled to a first word line,
2 and a source of the second transistor is coupled to a first bit line;
3 a third transistor, wherein a gate of the third transistor is coupled to a second word line,
4 and a source of the third transistor is coupled to a second bit line,
5 a fourth transistor, 304 wherein a gate of the fourth transistor is coupled to drains of the
6 first, second and third transistors;
7 a fifth transistor, wherein a gate of the fifth transistor is coupled to the first word line, and
8 a source of the fifth transistor is coupled to a third bit line; and
9 a sixth transistor, wherein a gate of the sixth transistor is coupled to the second word line
10 and a source of the sixth transistor is coupled to a fourth bit line, and wherein a gate of the first
11 transistor is coupled to drains of the fourth, fifth and sixth transistors.
12 6. The CAM circuit of claim 5 wherein the first and fourth transistors of the CAM cell are p-
13 channel field effect transistors (PFETs) and the second, third, fifth and sixth transistors of the CAM
14 cell are n-channel field effect transistors (NFETs).
15 7. The CAM circuit of any of claims 5-6 wherein the first and second word lines are controlled
16 by mutually exclusive word line signals.
17 8. The CAM circuit of any of claims 5-7 wherein the sources of the second, third, fifth and
18 sixth transistors respectively provide output representing Boolean operations between state of the
19 first and second word lines and state of the CAM cell.
20 9. The CAM circuit of any of the preceding claims further comprising at least one bit line
21 driver coupled to bit lines of the one or more CAM cells and configured to supply output to drive
22 the bit lines of the one or more CAM cells, wherein the bit line driver comprises:
23 a first transistor;
24 a second transistor, wherein a drain of the second transistor is coupled to a drain of the first
25 transistor; and
26 a DAC coupled to a source of the second transistor and a gate of the first transistor; and
27 an operational amplifier (OpAmp) comprising:
28 a first input terminal coupled to the source of the second transistor;
29 an output terminal supplying the output to drive the bit lines of the CAM cells; and
30 a second input terminal coupled to the output terminal.

1 10. The CAM circuit of claim 9 wherein the first transistor of the bit line driver is a p-channel
2 field effect transistor (PFET) and the second transistor of the bit line driver is n-channel field effect
3 transistor (NFET).

4 11. A content addressable memory (CAM) circuit, comprising:
5 one or more of CAM cells configured to store bit values; and
6 at least one bit line driver coupled to bit lines of the one or more CAM cells and configured
7 to supply output to drive the bit lines of the one or more CAM cells, wherein the bit line driver
8 comprises:

9 a first transistor;
10 a second transistor, wherein a drain of the second transistor is coupled to a drain of
11 the first transistor; and
12 a digital-to-analog converter (DAC) coupled to a source of the second transistor
13 and a gate of the first transistor; and
14 an operational amplifier (OpAmp) comprising:
15 a first input terminal coupled to the source of the second transistor;
16 an output terminal supplying the output to drive the bit lines of the CAM
17 cells; and
18 a second input terminal coupled to the output terminal.

19 12. The CAM circuit of claim 11 wherein the first transistor of the bit line driver is a p-channel
20 field effect transistor (PFET) and the second transistor of the bit line driver is n-channel field effect
21 transistor (NFET).

22 13. The CAM circuit of any of claims 11-12 wherein each CAM cell comprises:
23 a first transistor;
24 a second transistor, wherein a gate of the second transistor is coupled to a first word line,
25 and a source of the second transistor is coupled to a first bit line;
26 a third transistor, wherein a gate of the third transistor is coupled to a second word line,
27 and a source of the third transistor is coupled to a second bit line,
28 a fourth transistor, 304 wherein a gate of the fourth transistor is coupled to drains of the
29 first, second and third transistors;
30 a fifth transistor, wherein a gate of the fifth transistor is coupled to the first word line, and
31 a source of the fifth transistor is coupled to a third bit line; and

1 a sixth transistor, wherein a gate of the sixth transistor is coupled to the second word line
2 and a source of the sixth transistor is coupled to a fourth bit line, and wherein a gate of the first
3 transistor is coupled to drains of the fourth, fifth and sixth transistors.

4 14. The CAM circuit of claim 13 wherein the first and fourth transistors of the CAM cell are
5 p-channel field effect transistors (PFETs) and the second, third, fifth and sixth transistors of the
6 CAM cell are n-channel field effect transistors (NFETs).

7 15. The CAM circuit of any of claims 13-14 wherein the first and second word lines are
8 controlled by mutually exclusive word line signals.

9 16. The CAM circuit of any of claims 13-15 wherein the sources of the second, third, fifth and
10 sixth transistors respectively provide output representing Boolean operations between state of the
11 first and second word lines and state of the CAM cell.

12 17. The CAM circuit of any of claims 11-16 further comprising at least one word line driver
13 coupled to word lines of the one or more CAM cells and configured to supply output to drive the
14 word lines of the one or more CAM cells, wherein the word line driver comprises:

15 a first transistor;

16 a second transistor, wherein a drain of the second transistor is coupled to a drain of the first
17 transistor;

18 a current source generating a first current, wherein a source of the second transistor is
19 coupled to the current source and a gate of the first transistor is coupled to the current source, and
20 wherein the first transistor, the second transistor and the current source are configured to generate
21 a reference voltage;

22 a third transistor;

23 a first DAC coupled to a source of the third transistor and gate of the first transistor;

24 a second DAC coupled to a drain of the third transistor; and

25 an operational amplifier (OpAmp) comprising:

26 a first input terminal coupled to the drain of the third transistor; and

27 a second input terminal coupled to the drain of the second transistor; and

28 an output terminal supplying the output to drive the word lines of the CAM cells.

29 18. The CAM circuit of claim 17 wherein the first transistor of the word line driver is a p-
30 channel field effect transistor (PFET) and the second and third transistors of the word line driver
31 are n-channel field effect transistors (NFETs).

- 1 19. The CAM circuit of any of claims 17-18 wherein the output terminal of the OpAmp of the
- 2 word line driver is coupled to a gate of the third transistor to drive the third transistor.
- 3 20. The CAM circuit of any of claims 17-19 wherein the first DAC and the second DAC of the
- 4 word line driver are configured to generate the same amount of electrical current.