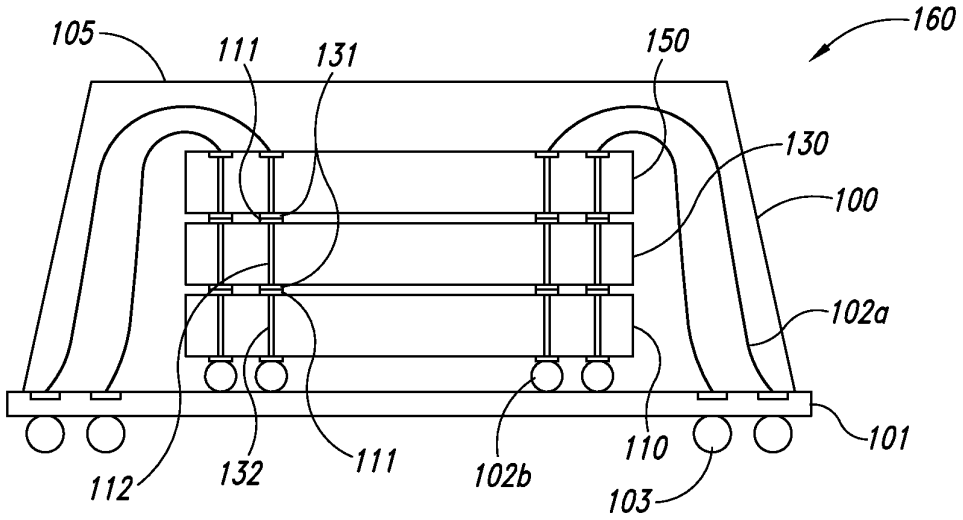

105
111
131
150
160
130
100
102a
101
110
103
102b
111
132
112

Fig. 1

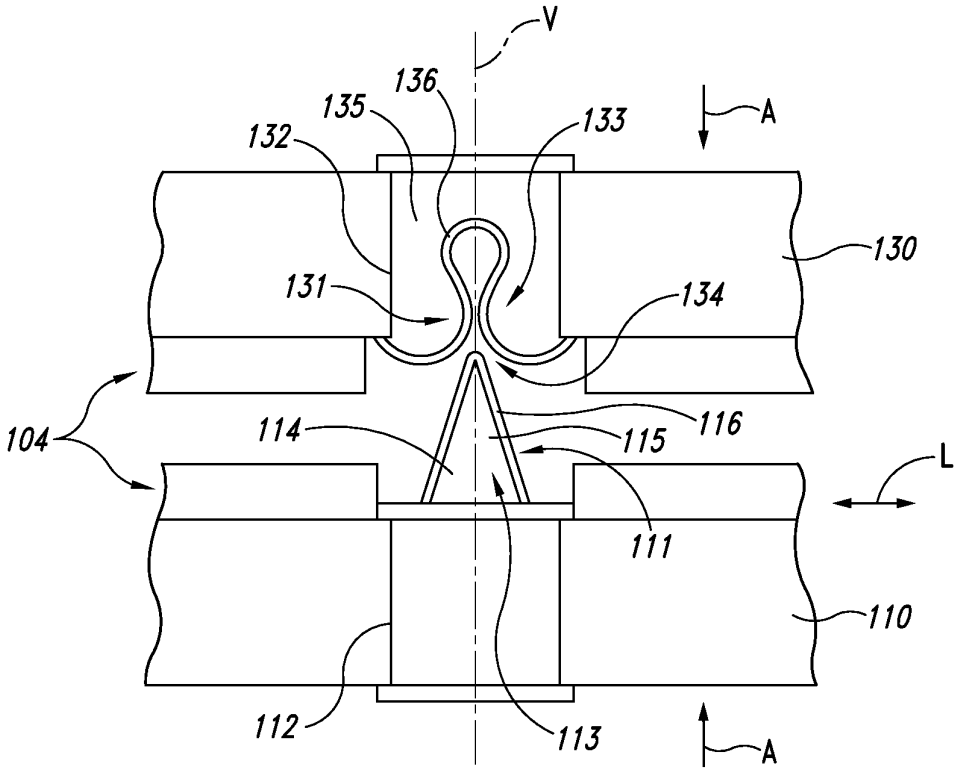

V
136
135
132
133
A
130
131
134
104
114
115
116
L
111
110
112
113
A

Fig. 2

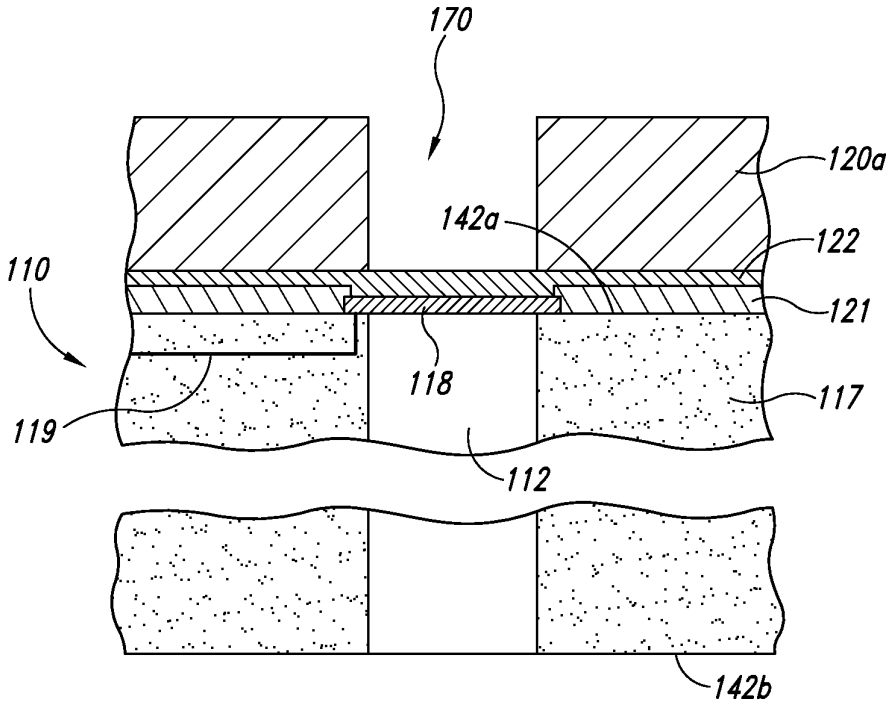

170
120a
142a
122
110
121
118
117
119
112
142b

Fig. 3A

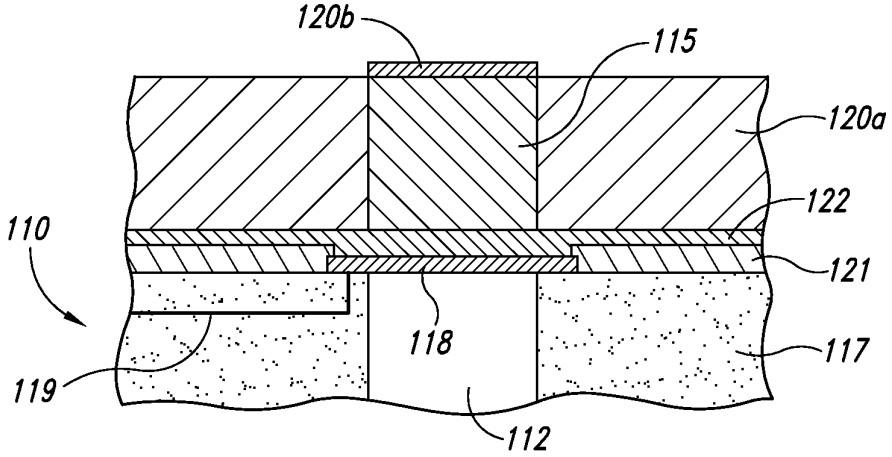

120b
115
120a
122
110
121
118
117
119
112

Fig. 3B

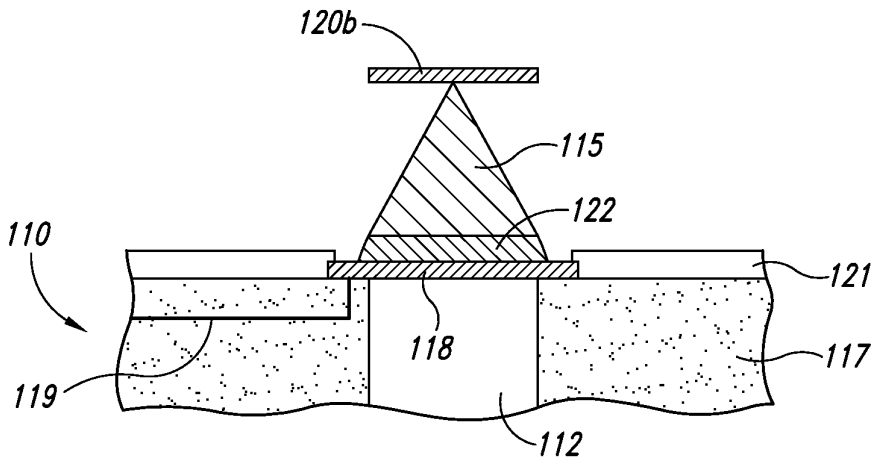


Fig. 3C

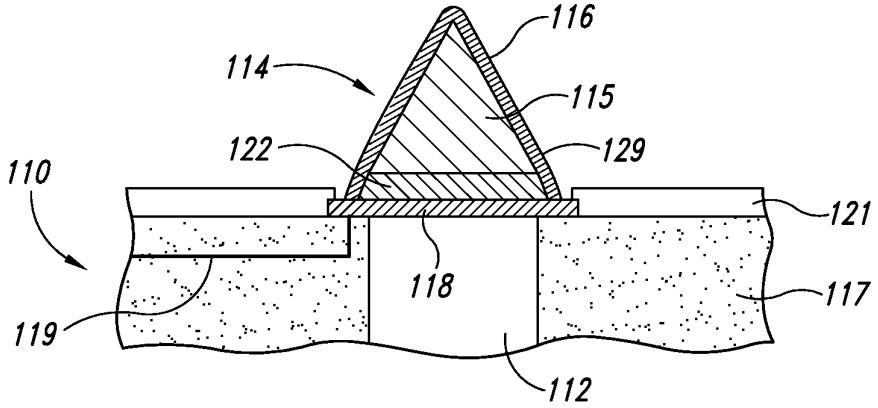


Fig. 3D

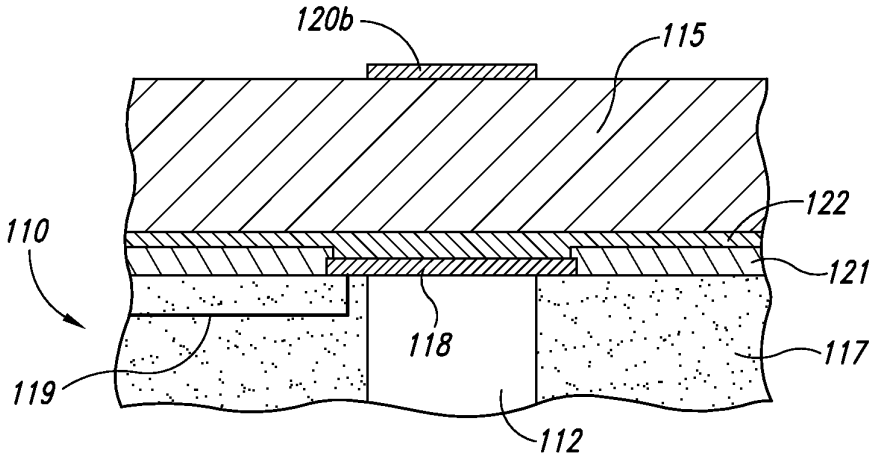


Fig. 3E

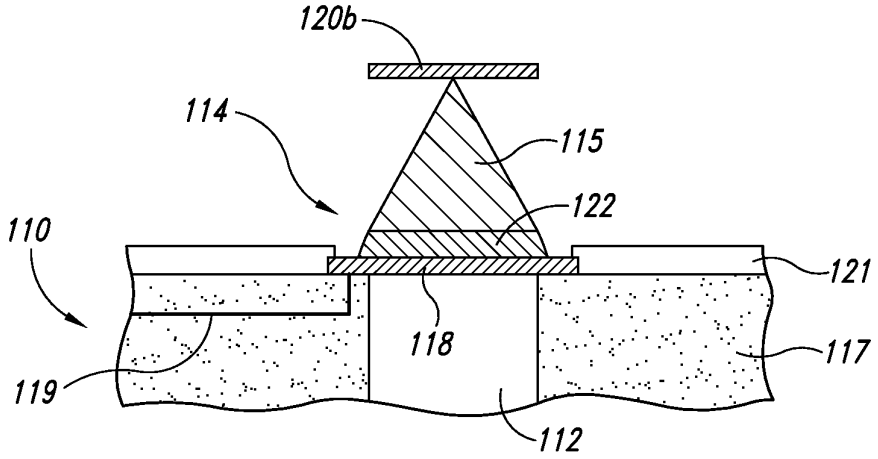

120b
114
115
122
110
121
118
117
119
112

Fig. 3F

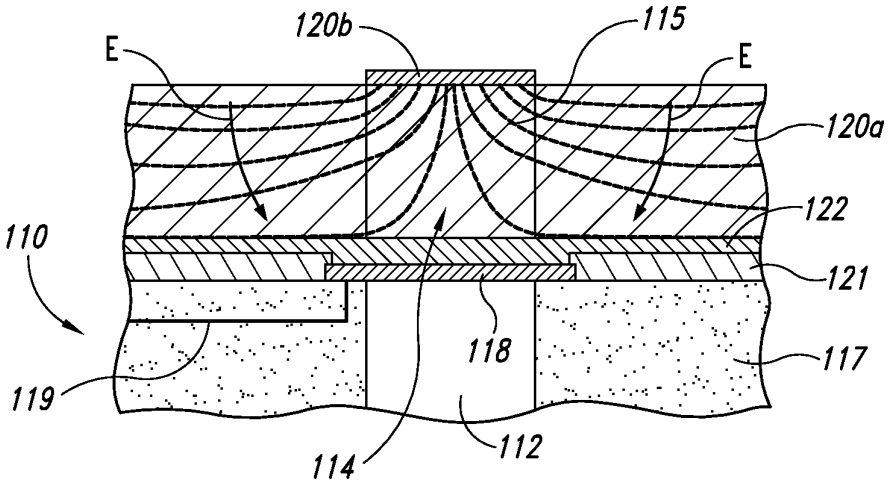

E
120b
115
E
120a
122
110
121
118
117
119
114
112

Fig. 3G

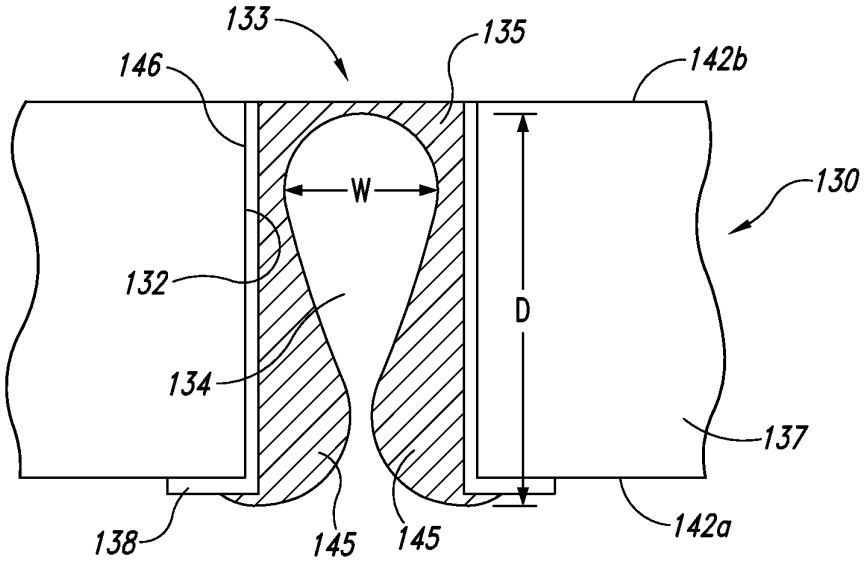

133
135
146
142b
W
130
132
D
134
137
138
145
145
142a

Fig. 4A

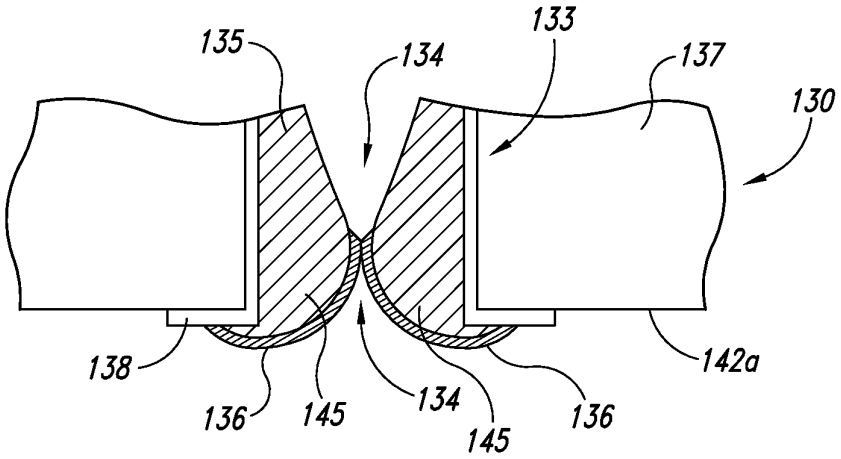

135
133
134
137
130
138
136
145
134
145
136
142a

Fig. 4B

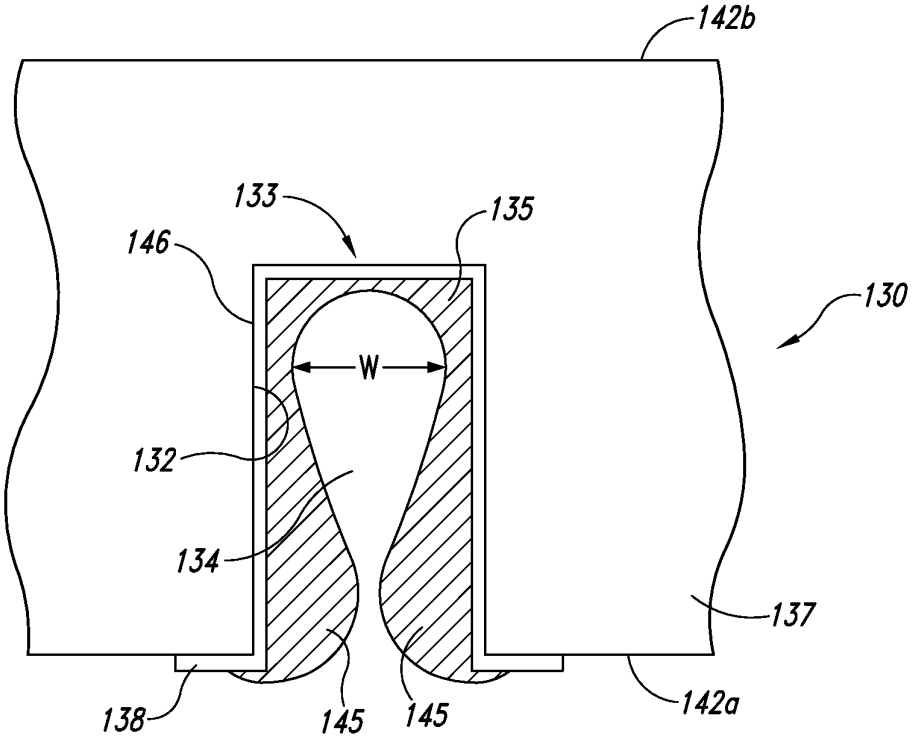

142b
133
135
146
130
W
132
134
137
138
145
145
142a

Fig. 4C

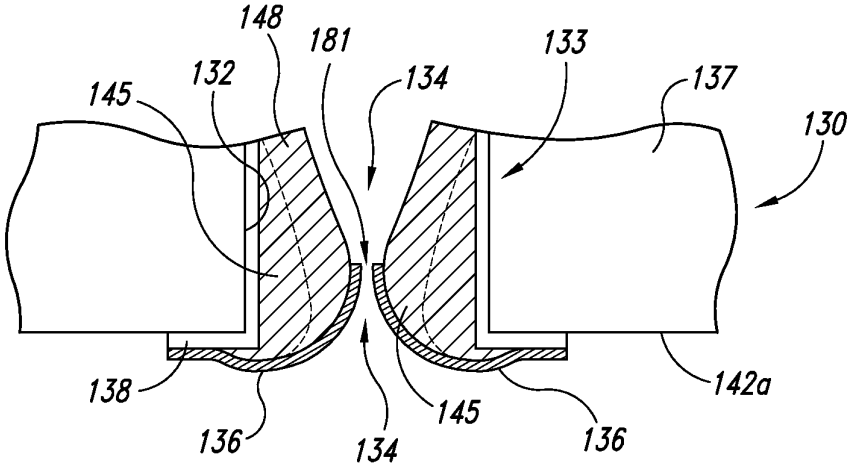

148
181
133
132
134
137
145
130
138
136
134
145
136
142a

Fig. 4D

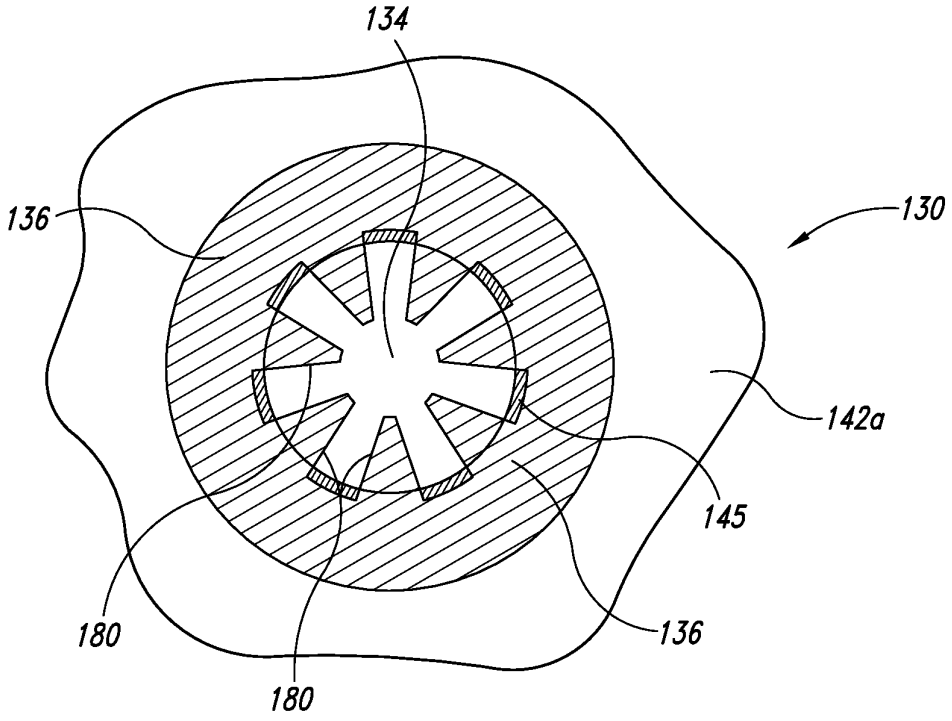


Fig. 4E

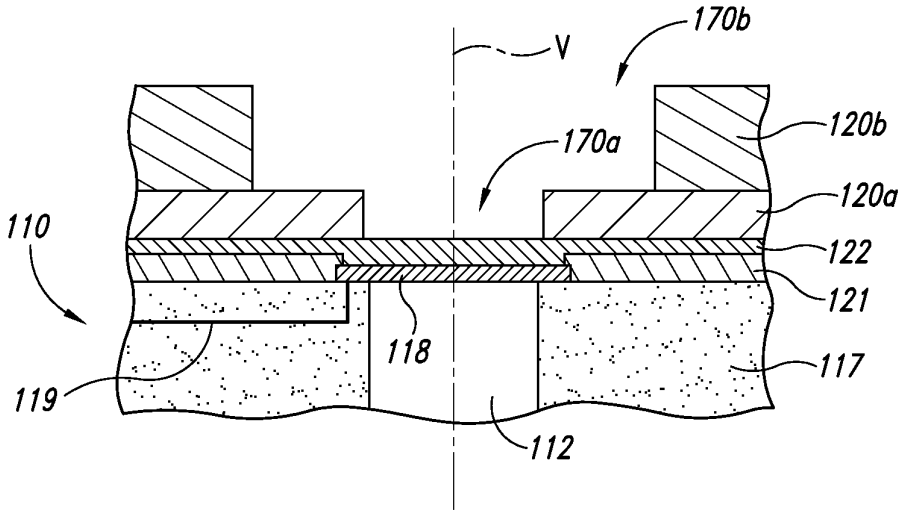

V
170b
170a
120b
120a
110
122
121
118
117
119
112

Fig. 5A

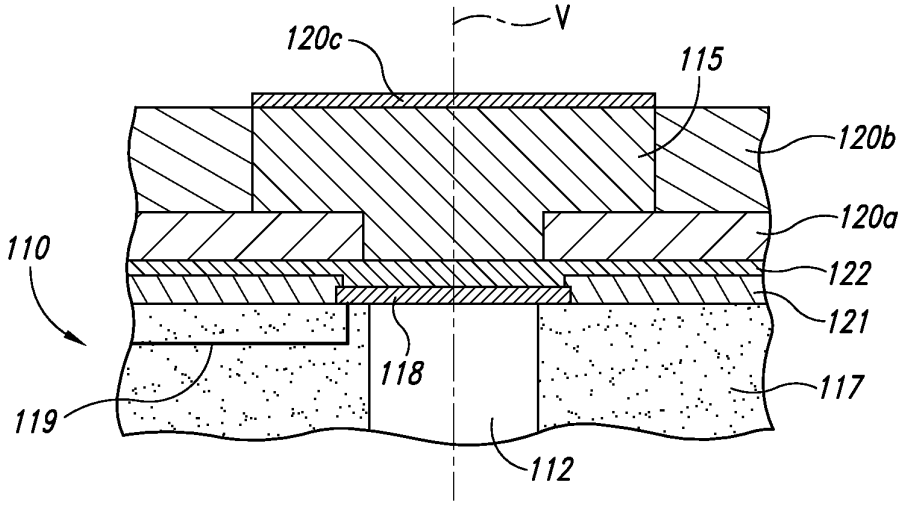

V
120c
115
120b
120a
110
122
121
118
117
119
112

Fig. 5B

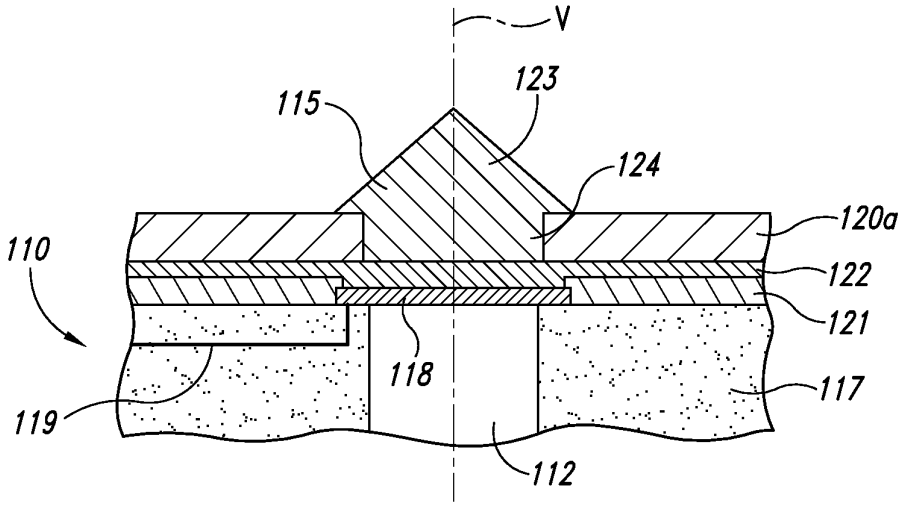

V
123
115
124
120a
110
122
121
118
117
119
112

Fig. 5C

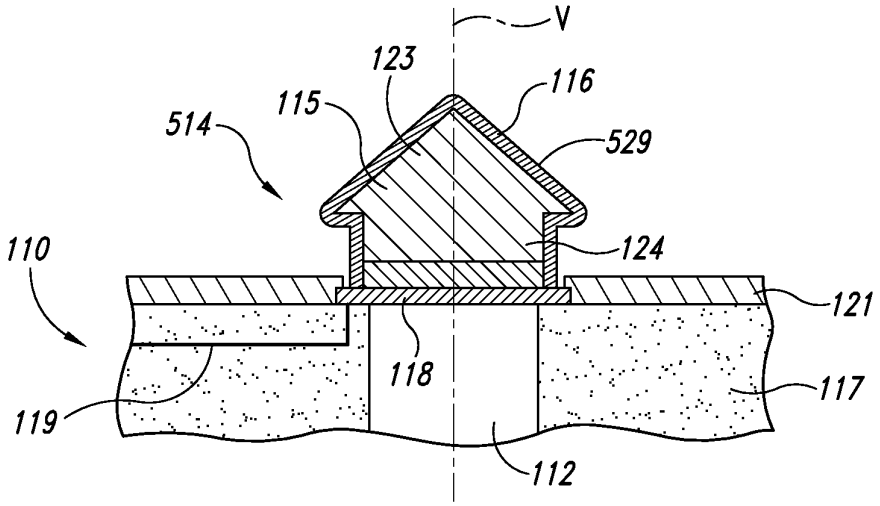

V
123
116
115
514
529
110
124
121
118
117
119
112

Fig. 5D

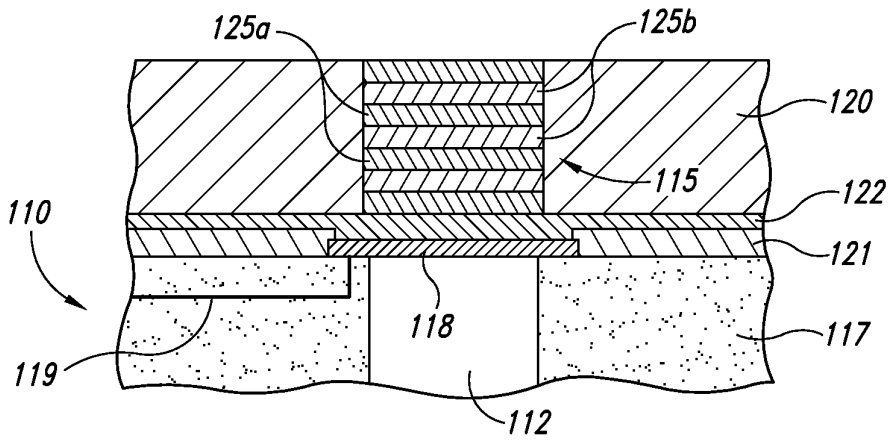


Fig. 6A

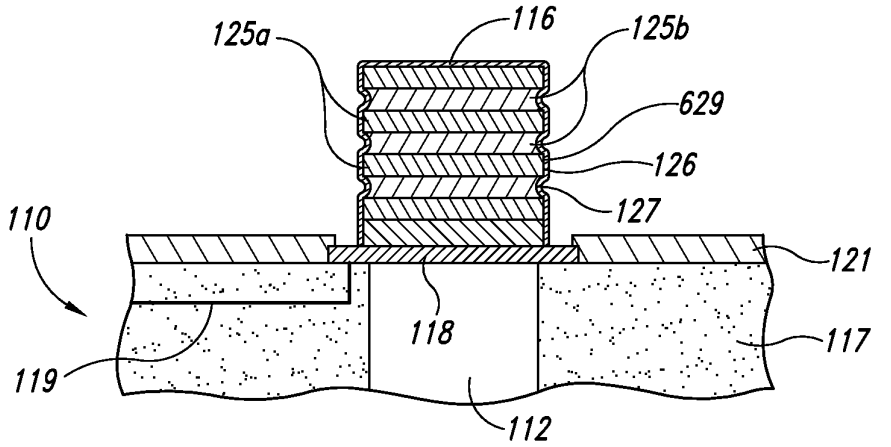


Fig. 6B

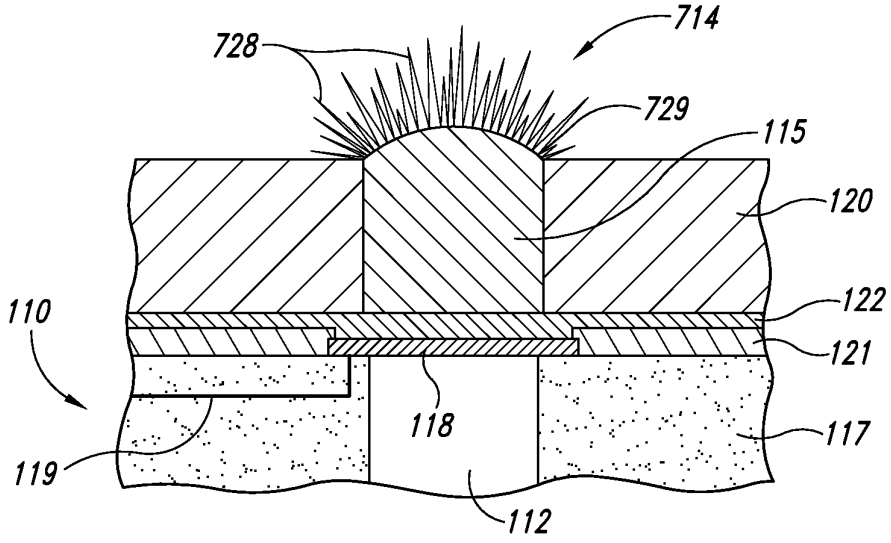


Fig. 7

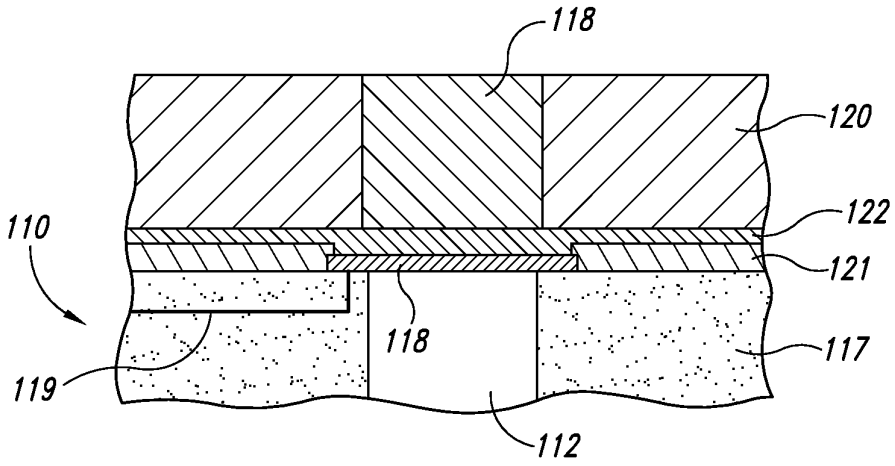

118
120
122
110
121
118
117
119
112

Fig. 8A

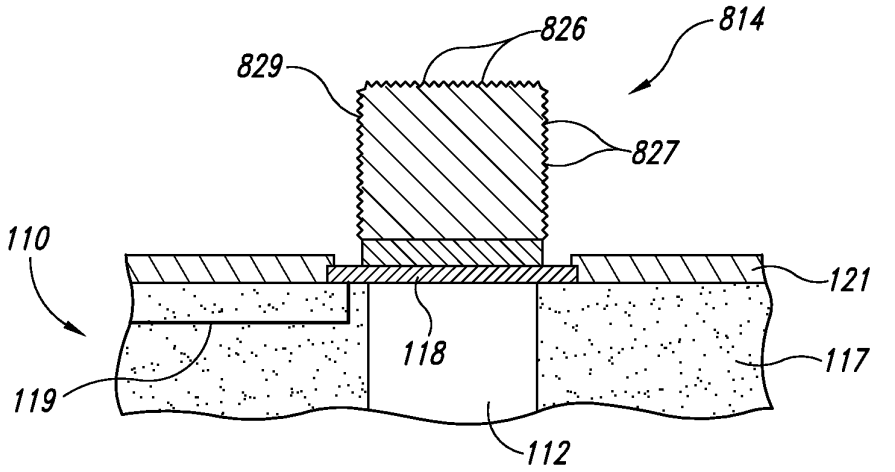

826
814
829
827
110
121
118
117
119
112

Fig. 8B

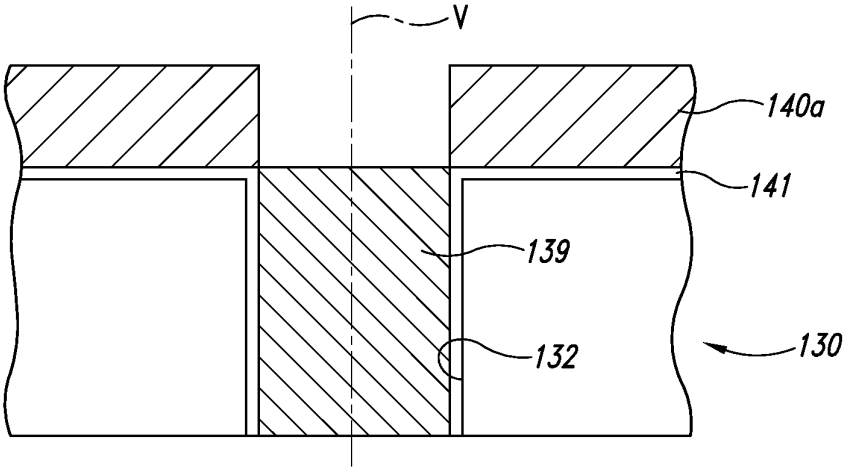


Fig. 9A

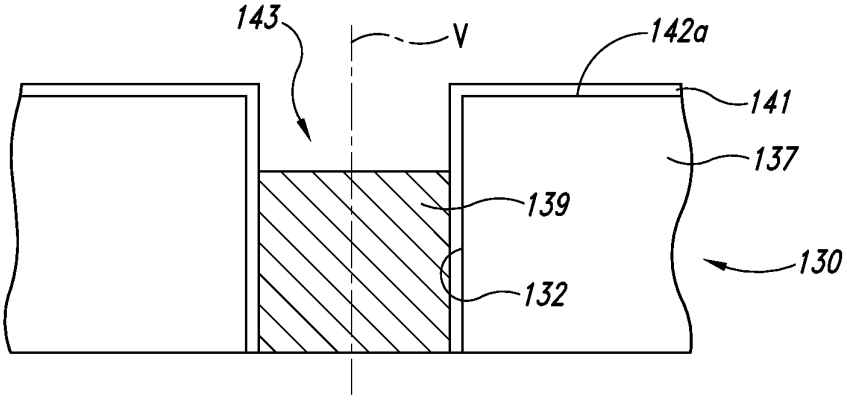


Fig. 9B

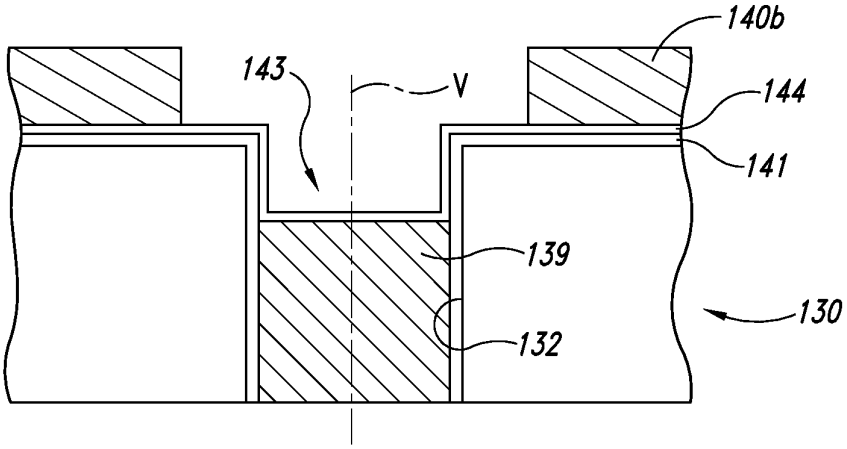


Fig. 9C

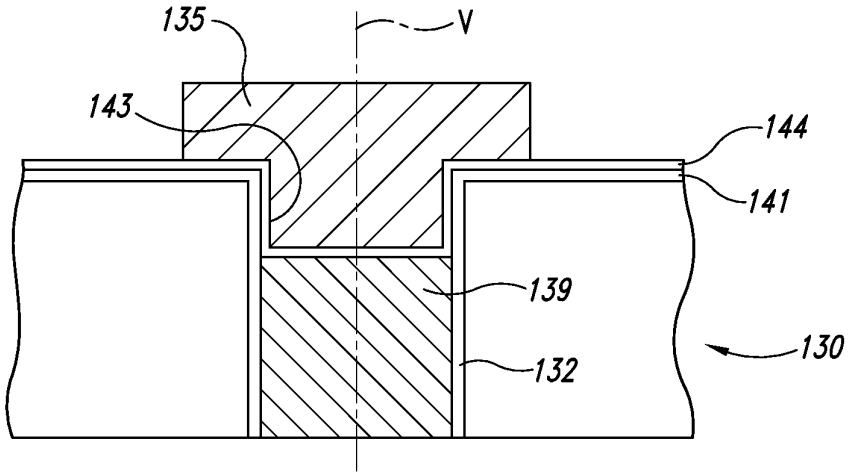

135
V
143
144
141
139
130
132

Fig. 9D

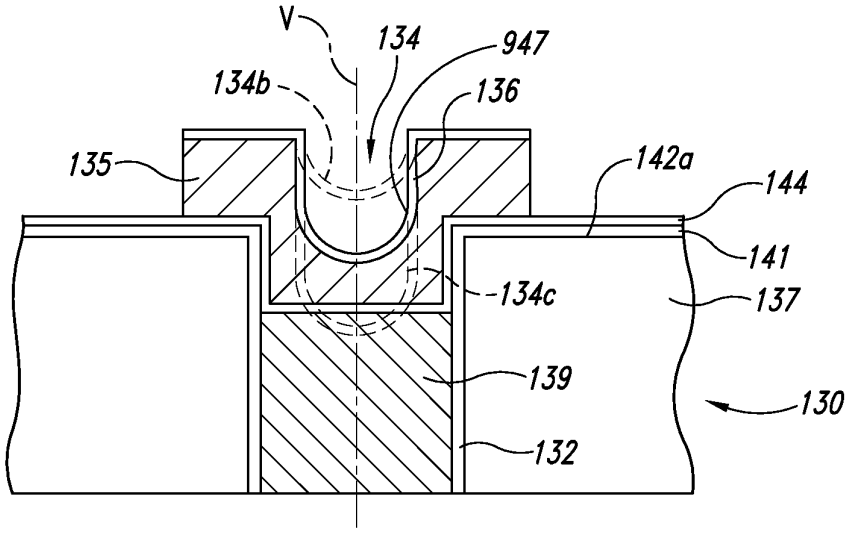

V
134
947
134b
136
135
142a
144
141
134c
137
139
130
132

Fig. 9E

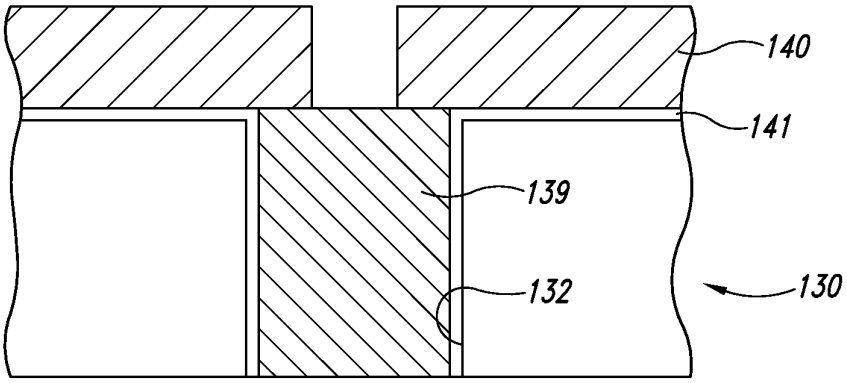


Fig. 10A

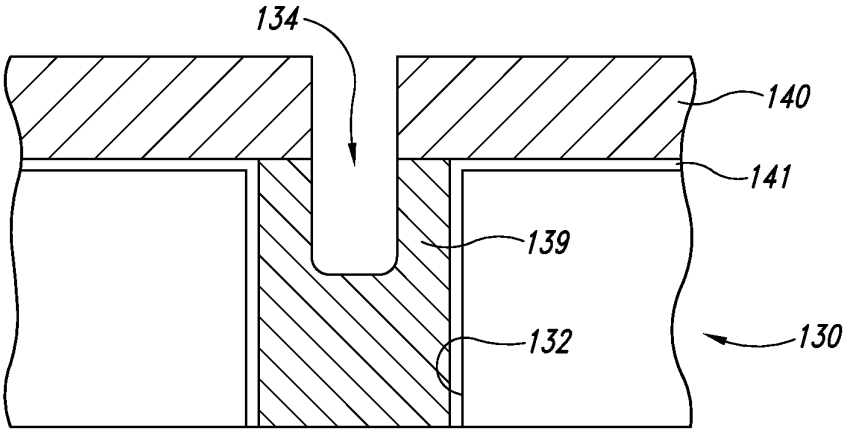


Fig. 10B

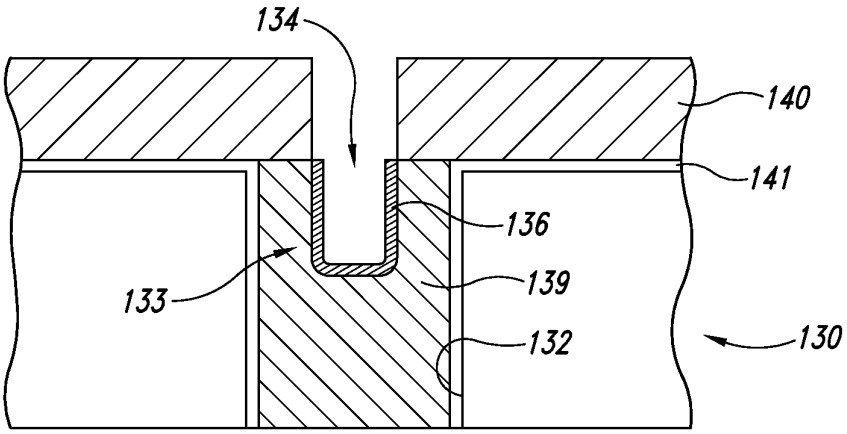


Fig. 10C

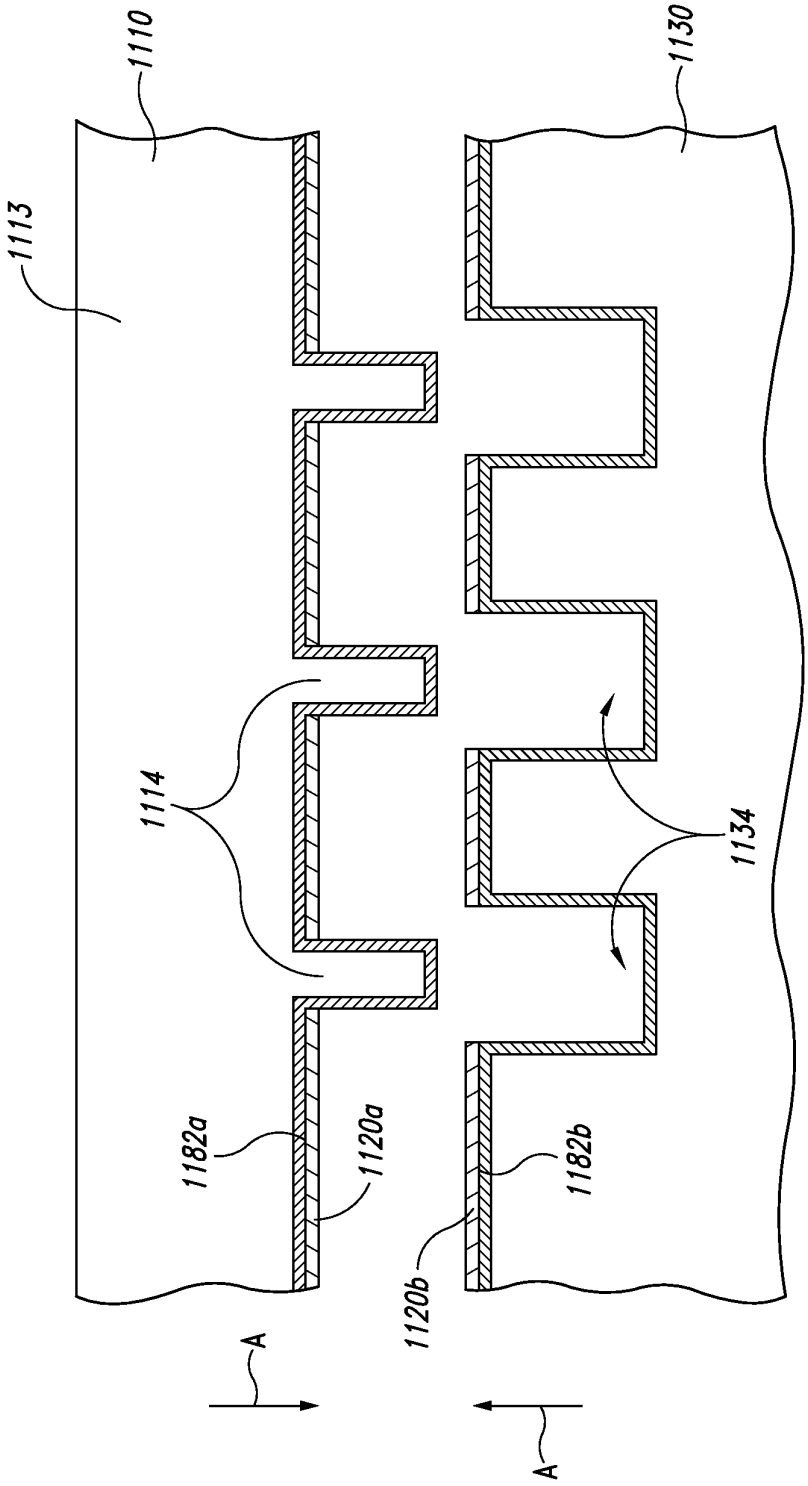


Fig. 11A

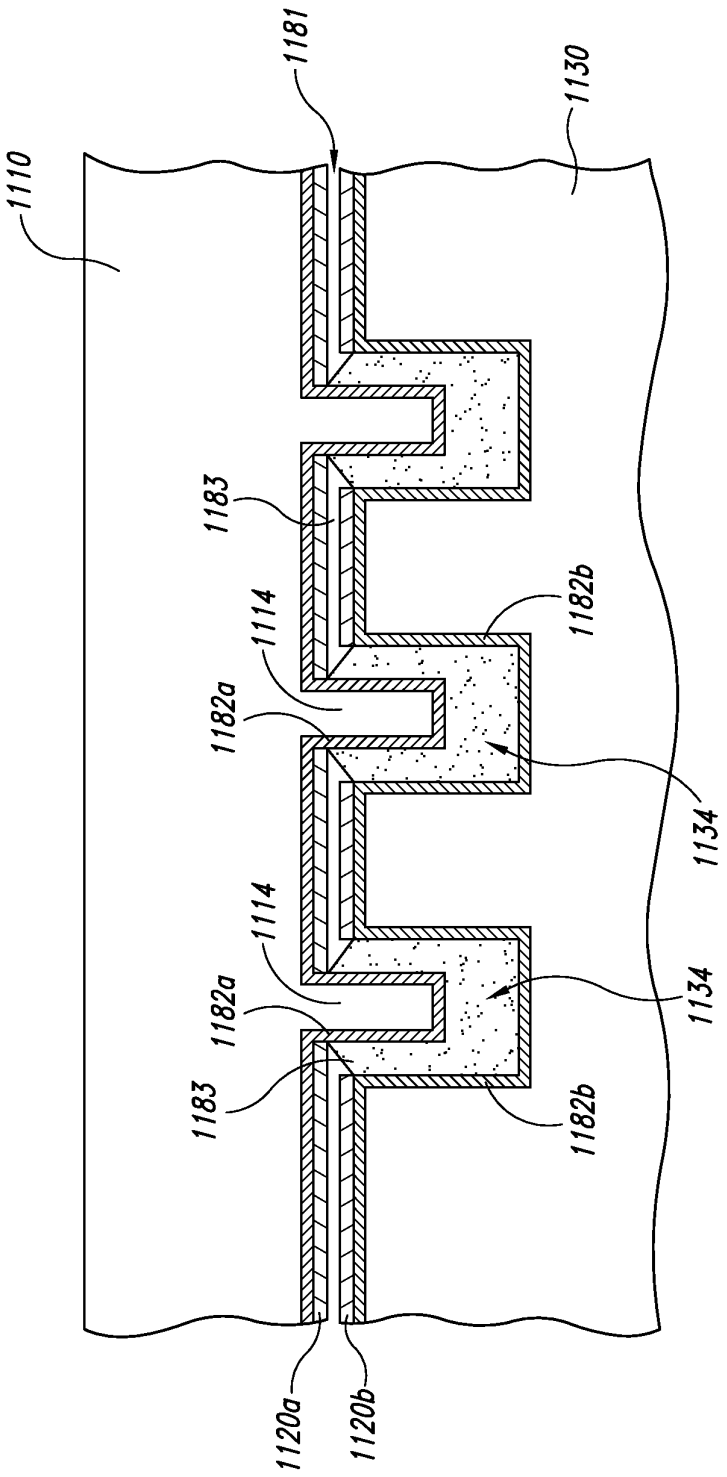

1181
1130
1110
1183
1182b
1114
1182a
1134
1114
1182a
1134
1183
1182b
1120a
1120b

Fig. 11B

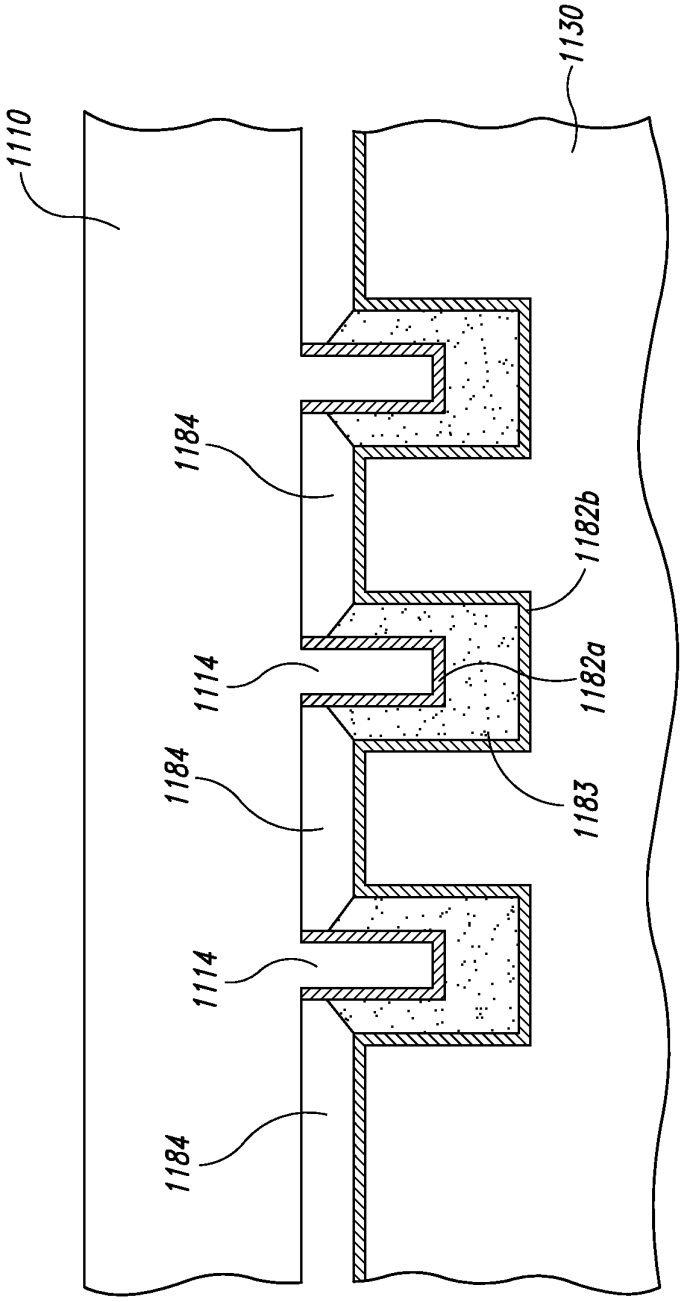


Fig. 11C

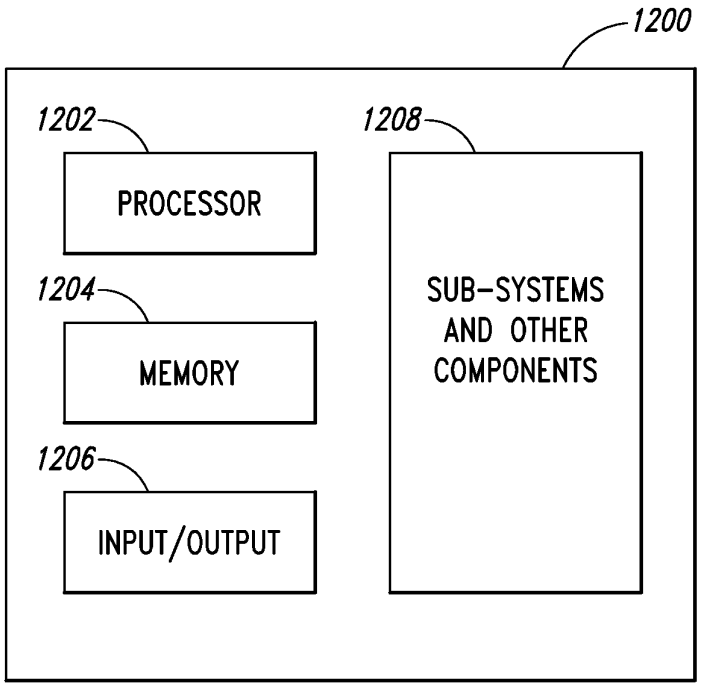

1200
1202
PROCESSOR
1204
MEMORY
1206
INPUT/OUTPUT
1208
SUB-SYSTEMS AND OTHER COMPONENTS

Fig. 12