includes a resistor R_s of a constant resistance value and a comparator, one end of the resistor R_s is connected to the j^{th} bit line in the N bit lines and the comparator, the other end of the resistor R_s is grounded, a voltage threshold of the j^{th} comparator circuit is $V_r*g_{on}*R_s*(2j+1)/2$, V_r indicates a voltage value corresponding to a Boolean value 1, and g_{on} indicates a reciprocal of R_{on}.

[0019] With reference to the second implementation of the first aspect, in a third implementation of the first aspect, the logic module includes at least three layers of RRAM crossbar arrays, and the other layers of RRAM crossbar arrays include the second layer of RRAM crossbar array and the third layer of RRAM crossbar array; the second layer of RRAM crossbar array includes a (2N–1) rows × N columns resistor array, an input end of a resistor in each row at the second layer of RRAM crossbar array is connected to a word line, an output end of a resistor in each column at the second layer of RRAM crossbar array is connected to a bit line, and word lines of the second layer of RRAM crossbar array are connected to output ends of bit lines of the first layer of RRAM crossbar array; the second layer of RRAM crossbar array receives the voltage signal corresponding to the first computing result from the output ends of the bit lines of the first layer of RRAMs through the 2N–1 word lines, and performs a logic operation according to the voltage signal corresponding to the first computing result and a resistance value of a resistor at the second layer of RRAM crossbar array:

$$\overline{O}_{2,j}=\begin{cases}\overline{O}_{1,j}+O_{1,j+1}, j<N-1\\ \overline{O}_{1,j}, j=N-1\end{cases}$$

so as to obtain a voltage signal corresponding to an intermediate computing result, where $\overline{O}_{1,j}$ is a negation of a Boolean value corresponding to a voltage signal output by the j^{th} bit line of the first layer of RRAM crossbar array, $O_{1,j+1}$ is a Boolean value corresponding to a voltage signal output by the $(j+1)^{th}$ bit line of the first layer of RRAM crossbar array, and $\overline{O}_{2,j}$ is a negation of a Boolean value corresponding to a voltage signal output by the j^{th} bit line of the second layer of RRAM crossbar array; the third layer of RRAM crossbar array includes an N rows × n columns resistor array, an input end of a resistor in each row at the third layer of RRAM crossbar array is connected to a word line, an output end of a resistor in each column at the third layer of RRAM crossbar array is connected to a bit line, and n is greater than or equal to a minimum quantity of bits required for expressing the integer N in binary; and the third layer of RRAM crossbar array receives the voltage signal corresponding to the intermediate computing result from N bit lines of the second layer of RRAM crossbar array through N word lines of the third layer of RRAM crossbar array, and encodes the intermediate computing result according to the voltage signal corresponding to the

quantity of bits required for expressing the integer N in binary; and the receiving, by the other layers of RRAM crossbar arrays, the voltage signal corresponding to the first computing result from the output ends of the N bit lines, and obtaining, according to the voltage signal corresponding to the first computing result and a resistance value of a resistor in the other layers of RRAM crossbar arrays, a voltage signal corresponding to a second computing result includes: receiving, by the second layer of RRAM crossbar array, the voltage signal corresponding to the first computing result from the output ends of the bit lines of the first layer of RRAMs through the 2N–1 word lines, and performing a logic operation according to the voltage signal corresponding to the first computing result and a resistance value of a resistor at the second layer of RRAM crossbar array:

$$\overline{O}_{2,j} = \begin{cases} \overline{O}_{1,j} + O_{1,j+1}, j < N-1 \\ \overline{O}_{1,j}, j = N-1 \end{cases}$$

so as to obtain a voltage signal corresponding to an intermediate computing result, where $\overline{O}_{1,j}$ is a negation of a Boolean value corresponding to a voltage signal output by the j^{th} bit line of the first layer of RRAM crossbar array, $O_{1,j+1}$ is a Boolean value corresponding to a voltage signal output by the $(j+1)^{th}$ bit line of the first layer of RRAM crossbar array, and $\overline{O}_{2,j}$ is a negation of a Boolean value corresponding to a voltage signal output by the j^{th} bit line of the second layer of RRAM crossbar array; and receiving, by the third layer of RRAM crossbar array, the voltage signal corresponding to the intermediate computing result from N bit lines of the second layer of RRAM crossbar array through N word lines of the third layer of RRAM crossbar array, and encoding the intermediate computing result according to the voltage signal corresponding to the intermediate computing result and a resistance value of a resistor at the third layer of RRAM crossbar array, so as to obtain the voltage signal corresponding to the second computing result.

[0027] With reference to the second aspect or the first implementation of the second aspect, in a second implementation of the second aspect, the j^{th} comparator circuit in the N comparator circuits includes a resistor R_s of a constant resistance value and a comparator, one end of the resistor R_s is connected to the j^{th} bit line in the N bit lines and the comparator, the other end of the resistor R_s is grounded, a voltage threshold of the j^{th} comparator circuit is $V_r*g_{on}*R_s*(2j+1)/2$, V_r indicates a voltage value corresponding to a Boolean value 1, and g_{on} indicates a reciprocal of R_{on}.

[0028] In some of the foregoing implementations, the storage module is a storage module based on the RRAM crossbar array. The storage module based on the RRAM crossbar array can reduce memory power consumption.

DESCRIPTION OF EMBODIMENTS

[0043] FIG. 4 is a schematic structural diagram of a memory device according to an embodiment of the present invention. It may be learned, from FIG. 4, that the memory device 40 is in an H-tree structure on the whole. In this structure, a storage module 43 (or referred to as a data module, a data array, or the like) is paired with a logic module 44 (or referred to as a logic circuit, a logic operation circuit, an in-memory logic, or the like).

[0044] Optionally, in an embodiment, both the storage module 43 and the logic module 44 may be RRAM crossbars. Further, the storage module 43 may be a single-layer RRAM crossbar, and the logic module 44 may be a multilayer RRAM crossbar. Certainly, a type of the storage module 43 is not specifically limited in this embodiment of the present invention, and another type of storage medium may be used. In addition, even if both the storage module 43 and the logic module 44 are RRAM crossbars, a quantity of layers of the RRAM crossbar is not specifically limited in this embodiment of the present invention. For example, the storage module 43 may be designed as a multilayer RRAM crossbar, and the logic module 44 may be designed as a single-layer logic module 44 (a single-layer RRAM crossbar can also implement a simple logic operation).

[0045] Still referring to FIG. 4, the memory device 40 mainly includes four parts: a block decoder 41 (Block decoder), a storage module 43, a logic module 44, and a control module 45. The control module 45 may be a CMOS-based control module. The storage module 43, the logic module 44, and the control module 45 may be included in a memory unit 42 (or referred to as a data/logic pair).

[0046] In FIG. 4, the control module 45 is separately connected to the storage module 43, the logic module 44, and the block decoder 41, and is connected to the processor 47 (such as a CPU) through the block decoder 41. The control module 45 may receive and parse an instruction of the processor 47, and may further be responsible for data exchange or transmission between the storage module 43 and the logic module 44. The block decoder 41 may transfer the instruction delivered by the processor 47 to a control module 45 of a memory unit 42 corresponding to the instruction. In addition, in an embodiment, an address search function of the memory unit 42 may be integrated in the block decoder 41, and remaining control functions are all integrated in the control module 45.

[0047] It may be learned, from the foregoing description, that the control module 45 may be connected to the block decoder 41, but the block decoder 41 may be responsible only for transferring the instruction delivered by the processor 47 to the control module 45 of the corresponding memory unit 42. Therefore, from another perspective, the control module 45

ST (Start)	Memory unit serial number	-	Turn on all row/column switches of a logic module in a memory unit corresponding to this serial number	Performing memory computing
WT (Wait)	-	-	Wait for a completion signal of memory computing of a logic module	Preventing an instruction in an instruction queue from being operated during memory computing

[0050] Using a memory computing process as an example, first, logic configuration is performed on the logic module 44, that is, a resistance value of a resistor in the logic module 44 is configured so that the logic module 44 can implement particular operation logic. Then an input signal is provided to the logic module 44. That is, data requiring a logic operation is input into the logic module 44. Then, memory computing may be performed in the logic module 44 according to the input signal and configured operation logic. The following describes in detail a memory computing process with reference to the instructions in Table 1.

[0051] When memory computing is needed, the processor 47 may deliver the following instructions to the memory device 40.

[0052] Instruction 1: an SW instruction, which is used to write data in the processor 47 or the storage module 43 into the logic module 44 to configure a resistance value of the RRAM in the logic module 44, so that the logic module can implement particular logic such as summation, exclusive OR, and multiplication.

[0053] Instruction 2: an SW instruction, which is used to write data in the processor 47 or the storage module 43 into an input column (a voltage V_{wl}^{i} input by a word line (word line) in FIG. 6) of the logic module 44. A particular logic operation on input data can be implemented in the logic module based on previously configured operation logic. For example, the logic module 44 implements a+b summation logic. b may be stored into the logic module by using the instruction 1, then a is input by using the instruction 2, and then a and b are summed.

[0054] Instruction 3: an ST instruction, which is used to turn on all row/column switches of the logic module 44, so that a current flows through all rows/columns of the logic module 44.

[0055] Instruction 4: a WT instruction. When a complex logic operation is implemented by using an RRAM crossbar, multiple layers of RRAM crossbars are needed in the logic module 44. In this case, it takes a time to complete computing of the RRAM crossbars. Therefore, the ST instruction may be used to instruct the control module 45 to wait for completion of memory computing of the logic module 44, and then execute a subsequent instruction.

A voltage threshold V_{th2} of the comparator circuit may be set to $V_r*g_{on}*R_s/2$. In addition, a positive pole and a negative pole of a comparator in an operation circuit need to be swapped (that is, the voltage threshold V_{th2} is set at an in-phase input end of the comparator, and a reverse-phase input end is connected to the resistor R_s and the bit line) to obtain an output $O_{2,j}$ of the second layer, where $0 \leq j \leq N-1$.

[0082] A relationship between the output $O_{2,j}$ of the second layer of RRAM crossbar and the output of the first layer of RRAM crossbar may be expressed by a formula (5). That is, the formula (5) is a logic function to be implemented by the second layer of the RRAM crossbar.

$$\overline{O}_{2,j} = \begin{cases} \overline{O}_{1,j} + O_{1,j+1}, j < N-1 \\ \overline{O}_{1,j}, j = N-1 \end{cases} \quad (5)$$

[0083] Logic expressed by the formula (5) is actually exclusive-OR logic. That is, an exclusive-OR operation is performed pairwise on the first computing result output by the first layer of RRAM crossbar to obtain an intermediate computing result. The intermediate computing result is an N-dimensional vector. The $(K-1)^{th}$ element of the N-dimensional vector is 1, and remaining elements are 0. K is a result of a point multiplication operation on the Boolean vector $\left[\phi_{0,j}, \phi_{1,j} \ldots \phi_{N-1,j}\right]$ and the Boolean vector $\left[x_{i,0}, x_{i,1} \ldots x_{i,N-1}\right]$. That an output result of the first layer of RRAM crossbar is 11100000 is used as an example. An obtained result is 00100000 after the logic operation of the second layer is performed. However, it should be noted that a structure of the RRAM crossbar for implementing the exclusive-OR logic is not specifically limited in this embodiment of the present invention, and FIG. 8 is merely an example. In practice, the exclusive-OR logic may alternatively be implemented by configuring resistance values of resistors and voltage thresholds in another manner.

[0084] The second layer of RRAM crossbar transfers the voltage signal corresponding to the intermediate computing result to the word lines of the second layer of RRAM crossbar. The output end $O_{2,j}$ of the j^{th} bit line of the second layer of RRAM crossbar is connected to the input end of the j^{th} word line of the third layer of RRAM crossbar. A logic circuit of the third layer of RRAM crossbar is shown in FIG. 9. The third layer of RRAM crossbar includes an N×n resistor array, where n is greater than or equal to a minimum quantity of bits required for expressing the integer N in binary (for example, N=8, a binary representation of 8 is 1000, that is, the binary representation of 8 requires 4 bits, and therefore, n is greater than or equal to 4). Resistance values of N rows of resistors are set so that the resistors indicate binary 1 to N sequentially from top to bottom. In this way, when the voltage signal corresponding to the intermediate operation result output by the second layer of RRAM crossbar is used as an input voltage signal

CLAIMS

1. A data processing apparatus comprising:

a control bus; and

multiple memory units connected by the control bus, each of the multiple memory units comprising a control circuit and a computation circuit,

wherein the computation circuit comprises a first resistive random access memory (RRAM) crossbar array and a format conversion circuit, the first RRAM crossbar array having multiple rows and multiple columns of memory cells, multiple word lines connected to respective rows of memory cells, and a plurality of comparator circuits each connected to a corresponding column of the first RRAM crossbar array, wherein the comparator circuits are set to have incremental thresholds, and outputs of the comparator circuits are connected to the format conversion circuit;

wherein the control circuit is connected to the control bus and configured to:

receive a computation instruction for performing a vector multiplication of vector A and vector B;

setting the memory cells in the first RRAM crossbar array such that states of memory cells of each column of the first RRAM crossbar array correspond to elements of vector B;

setting the word lines of the first RRAM crossbar array according to elements of vector A;

wherein the outputs of the comparator circuits are voltage signals corresponding to a first binary number in which a number of bits with a value 1 indicates a numerical result of multiplication of vector A and vector B;

the format conversion circuit being set up to convert the outputs of the comparator circuits into an output corresponding to a second binary number having a numerical value equal to the numerical result of multiplication of vector A and vector B.

2. The data processing apparatus according to claim 1, wherein the format conversion circuit comprises:

a second RRAM crossbar array connected to receive the outputs of the comparator circuits and configured to generate an output that corresponds to an intermediate binary number in

which a location of a bit with a value 1 indicates the numerical result of multiplication of vector A and vector B; and

a third RRAM crossbar array connected to receive the output of the second RRAM crossbar array and configured to generate the output corresponding to the second binary number.

3. The data processing apparatus according to claim 2, wherein

the multiple rows and multiple columns of memory cells in the first RRAM crossbar array comprise N rows × N columns resistors, an input end of a resistor in each row at the first RRAM crossbar array is connected to a word line, an output end of a resistor in each column at the first RRAM crossbar array is connected to a bit line, N word lines of the first RRAM crossbar array are connected to the control circuit, and each of N bit lines of the first RRAM crossbar array are respectively connected to a comparator circuit of the plurality of comparator circuits;

the first RRAM crossbar array generates N current signals on the N bit lines according to voltage signals input by the N word lines and a resistance value of a resistor at the first RRAM crossbar array, a voltage value of a voltage signal input by the j^{th} word line in the N word lines is a voltage value corresponding to B_j, a resistance value of a resistor in the j^{th} row at the first RRAM crossbar array is a resistance value corresponding to A_j, B_j is the j^{th} element of vector B, A_j is the j^{th} element of vector A, and a value of j ranges from 0 to N–1, wherein each of vector A and vector B indicates an N-dimensional vector, each elements of vector A and vector B indicates a value 1 or 0, and N is a positive integer not less than 2;

the N comparator circuits respectively convert the N current signals into N voltage signals, and compare the N voltage signals with voltage thresholds respectively corresponding to the N comparator circuits, to output, from output ends of the comparator circuits, the voltage signals corresponding to the first binary number, wherein the first binary number is an N-dimensional vector, first K elements of the first binary number are 1, remaining elements are 0, and K is the result of multiplication of vector A and vector B; and

the format conversion circuit receives the voltage signals corresponding to the first binary number from the output ends of the comparator circuits, and generates, according to the voltage signals corresponding to the first binary number and resistance values of resistors in the format conversion circuit, voltage signals corresponding to the second binary number, wherein the second binary number is a binary representation of K.

4. The data processing apparatus according to claim 3, wherein the j^{th} comparator circuit in the N comparator circuits comprises a resistor R_s of a constant resistance value and a comparator, one end of the resistor R_s is connected to the j^{th} bit line in the N bit lines and the comparator, the other end of the resistor R_s is grounded, a voltage threshold of the j^{th} comparator circuit is $V_r*g_{on}*R_s*(2j+1)/2$, V_r indicates a voltage value corresponding to a value 1, and g_{on} indicates a reciprocal of R_{on}.

5. The data processing apparatus according to claim 4, wherein

the second RRAM crossbar array comprises a (2N–1) rows × N columns resistor array, an input end of a resistor in each row at the second RRAM crossbar array is connected to a word line, an output end of a resistor in each column at the second RRAM crossbar array is connected to a bit line, and each of word lines of the second RRAM crossbar array is connected to a output end of a comparator circuit in the first RRAM crossbar array;

the second RRAM crossbar array receives the voltage signals corresponding to the first binary number from the output ends of the comparator circuits of the first RRAM crossbar array through the 2N–1 word lines, and performs a logic operation according to the voltage signal corresponding to the first computing result and a resistance value of a resistor at the second layer of RRAM crossbar array:

$$\overline{O}_{2,j} = \begin{cases} \overline{O}_{1,j} + O_{1,j+1}, j < N-1 \\ \overline{O}_{1,j}, j = N-1 \end{cases}$$

to obtain voltage signals corresponding to the intermediate binary number, wherein $\overline{O}_{1,j}$ is a negation of a value corresponding to a voltage signal output by a comparator circuit connected to the j^{th} bit line of the first RRAM crossbar array, $O_{1,j+1}$ is a value corresponding to a voltage signal output by a comparator circuit connected to the $(j+1)^{th}$ bit line of the first RRAM crossbar array, and $\overline{O}_{2,j}$ is a negation of a value corresponding to a voltage signal output by the j^{th} bit line of the second RRAM crossbar array;

the third RRAM crossbar array comprises an N rows × n columns resistor array, an input end of a resistor in each row at the third RRAM crossbar array is connected to a word line, an output end of a resistor in each column at the third RRAM crossbar array is connected to a bit

line, and n is greater than or equal to a minimum quantity of bits required for expressing the integer N in binary; and

the third RRAM crossbar array receives voltage signals corresponding to the intermediate binary number from N bit lines of the second RRAM crossbar array through N word lines of the third RRAM crossbar array, and encodes the intermediate binary number according to the voltage signals corresponding to the intermediate binary number and resistance values of resistors at the third RRAM crossbar array to obtain voltage signals corresponding to the second binary number.

6. The data processing apparatus according to claim 5, wherein the j^{th} word line of the third RRAM crossbar array is connected to the j^{th} bit line of the second RRAM crossbar array, and a resistance value of a resistor in the j^{th} row of the third RRAM crossbar array corresponds to a binary representation of the integer j+1.

7. The data processing apparatus according to claim 1, wherein vector A is a row vector of a matrix Φ, vector B is a column vector of a matrix X, each of the multiple computation circuits in the memory device is set for performing point multiplication operations of a plurality of row vectors of the matrix Φ and a plurality of column vectors of the matrix X, and the multiple computation circuits jointly implement a matrix multiplication operation of the matrix Φ and the matrix X.

8. The data processing apparatus according to claim 1, wherein the instruction of the processor further comprises a data access instruction, and each memory unit further comprises:

a storage circuit, wherein the storage circuit is connected to the control circuit, and the control circuit read data from the computation circuit or write data into the computation circuit according to the data access instruction.

9. A data processing apparatus comprising:

a control bus; and

a memory unit connected to the control bus, the memory unit comprising a control circuit and a computation circuit,

wherein the computation circuit comprises a first resistive random access memory (RRAM) crossbar having multiple rows and multiple columns of memory cells, multiple word lines connected to respective rows of memory cells, and a plurality of comparator circuits each connected to a corresponding column of the first RRAM crossbar array, wherein the comparator circuits are set to have incremental thresholds;

wherein the control circuit is connected to the control bus and configured to:

receive a computation instruction for performing a vector multiplication of vector A and vector B;

setting the memory cells in the first RRAM crossbar array such that states of memory cells of each column of the first RRAM crossbar array correspond to elements of vector B; and

setting the word lines of the first RRAM crossbar array according to elements of vector A;

wherein the outputs of the comparator circuits are voltage signals corresponding to a first binary number in which a number of bits with a value 1 indicates a numerical result of multiplication of vector A and vector B.

10. The data processing apparatus according to claim 9, wherein the computation circuit further comprises a second RRAM crossbar array and a third RRAM crossbar array each having multiple rows and multiple columns of memory cells and multiple word lines connected to respective rows of memory cells, wherein outputs of the comparator circuits are connected to corresponding word lines of the second RRAM crossbar array, outputs of the second RRAM crossbar array are connected to corresponding words lines of the third RRAM crossbar array, wherein

the second RRAM crossbar array being set up to convert the outputs of the comparator circuits into an output representing an intermediate binary number in which a location of a bit with a value 1 indicates the numerical result of multiplication of vector A and vector B; and

the third RRAM crossbar array being set up to convert the output of the second RRAM crossbar into an output representing a second binary number having a numerical value equal to the numerical result of multiplication of vector A and vector B.

11. The data processing apparatus according to claim 10, wherein the multiple rows and multiple columns of memory cells in the first RRAM crossbar array comprise N rows × N columns resistors, an input end of a resistor in each row at the first RRAM crossbar array is connected to a word line, an output end of a resistor in each column at the first RRAM crossbar array is connected to a bit line, N word lines of the first RRAM crossbar array are connected to the control circuit, and each of N bit lines of the first RRAM crossbar array are respectively connected to a comparator circuit of the plurality of comparator circuits;

the first RRAM crossbar array generates N current signals on the N bit lines according to voltage signals input by the N word lines and a resistance value of a resistor at the first RRAM crossbar array, a voltage value of a voltage signal input by the j^{th} word line in the N word lines is a voltage value corresponding to B_j, a resistance value of a resistor in the j^{th} row at the first RRAM crossbar array is a resistance value corresponding to A_j, B_j is the j^{th} element of vector B, A_j is the j^{th} element of vector A, and a value of j ranges from 0 to N–1, wherein each of vector A and vector B indicates an N-dimensional vector, each elements of vector A and vector B indicates a value 1 or 0, and N is a positive integer not less than 2;

the N comparator circuits respectively convert the N current signals into N voltage signals, and compare the N voltage signals with voltage thresholds respectively corresponding to the N comparator circuits, to output, from output ends of the N comparator circuits, the voltage signals corresponding to the first binary number, wherein the first binary number is an N-dimensional vector, first K elements of the first binary number are 1, remaining elements are 0, and K is the result of multiplication of vector A and vector B;

the second RRAM crossbar array receives the voltage signals corresponding to the first binary number from the output ends of the comparator circuits, and obtain, according to the voltage signals corresponding to the first binary number and resistance values of resistors in the second RRAM crossbar array, voltage signals corresponding to the intermediate binary number in which a location of a bit with a value 1 indicates the numerical result of multiplication of vector A and vector B; and

the third RRAM crossbar array receives the voltage signals corresponding to the intermediate binary number from the bit lines of second RRAM crossbar array, and convert the intermediate binary number into the second binary number, wherein the second binary number is a binary representation of K.

12. The data processing apparatus according to claim 11, wherein the j^{th} comparator circuit in the N comparator circuits comprises a resistor R_s of a constant resistance value and a comparator, one end of the resistor R_s is connected to the j^{th} bit line in the N bit lines and the comparator, the other end of the resistor R_s is grounded, a voltage threshold of the j^{th} comparator circuit is $V_r*g_{on}*R_s*(2j+1)/2$, V_r indicates a voltage value corresponding to a value 1, and g_{on} indicates a reciprocal of R_{on}.

13. The data processing apparatus according to claim 11, wherein the second RRAM crossbar array comprises a (2N–1) rows × N columns resistor array, an input end of a resistor in each row at the second RRAM crossbar array is connected to a word line, an output end of a resistor in each column at the second RRAM crossbar array is connected to a bit line, and each of word lines of the second RRAM crossbar array is connected to a output end of a comparator circuit in the first RRAM crossbar array;

the second RRAM crossbar array receives the voltage signals corresponding to the first binary number from the output ends of the comparator circuits of the first RRAM crossbar array through the 2N–1 word lines, and performs a logic operation according to the voltage signals corresponding to the first binary number and a resistance value of a resistor at the second RRAM crossbar array:

$$\overline{O}_{2,j} = \begin{cases} \overline{O}_{1,j} + O_{1,j+1}, j < N-1 \\ \overline{O}_{1,j}, j = N-1 \end{cases}$$

to obtain voltage signals corresponding to an intermediate binary number, wherein $\overline{O}_{1,j}$ is a negation of a value corresponding to a voltage signal output by a comparator circuit connected to the j^{th} bit line of the first RRAM crossbar array, $O_{1,j+1}$ is a value corresponding to a voltage signal output by a comparator circuit connected to the $(j+1)^{th}$ bit line of the first RRAM crossbar array, and $\overline{O}_{2,j}$ is a negation of a value corresponding to a voltage signal output by the j^{th} bit line of the second RRAM crossbar array;

the third RRAM crossbar array comprises an N rows × n columns resistor array, an input end of a resistor in each row at the third RRAM crossbar array is connected to a word line, an output end of a resistor in each column at the third RRAM crossbar array is connected to a bit

line, and n is greater than or equal to a minimum quantity of bits required for expressing the integer N in binary; and

the third RRAM crossbar array receives voltage signals corresponding to the intermediate binary number from N bit lines of the second RRAM crossbar array through N word lines of the third RRAM crossbar array, and encodes the intermediate binary number according to the voltage signals corresponding to the intermediate binary number and resistance values of resistors at the third RRAM crossbar array to obtain voltage signals corresponding to the second binary number.

14. The data processing apparatus according to claim 13, wherein the j^{th} word line of the third RRAM crossbar array is connected to the j^{th} bit line of the second RRAM crossbar array, and a resistance value of a resistor in the j^{th} row of the third RRAM crossbar array corresponds to a binary representation of the integer j+1.

15. The data processing apparatus according to claim 9, wherein the memory device comprises multiple memory units, each of the multiple memory units comprises a control circuit and a computation circuit, vector A is a row vector of a matrix Φ and vector B is a column vector of a matrix X, each of the multiple computation circuits in the memory device is set for performing point multiplication operations of a plurality of row vectors of the matrix Φ and a plurality of column vectors of the matrix X, and the multiple computation circuits jointly implement a matrix multiplication operation of the matrix Φ and the matrix X.

16. The data processing apparatus according to claim 9, wherein the instruction of the processor further comprises a data access instruction, and the memory unit further comprises:

a storage circuit, wherein the storage circuit is connected to the control circuit, and the control circuit read data from the computation circuit or write data into the computation circuit according to the data access instruction.

17. A computing device, comprising:

a processor configured to send a computation instruction;

a memory device connected to the processor, wherein the memory device comprising a

control bus and a memory unit connected to the control bus, the memory unit comprising a control circuit and a computation circuit;

wherein the computation circuit comprises a first resistive random access memory (RRAM) crossbar having multiple rows and multiple columns of memory cells, multiple word lines connected to respective rows of memory cells, and a plurality of comparator circuits each connected to a corresponding column of the first RRAM crossbar array, wherein the comparator circuits are set to have incremental thresholds;

wherein the control circuit is connected to the control bus and configured to:

receive the computation instruction for performing a vector multiplication of vector A and vector B;

setting the memory cells in the first RRAM crossbar array such that states of memory cells of each column of the first RRAM crossbar array correspond to elements of vector B;

setting the word lines of the first RRAM crossbar array according to elements of vector A;

wherein the outputs of the comparator circuits are voltage signals corresponding to a first binary number in which a number of bits with a value 1 indicates a numerical result of multiplication of vector A and vector B.

18. The computing device according to claim 17, wherein the computation circuit further comprises a second RRAM crossbar array and a third RRAM crossbar array each having multiple rows and multiple columns of memory cells and multiple word lines connected to respective rows of memory cells, wherein outputs of the comparator circuits are connected to corresponding word lines of the second RRAM crossbar array, outputs of the second RRAM crossbar array are connected to corresponding words lines of the third RRAM crossbar array, wherein

the second RRAM crossbar array being set up to convert the outputs of the comparator circuits into an output representing an intermediate binary number in which a location of a bit with a value 1 indicates the numerical result of multiplication of vector A and vector B; and

the third RRAM crossbar array being set up to convert the output of the second RRAM crossbar array into an output representing a second binary number having a numerical value equal to the numerical result of multiplication of vector A and vector B.

19. The computing device according to claim 18, wherein the multiple rows and multiple columns of memory cells in the first RRAM crossbar array comprise N rows × N columns resistors, an input end of a resistor in each row at the first RRAM crossbar array is connected to a word line, an output end of a resistor in each column at the first RRAM crossbar array is connected to a bit line, N word lines of the first RRAM crossbar array are connected to the control circuit, and each of N bit lines of the first RRAM crossbar array are respectively connected to a comparator circuit of the plurality of comparator circuits;

the first RRAM crossbar array generates N current signals on the N bit lines according to voltage signals input by the N word lines and a resistance value of a resistor at the first RRAM crossbar array, a voltage value of a voltage signal input by the j^{th} word line in the N word lines is a voltage value corresponding to B_j, a resistance value of a resistor in the j^{th} row at the first RRAM crossbar array is a resistance value corresponding to A_j, B_j is the j^{th} element of vector B, A_j is the j^{th} element of vector A, and a value of j ranges from 0 to N–1, wherein each of vector A and vector B indicates an N-dimensional vector, each elements of vector A and vector B indicates a value 1 or 0, and N is a positive integer not less than 2;

the N comparator circuits respectively convert the N current signals into N voltage signals, and compare the N voltage signals with voltage thresholds respectively corresponding to the N comparator circuits, to output, from output ends of the N comparator circuits, the voltage signals corresponding to the first binary number, wherein the first binary number is an N-dimensional vector, first K elements of the first binary number are 1, remaining elements are 0, and K is the result of multiplication of vector A and vector B;

the second RRAM crossbar array comprises a (2N–1) rows × N columns resistor array, an input end of a resistor in each row at the second RRAM crossbar array is connected to a word line, an output end of a resistor in each column at the second RRAM crossbar array is connected to a bit line, and each of word lines of the second RRAM crossbar array is connected to a output end of a comparator circuit in the first RRAM crossbar array;

the second RRAM crossbar array receives the voltage signals corresponding to the first binary number from the output ends of the comparator circuits of the first RRAM crossbar array through the 2N–1 word lines, and performs a logic operation according to the voltage signals corresponding to the first binary number and a resistance value of a resistor at the second RRAM

crossbar array:

$$\overline{O}_{2,j}=\begin{cases}\overline{O}_{1,j}+O_{1,j+1}, j<N-1\\ \overline{O}_{1,j}, j=N-1\end{cases}$$

to obtain voltage signals corresponding to an intermediate binary number, wherein $\overline{O}_{1,j}$ is a negation of a value corresponding to a voltage signal output by a comparator circuit connected to the j^{th} bit line of the first RRAM crossbar array, $O_{1,j+1}$ is a value corresponding to a voltage signal output by a comparator circuit connected to the $(j+1)^{th}$ bit line of the first RRAM crossbar array, and $\overline{O}_{2,j}$ is a negation of a value corresponding to a voltage signal output by the j^{th} bit line of the second RRAM crossbar array;

the third RRAM crossbar array comprises an N rows × n columns resistor array, an input end of a resistor in each row at the third RRAM crossbar array is connected to a word line, an output end of a resistor in each column at the third RRAM crossbar array is connected to a bit line, and n is greater than or equal to a minimum quantity of bits required for expressing the integer N in binary; and

the third RRAM crossbar array receives voltage signals corresponding to the intermediate binary number from N bit lines of the second RRAM crossbar array through N word lines of the third RRAM crossbar array, and encodes the intermediate binary number according to the voltage signals corresponding to the intermediate binary number and resistance values of resistors at the third RRAM crossbar array to obtain voltage signals corresponding to the second binary number.

20. The computing device according to claim 19, wherein the j^{th} comparator circuit in the N comparator circuits comprises a resistor R_s of a constant resistance value and a comparator, one end of the resistor R_s is connected to the j^{th} bit line in the N bit lines and the comparator, the other end of the resistor R_s is grounded, a voltage threshold of the j^{th} comparator circuit is $V_r*g_{on}*R_s*(2j+1)/2$, V_r indicates a voltage value corresponding to a value 1, and g_{on} indicates a reciprocal of R_{on}.