

DESCRIPTION

TITLE OF INVENTION

Information Processing Device and Communication Switching Method

5 TECHNICAL FIELD

[0001] The present disclosure relates to an information processing device and a communication switching method for switching a data bus, a control bus, and an interrupt bus.

BACKGROUND ART

10 [0002] Conventionally, there is a technique for switching a combination of a central processing unit (CPU) and a communication port in an information processing device including a plurality of CPUs and a plurality of communication ports (for example, see PTL 1). A CPU board assembly includes a carrier board that provides an external interface and one or two CPU boards mounted on the carrier board. For example, the
15 CPU board assembly is used for the following purposes (1), (2).

[0003] (1) Device control: a CPU board assembly includes one CPU board, and the CPU board needs two communication paths to communicate with a host device and each part in the device to be controlled.

(2) Signal processing: a CPU board assembly includes two CPU boards to
20 perform signal processing in parallel, and each CPU needs one communication path to transmit and receive processing data with the host device.

[0004] A CPU board includes two media access controls (MAC), which are local area network (LAN) controllers, as communication devices. Each LAN controller provides the communication function by being connected to a LAN connector through
25 a physical layer device that is a circuit included in the carrier board and on which a function of a physical layer (PHY) is implemented. Hereinafter, sometimes the physical layer device is simply referred to as a PHY.

[0005] In order to mount two CPU boards to use all MACs, the carrier board needs four PHY and LAN connectors. However, for the purpose of the above-described

device control and signal processing, the number of communication paths required on each CPU board assembly is two, and mounting more than three systems leads to an increase in size and cost of the device.

[0006] For this reason, desirably the number of these components is two. In this case,
5 the connection between the MAC of the CPU board and the PHY of the carrier board is different between the device control and the signal processing, so that one of the following two is required.

(a) Switch the connection between the MAC and the PHY according to purpose,
and

10 (b) Prepare two types of carrier boards having different connections between the MAC and the PHY according to the purpose. In contrast with (b), (a) is economical because only one type of carrier board is required. PTL 1 discloses a technique related to the switching between the CPU and the communication path.

CITATION LIST

15 PATENT LITERATURE

[0007] PTL 1: Japanese Patent Laying-Open No. 2012-14380

SUMMARY OF INVENTION

TECHNICAL PROBLEMS

[0008] The conventional technique described in PTL 1 provides a mechanism that
20 switches connections between two CPUs and external communication paths, but has a problem in that a mechanism that switches the connections of the following three buses is not mentioned. That is, the connection between the MAC and the PHY requires three types of buses of a data bus through which the communication data is transmitted and received, a control bus through which the MAC controls the PHY, and an interrupt
25 bus through which the CPU is notified interrupt from the PHY, and the change of the connection is required to switch these buses at the same time.

[0009] The present disclosure has been made to solve the above problems, and an object of the present disclosure is to provide an information processing device and a communication switching method for easily performing switching of data bus

connection, control bus connection, and interrupt bus connection at the same timing.

SOLUTION TO PROBLEM

[0010] An information processing device and a communication switching method according to an aspect of the present disclosure is featured by: switching a connection destination of a second physical layer device through a data bus (second data bus) to either a second LAN controller or a third LAN controller; switching a connection of a control bus such that either a first LAN controller or the third LAN controller accesses the second physical layer device according to the connection destination of the second physical layer device through the data bus (second data bus); and switching a connection of an interrupt bus according to the connection destination of the second physical layer device through the data bus (second data bus) to notify the first CPU that interrupt processing for the first CPU is transmitted from both the first physical layer device and the second physical layer device or only from the first physical layer device.

ADVANTAGEOUS EFFECTS OF INVENTION

[0011] As described above, according to the present disclosure, the information processing device and the communication switching method for easily performing the switching of data bus connection, the control bus connection, and the interrupt bus connection at the same timing can be obtained by performing the switching of control bus connection and the interrupt bus connection according to the connection destination of the second physical layer device through the second data bus.

BRIEF DESCRIPTION OF DRAWINGS

[0012] Fig. 1 is a functional block diagram illustrating an information processing device (CPU board assembly portion) according to a first embodiment.

Fig. 2 is a functional block diagram illustrating the information processing device (CPU board assembly portion) of the first embodiment.

Fig. 3 is a connection table of the information processing device (CPU board assembly portion) of the first embodiment.

Fig. 4 is a functional block diagram illustrating a data bus switching unit of the information processing device (CPU board assembly portion) of the first embodiment.

Fig. 5 is a functional block diagram illustrating a control bus switching unit of the information processing device (CPU board assembly portion) of the first embodiment.

5 Fig. 6 is a functional block diagram illustrating an interrupt bus switching unit of the information processing device (CPU board assembly portion) of the first embodiment.

Fig. 7 is a functional block diagram illustrating the interrupt bus switching unit of the information processing device (CPU board assembly portion) of the first embodiment.

10 Fig. 8 is a flowchart illustrating processing steps of the communication switching method of the first embodiment.

Fig. 9 is a functional block diagram illustrating the information processing device of the first embodiment.

DESCRIPTION OF EMBODIMENTS

15 [0013] Embodiment

Hereinafter, a first embodiment will be described with reference to Figs. 1 to 9. With reference to Figs. 1 to 7 and 9, an information processing device according to a first embodiment will be described. With reference to Figs. 8 and 9, a communication switching method of the first embodiment will be described. The information
20 processing device of the first embodiment means a CPU board assembly 100 or a device 110 in which a plurality of CPU board assemblies 100 are incorporated for device control and signal processing. That is, an information processing device 100 is provided when only CPU board assembly 100 is indicated, and an information
25 processing device 110 is provided when the plurality of CPU board assemblies 100 (for example, a CPU board assembly 101, a CPU board assembly 102) are incorporated for the device control and the signal processing.

[0014] In Figs. 1 to 9, a first CPU board 1 includes a first CPU 10, a first LAN controller 11 (first MAC 11), and a second LAN controller 12 (second MAC 12). A second CPU board 2 includes a second CPU 20 and a third LAN controller 21 (third

MAC 21). As illustrated in the drawing, the second CPU board 2 may include a fourth LAN controller 22 (fourth MAC 22).

[0015] In Figs. 1 to 9, a carrier board 3 includes a first physical layer device 30 (first PHY 30) that communicates with an outside, preferably a first LAN connector 31, a second physical layer device 32 (second PHY 32) that communicates with the outside, and preferably a second LAN connector 33. A switching unit 4 switches connection between: first CPU board 1 and second CPU board 2; and first physical layer device 30 and second physical layer device 32. Switching unit 4 includes a data bus switching unit 40, a control bus switching unit 41, and an interrupt bus switching unit 42.

Switching unit 4 may be included in the carrier board 3 as illustrated in the drawing. A first data bus 5 connects first physical layer device 30 to first LAN controller 11. A second data bus 6 connects second physical layer device 32 to either second LAN controller 12 or third LAN controller 21. A control bus 7 and an interrupt bus 8 will be described later.

[0016] Fig. 1 is a functional block diagram of the information processing device (CPU board assembly 100) of the first embodiment. Fig. 2 is a functional block diagram of the information processing device (CPU board assembly 100) of the first embodiment and illustrates an example of a preferred internal configuration of switching unit 4. CPU board assembly 100 includes two CPU boards, first CPU board 1 and second CPU board 2, and carrier board 3. That is, CPU board assembly 100 is configured by a combination of two types of boards of the CPU board (first CPU board 1 and second CPU board 2) and carrier board 3.

[0017] In the information processing device (CPU board assembly 100) of the first embodiment, the first CPU board 1 includes the CPU (first CPU 10) and the LAN controller (first MAC 11, second MAC 12) that controls LAN communication. The second CPU board 2 includes the CPU (second CPU 20) and the LAN controller (third MAC 21, fourth MAC 22) that controls the LAN communication. The carrier board 3 includes the physical layer device (first PHY 30, second PHY 32) that conducts LAN communication with the outside and the LAN connector (first LAN connector 31,

second LAN connector 33).

[0018] The first embodiment also includes the case where a combination of one carrier board 3 and one or more CPU boards (in the case of only first CPU board 1 described above) constitutes one CPU board assembly 100. In this case, that is, the case where
 5 second CPU board 2 is not installed will be described later. First, the case where CPU board assembly 100 in Figs. 1 and 2 is the combination of one carrier board 3 and two CPU boards (first CPU board 1, second CPU board 2) will be described as a representative example. Because each CPU board includes two MACs, and two CPU boards are installed on CPU board assembly 100 in Figs. 1 and 2, the number of LAN
 10 controllers (MAC) becomes four in total including first MAC 11, second MAC 12, third MAC 21, and fourth MAC 22. The carrier board 3 includes two sets (set of first PHY 30 and first LAN connector 31, set of second PHY 32 and second LAN connector 33) of the physical layer device and the LAN connector. Therefore, CPU board assembly 100 can conduct the LAN communication of up to two ports by connecting
 15 the LAN controller (MAC) of the CPU board and the physical layer device of carrier board 3.

[0019] In the information processing device (CPU board assembly 100) of the first embodiment, switching unit 4 is a circuit that connects a plurality of physical layer devices (PHY) that conducts the LAN communication with the outside to the LAN
 20 controller (MAC) that conducts the LAN communication with the outside through the physical layer device (PHY). Between the LAN controller and physical layer device (between MAC and PHY), there are three bus connections including a data bus (first data bus 5, second data bus 6) through which communication data is input and output, control bus 7 through which the physical layer device (first PHY 30, second PHY 32) is
 25 controlled, and interrupt bus 8 through which the physical layer device (first PHY 30, second PHY 32) requests interrupt processing from the CPU (first CPU 10, second CPU 20). In Figs. 1 and 2, the data bus (first data bus 5, second data bus 6) is indicated by a thick solid line, control bus 7 is indicated by a thin solid line as compared with the thick solid line, and interrupt bus 8 is indicated by a thin broken line

as compared with the thick solid line.

[0020] As illustrated in Figs. 1 and 2, switching unit 4 has a function of switching the connection between the total of three LAN controllers (MAC) of first MAC 11 and second MAC 12 of first CPU board 1 and third MAC 21 of second CPU board 2, and first PHY 30 or second PHY 32 of carrier board 3. Particularly, switching unit 4 controls switching the connection of second data bus 6, the connection of control bus 7, and the connection of interrupt bus 8 with reception of the identical selection signal as a trigger. With reference to the drawings, data bus switching unit 40, control bus switching unit 41, and interrupt bus switching unit 42 that are parts of switching unit 4 will be described below. Switching unit 4 can be included in carrier board 3.

[0021] In Fig. 2, data bus switching unit 40 switches the connection destination of second physical layer device 32 through second data bus 6 to either second LAN controller 12 or third LAN controller 21. Control bus switching unit 41 switches the connection of control bus 7 such that either first LAN controller 11 or third LAN controller 21 accesses second physical layer device 32 according to the connection destination of second physical layer device 32 through second data bus 6. Interrupt bus switching unit 42 switches the connection of interrupt bus 8 according to the connection destination of second physical layer device 32 through second data bus 6 to notify first CPU 10 that the interrupt processing for first CPU 10 is transmitted from both first physical layer device 30 and second physical layer device 32 or only from first physical layer device 30. The connection destination of second physical layer device 32 through second data bus 6, for example, is shown in a connection table illustrating a correspondence example of the connection between the LAN controller and the physical layer device (between the MAC and the PHY) and the selection signal in Fig. 3 to be described later.

[0022] In Fig. 2, particularly, switching unit 4 includes data bus switching unit 40 that switches the connection of second data bus 6 between a CPU-side data port 34 and a physical layer side data bus 35, control bus switching unit 41 that switches the connection of control bus 7 between a CPU-side control port 36 and a physical layer-

side control bus 37, and interrupt bus switching unit 42 that switches the connection of interrupt bus 8 between a CPU-side interrupt port 38 and a physical layer-side interrupt bus 39. Some configurations of the port and the bus are also illustrated in Fig. 1.

[0023] As illustrated in the drawing, the information processing device (CPU board assembly 100) of the first embodiment may further include a switching controller 9 that generates the selection signal. That is, the information processing device (CPU board assembly 100) of the first embodiment may include switching controller 9 and signal lines for the selection signal for selecting the connection destination for three of data bus switching unit 40, control bus switching unit 41, and interrupt bus switching unit 42. Switching controller 9 outputs a selection signal according to an instruction from first CPU 10, and notifies (instructs) each switching unit (data bus switching unit 40, control bus switching unit 41, interrupt bus switching unit 42) of the switching of the connection between the LAN controller and the physical layer device (between the MAC and the PHY). For example, it is conceivable that switching controller 9 transmits the selection signal to switching unit 4 as a first signal or a second signal. In the present application, the first signal is “0”, and the second signal is “1”.

[0024] Switching controller 9 generates the selection signal of “0” or “1” (first signal or second signal) according to the instruction (instruction signal) from first CPU 10. In Fig. 2, the flow of the instruction signal is indicated by a thin dotted line (from first CPU 10 to switching controller 9) as compared with the thick solid line of the data bus. That is, it can be said that the thin dotted line has a finer pitch than the thin broken line indicating interrupt bus 8 in Fig. 2. In Fig. 2, the thin dotted line from switching controller 9 to data bus switching unit 40 indicates the selection signal sent from switching controller 9 to data bus switching unit 40, the thin dotted line from switching controller 9 to control bus switching unit 41 indicates the selection signal sent from switching controller 9 to control bus switching unit 41, and the thin dotted line from switching controller 9 to interrupt bus switching unit 42 indicates the selection signal sent from switching controller 9 to interrupt bus switching unit 42.

[0025] Fig. 3 is a connection table illustrating a correspondence example of the

connection between the LAN controller and the physical layer device (between the MAC and the PHY) and the selection signal. In the table of Fig. 3, a row indicates the LAN controller (MAC), and a column indicates the selection signal. Fig. 3 shows a correspondence example of the connection destination and the connection status.

5 Switching controller 9 may be included in carrier board 3 as illustrated in the drawing. Of course, at least one of switching unit 4 and switching controller 9 may be included in carrier board 3.

[0026] The details are as follows. When first CPU board 1 uses two LAN communication ports, namely, when first MAC 11 and second MAC 12 of first CPU board 1 are connected to first PHY 30 and second PHY 32, respectively, switching controller 9 outputs the selection signal “0” (first signal). On the other hand, when one LAN communication port is used for each of first CPU board 1 and the second CPU board 2, namely, when first MAC 11 and first PHY 30 of first CPU board 1 are connected and third MAC 21 and second PHY 32 of second CPU board 2 are connected, switching controller 9 outputs the selection signal “1” (second signal).

[0027] For example, in addition to the communication through the LAN between first CPU board 1 and second CPU board 2, a communication path through which CPUs (the first CPU 10 and the second CPU 20) can communicate with each other is provided on carrier board 3, and first CPU 10 checks whether second CPU board 2 is installed by using a method such as a method in which first CPU 10 accesses second CPU 20 through the communication path. In this manner, first CPU 10 checks whether second CPU board 2 is installed, first CPU 10 selects 0 as the selection signal when second CPU board 2 is not installed, and enables first CPU board 1 to use all the LAN communication ports. First CPU 10 selects “1” as the selection signal when second CPU board 2 is installed, and enables both first CPU board 1 and second CPU board 2 to use one LAN communication port. This combination may be another combination according to the purpose. That is, when it is checked that second CPU board 2 is installed, the selection signal “0” or the selection signal “1” may be generated as necessary.

[0028] In other words, the information processing device (CPU board assembly 100) of the first embodiment includes first CPU board 1, carrier board 3, and switching unit 4 that switches the connection between "first CPU board 1 and the external board (selectable implementation and non-implementation)" and "first PHY 30 and the second PHY 32". First PHY 30 is connected to first MAC 11 through first data bus 5. When second CPU board 2 is installed as an external board, the operation of switching unit 4 (data bus switching unit 40, control bus switching unit 41, interrupt bus switching unit 42) described above is performed. Of course, also in this configuration, the information processing device (CPU board assembly 100) may include switching controller 9.

[0029] Data bus switching unit 40, control bus switching unit 41, and interrupt bus switching unit 42, which switch connections of three buses, will be described below. Data bus switching unit 40, control bus switching unit 41, and interrupt bus switching unit 42 switch the connections of the respective buses, second data bus 6, control bus 7, and interrupt bus 8, according to Fig. 3, by the selection signals from switching controller 9.

[0030] Fig. 4 illustrates a configuration of data bus switching unit 40. The first data bus 5 may be formed outside of data bus switching unit 40. As illustrated in Fig. 4, data bus switching unit 40 causes data bus switch 400 to connect the second physical layer device 32 to second LAN controller 12 via the second data bus 6 when receiving the selection signal "0" (first signal), and data bus switching unit 40 causes data bus switching unit 400 to connect the second physical layer device 32 to third LAN controller 21 via second data bus 6 through the data bus switch 400 when receiving the selection signal "1" (second signal). Data bus switch 400 does not operate when being disposed on a desired side at the time of receiving the selection signal, but for convenience, this is also included in the switching.

[0031] Furthermore, data bus switching unit 40 may improve signal quality by a buffer 401 in addition to the switching of the connection corresponding to Fig. 3 by the selection signal. When a communication speed of the LAN communication exceeds 1

Gbps, high-speed serial transmission using a differential signal is generally used for data bus (first data bus 5, second data bus 6) because of fast data communication. At this point, the CPU board (first CPU board 1, second CPU board 2) and carrier board 3 are connected through the connector, and the connections of busses are switched by the switch, so that the signal quality may be degraded. Accordingly, as illustrated in Fig. 4, in data bus switching unit 40, buffers 401 are inserted into the data bus (first data bus 5, second data bus 6) to improve the signal degraded due to a MAC-PHY connector and a changeover switch, so that the signal quality can be improved. Buffers 401 inserted in first data bus 5 may be formed outside of data bus switching unit 40 together with first data bus 5.

[0032] Fig. 5 illustrates the configuration of control bus switching unit 41. As illustrated in Fig. 5, control bus switching unit 41 switches a control bus switch 403 and a control bus switch 404 among the three bus switches such that first LAN controller 11 accesses second physical layer device 32 when receiving the selection signal “0 ” (first signal), and control bus switching unit 41 switches control bus switch 403 and control bus switch 404 among the three bus switches such that third LAN controller 21 accesses second physical layer device 32 when receiving the selection signal “ 1 ” (second signal). In any case, to make a control bus switch 402 always selected, “1” is input to the enable signal input port of the control bus switch 402 without connecting the selection signal.

[0033] As illustrated in Fig. 5, control bus 7 is a bus that is used to control the operation of the PHY through which first CPU 10 (via the first MAC11) or second CPU20 (via the second MAC 21) operates register of the PHY (first PHY 30, second PHY 32), and second PHY 32 is accessed from either first CPU board 1 or second CPU board 2 in response to the switching. Control bus switches 402, 403, 404, that are previously mentioned, are used for switching connection of control bus 7, and the switching is performed by exclusively selecting either control bus switch 403 or the control bus switch 404.

[0034] These control bus switches 402, 403, 404 comprise a voltage conversion

function and have open drain circuits. Accordingly, I/O voltage may be different between the CPU board (first CPU board 1, second CPU board 2) and carrier board 3. Because of the open drain circuits, the control bus signal after the switching can be set to wired-OR and connected to second PHY 32. The wired-OR is a logical OR

5 obtained by connecting a plurality of output signals.

[0035] Figs. 6 and 7 illustrate the configuration of interrupt bus switching unit 42.

The configuration of Fig. 7 will be described later. As illustrated in Fig. 6, when receiving the selection signal “0” (first signal), interrupt bus switching unit 42 controls interrupt bus switch 405 to notify first CPU 10 that the interrupt signal to first CPU 10 is sent by both first physical layer device 30 and second physical layer device 32, and when receiving the selection signal “1” (second signal), interrupt bus switching unit 42 controls interrupt bus switch 405 to notify first CPU 10 that the interrupt signal to first CPU 10 is sent by only first physical layer device 30. The fact that the interrupt signal to first CPU 10 is only from first physical layer device 30 means that there is no interrupt signal to first CPU 10 from second physical layer device 32, but does not mean that the interrupt signal to first CPU 10 from devices other than second physical layer device 32 is limited to those from first physical layer device 30.

[0036] The interrupt signal to second CPU 20 is sent only through second physical layer device 32, but interrupt bus switching unit 42 notifies second CPU 20 that the interrupt signal is not sent because the second data bus is not connected when receiving the selection signal “0” (first signal). On the other hand, interrupt bus switching unit 42 notifies second CPU 20 that the interrupt signal is sent because the second data bus is connected when receiving the selection signal “1” (second signal). Of course, when the interrupt signal is not sent, it is also conceivable that no notification is made.

25 [0037] Figs. 6 and 7 illustrate examples of the configuration of interrupt bus switch 405, Fig. 7 is a different configuration example of interrupt bus switching unit 42, and the interrupt bus switching unit 42 may be configured as illustrated in Fig. 7. In Fig. 6, the logical OR of the interrupt signals from the plurality of PHYs (first PHY 30, second PHY 32) is switched, but in Fig. 7, the logical OR of the switched signals is

output to the CPU (first CPU, second CPU).

[0038] Interrupt bus 8 is used such that the PHY (first PHY 30, second PHY 32) notifies the CPU (first CPU 10, second CPU 20) of the change in the connection state of the cable connected to the LAN connector (first LAN connector 31, second LAN connector 33) and requests the CPU to perform the interrupt processing according to the change. For example, when the CPU (first CPU 10, second CPU 20) is notified that the cable is connected, the CPU (first CPU 10, second CPU 20) sets itself such that the communication can be started. When the selection signal is set to "0" in Fig. 3, in order to notify first CPU 10 of the interruption of both first PHY 30 and second PHY 32, instead of switching, the logical OR of the interrupt signal from first PHY 30 and the interrupt signal from second PHY 32 is used.

[0039] In the present application, it is assumed that the interruption detection includes periodical process performed at a predetermined period in addition to occasional process. That is, the interruption detection of the present application may be replaced with polling process. The polling process may be simply referred to as polling. Therefore, interrupt bus 8, a CPU-side interrupt port 38, a physical layer-side interrupt bus 39, and an interrupt bus switch 45 can be replaced with a polling bus 8, a CPU-side polling port 38, a physical layer-side polling bus 39, and a polling bus switch 45, respectively.

[0040] With reference to Fig. 8, a communication switching method of the first embodiment will be described. The communication switching method of the first embodiment is a method related to the operation (processing step) of switching unit 4 or the operation of switching unit 4 and switching controller 9 (including first CPU 10 in some cases) of the information processing device of the first embodiment. For this reason, the description of the communication switching method of switching unit 4 or switching unit 4 and switching controller 9 (including first CPU 10 in some cases), described in the first embodiment of the information processing device, may be omitted from a description of a second embodiment. Furthermore, a content described in the information processing device of the first embodiment can also be applied to the

communication switching method of the first embodiment.

[0041] That is, it can be said that the communication switching method of the first embodiment switches the connection between "first CPU board 1 and second CPU board 2" and "first PHY 30 and second PHY 32". Processing steps in the flowchart of Fig. 8 indicate basic processing steps of the communication switching method of the first embodiment, a data bus switching step (STEP 11), a control bus switching step (STEP 12), and an interrupt bus switching step (STEP 13). The communication switching method of the first embodiment is characterized in that the data bus switching step, the control bus switching step, and the interruption bus switching step are triggered by the same trigger processing step. The trigger processing step is described as STEP 1 in Fig. 8. In the trigger processing step an information (switching information about second LAN controller 12 and third LAN controller 21) is indicated whether the connection destination of second physical layer device 32 through second data bus 6 is second LAN controller 12 or third LAN controller 21. Acquisition or determination of the switching information serves as the trigger processing step.

[0042] Although not illustrated, the communication switching method of the first embodiment may preferably include a installing check step (STEP 0) and a switching control step (STEP 1). The installing check step and the switching control step will be described after the description of the basic processing steps in Fig. 8. The switching control step (STEP 1) is an example of the trigger processing step in Fig. 8, and thus has the same processing step name of STEP 1.

[0043] In Fig. 8, the data bus switching step is a processing step in which data bus switching unit 40 switches the connection destination (Fig. 3) of second PHY 32 through second data bus 6 to either second MAC 12 or third MAC 21. The control bus switching step is a processing step in which control bus switching unit 41 switches the connection of control bus 7 such that either first MAC 11 or third MAC 21 accesses second PHY 32 according to the connection destination (Fig. 3) of second PHY 32 through second data bus 6. The interrupt bus switching step is a processing step in

which interrupt bus switching unit 42 switches the connection of interrupt bus 8 according to the connection destination (Fig. 3) of second PHY 32 through second data bus 6 to notify first CPU 10 that the interrupt processing for first CPU 10 is transmitted from both first PHY 30 and second PHY 32 or only from first PHY 30. The interrupt processing for second CPU 20 is as described in the description about interrupt bus switching unit 42 of the information processing device of the first embodiment.

[0044] In the communication switching method of the first embodiment, a switching control step will be described as an example of the trigger processing step for executing the data bus switching step, the control bus switching step, and the interrupt bus switching step with the same trigger. The switching control step corresponds to the processing steps preceding STEP 11, STEP 12, STEP 13, and thus can be said to be STEP 1. That is, in the switching control step, switching controller 9 generates the first signal and the second signal (selection signal) that are the trigger for determining the connection destination in the data bus switching step at the timing before the execution of the data bus switching step, the control bus switching step, and the interrupt bus switching step. Particularly, in the switching control step, switching controller 9 generates the first signal that is the instruction for second data bus 6 to set second PHY 32 and second MAC 12 to the connected state or the second signal that is the instruction for second data bus 6 to set second PHY 32 and the third MAC 21 to the connected state.

[0045] The communication switching method of the first embodiment may further include the installing check step (STEP 0) in which first CPU 10 checks whether second CPU board 2 is installed at the timing before the switching control step (STEP 1). Because the installing check step is a processing step before the switching control step and is a previous step of the switching, it can be said as STEP 0. Because the installing check step checks whether second CPU board 2 is installed, in the switching control step, only the first signal (selection signal "0") may be generated when it is checked that second CPU board 2 is not installed in the installing check step. On the other hand, when the installing check step checks that second CPU board 2 is installed,

in the switching control step the first signal (selection signal “0”) or the second signal (selection signal “1”) may be generated as necessary.

[0046] As described above, the three buses of second data bus 6, control bus 7, and interrupt bus 8 that are required for the communication between the MAC (LAN controller) and the PHY (physical layer device) can be easily and simultaneously switched by the information processing device (switching unit 4) and the communication switching method of the first embodiment. Even when the combination of the CPU board (first CPU board 1, second CPU board 2) and carrier board 3 is recombined according to the purpose, the LAN communication port can be efficiently used. The hardware configuration can be implemented as necessary by making the number of CPU boards variable, such as installing two CPU boards when a large amount of processing performance is required and installing one CPU board when a large amount of processing performance is not required. With reference to Fig. 9, details will be described.

[0047] Fig. 9 is an example of a CPU board assembly 110 (CPU board assembly 101, CPU board assembly 102) that is a signal processing device to which the information processing device (communication switching method) of the first embodiment is applied. In Fig. 9, CPU board assembly 101 is CPU board assembly 100 itself. CPU board assembly 102 corresponds to CPU board assembly 101 (CPU board assembly 100) on which second CPU board 2 is not installed (not implemented). A switching hub 103 connects CPU board assembly 101 with CPU board assembly 102 to enable them to communicate with each other, and performs communication relay. Switching hub 103 is connected to first LAN connector 31 of CPU board assembly 101, second LAN connector 33 of CPU board assembly 101, and second LAN connector 33 of CPU board assembly 102. First LAN connector 31 of CPU board assembly 102 is connected to a host device.

[0048] As described above, what is illustrated in Fig. 9 is an example of information processing device 110, and includes two types of information processing device 110 of device control CPU board assembly 102 on which one CPU board (first CPU board 1)

is installed and signal processing CPU board assembly 101 on which two CPU boards (first CPU board 1, second CPU board 2) are installed. In device control CPU board assembly 102, one CPU (first CPU 10) performs two LAN communications, namely, the communication with the host device and the communication with signal processing CPU board assembly 101. Signal processing CPU board assembly 101 performs the signal processing with two CPUs (first CPU 10, second CPU 20), and transmits a processing result from each CPU board (first CPU board 1, second CPU board 2) to device control CPU board assembly 102 through switching hub 103 by the LAN communication.

[0049] The configuration of Fig. 9 can be implemented only by two types of boards of the CPU board (first CPU board 1, second CPU board 2) and carrier board 3 and switching unit 4, so that the configuration of Fig. 9 can be implemented at low cost as compared with the case where device control CPU board assembly 102 and signal processing CPU board assembly 101 are separately prepared. Except for buffer 401 used for the data bus (first data bus 5, second data bus 6), the circuit constituting switching unit 4 can be implemented in a small number of additional components using a programmable logic such as a field-programmable gate array (FPGA) with other functions of the carrier board. Buffer 401 used for the data bus (first data bus 5, second data bus 6) may also be implemented in a general integrated circuit (IC) compatible with high-speed serial transmission.

[0050] As described above, according to the information processing device and the communication switching method of the first embodiment, the carrier board having the switching unit that simultaneously switches the connections of the three buses required for the communication between the MAC (LAN controller) and the PHY (physical layer device) is provided, and the connection between the MAC (LAN controller) and the PHY (physical layer device) is switched according to the number of installed CPU boards, thereby implementing the optimal configuration of the LAN communication port according to the CPU board assembly. Thus, preparation of two types of carrier boards having different connections between the MAC (LAN controller) and the PHY

(physical layer device) according to the purpose is not required, so that, the cost reduction of the device can be achieved. The information processing device and the communication switching method of the first embodiment relate to the switching of the connection between the MAC and the PHY according to the purpose as described above, and the three types of buses between the MAC and the PHY are easily and simultaneously switched.

REFERENCE SIGNS LIST

- [0051] 1: first CPU board
- 10: first CPU
- 10 11: first LAN controller (first MAC)
- 12: second LAN controller (second MAC)
- 2: second CPU board
- 20: second CPU, 21: third LAN controller (third MAC)
- 22: fourth LAN controller (fourth MAC)
- 15 3: carrier board
- 30: first physical layer device (first PHY)
- 31: first LAN connector
- 32: second physical layer device (second PHY)
- 33: second LAN connector
- 20 34: CPU-side data port
- 35: physical layer-side data bus
- 36: CPU-side control port
- 37: physical layer-side control bus
- 38: CPU-side interrupt port
- 25 39: physical layer-side interrupt bus
- 4: switching unit
- 40: data bus switching unit
- 41: control bus switching unit
- 42: interrupt bus switching unit

	400: data bus switch
	401: buffer
	402: control bus switch (bus switch)
	403: control bus switch (bus switch)
5	404: control bus switch (bus switch)
	405: interrupt bus switch
	5: first data bus
	6: second data bus
	7: control bus
10	8: interrupt bus
	9: switching controller
	100: CPU board assembly
	101: CPU board assembly
	102: CPU board assembly
15	103: switching circuit
	110: signal processing device

CLAIMS

1. An information processing device comprising:
 - a first CPU board including a first CPU, a first LAN controller, and a second
 - 5 LAN controller;
 - a second CPU board including a second CPU and a third LAN controller;
 - a carrier board including a first physical layer device that communicates with an outside and a second physical layer device that communicates with the outside; and
 - a switching unit to switch connection between: the first CPU board and the
 - 10 second CPU board; and the first physical layer device and the second physical layer device,
 - wherein the first physical layer device is connected to the first LAN controller through a first data bus,
 - the switching unit includes:
 - 15 a data bus switching unit that switches a connection destination of the second physical layer device through the second data bus to either the second LAN controller or the third LAN controller;
 - a control bus switching unit that switches a connection of a control bus such that either the first LAN controller or the third LAN controller accesses the second
 - 20 physical layer device through the control bus according to the connection destination of the second physical layer device through the second data bus; and
 - an interrupt bus switching unit that switches a connection of an interrupt bus such that according to the connection destination of the second physical layer device through the second data bus to notify the first CPU that interrupt processing for the first
 - 25 CPU is transmitted from both the first physical layer device and the second physical layer device or only from the first physical layer device, and
 - the switching unit controls switching connections of the second data bus, the control bus, and the interrupt bus with reception of a selection signal as a trigger, the selection signal being identical.

2. An information processing device comprising:

a first CPU board including a first CPU, a first LAN controller, and a second LAN controller;

5 a carrier board including a first physical layer device that communicates with an outside and a second physical layer device that communicates with the outside; and

a switching unit to switch connection between: the first CPU board and an external board; and the first physical layer device and the second physical layer device,

wherein the first physical layer device is connected to the first LAN controller through a first data bus,

10 the switching unit includes a data bus switching unit, a control bus switching unit, and an interrupt bus switching unit,

when a second CPU board including a second CPU and a third LAN controller is installed as the external board,

15 the data bus switching unit switches a connection destination of the second physical layer device through the second data bus to either the second LAN controller or the third LAN controller,

the control bus switching unit switches a connection of a control bus such that either one of the first LAN controller or the third LAN controller accesses the second physical layer device according to the connection destination of the second physical layer device through the second data bus,

20 the interrupt bus switching unit switches a connection of an interrupt bus according to the connection destination of the second physical layer device through the second data bus to notify the first CPU that interrupt processing for the first CPU is transmitted from both the first physical layer device and the second physical layer device or only from the first physical layer device, and

25 the switching unit controls switching connections of the second data bus, the control bus, and the interrupt bus with reception of a selection signal as a trigger, the selection signal being identical.

3. The information processing device according to claim 1 or 2, further comprising a switching controller to generate the selection signal,
wherein the switching controller transmits the selection signal to the switching
5 unit as a first signal or a second signal.

4. The information processing device according to claim 3, wherein the data bus switching unit causes a data bus switch to connect the second physical layer device and the second LAN controller through the second data bus when receiving the first
10 signal, and the data bus switching unit causes the data bus switch to connect the second physical layer device and the third LAN controller through the second data bus when receiving the second signal.

5. The information processing device according to claim 3 or 4, wherein the
15 control bus switching unit switches the connection of the control bus such that the first LAN controller accesses the second physical layer device when receiving the first signal, and the control bus switching unit switches the connection of the control bus such that the third LAN controller accesses the second physical layer device when receiving the second signal.

20 6. The information processing device according to any one of claims 3 to 5, wherein the interrupt bus switching unit controls an interrupt bus switch to notify the first CPU that the interrupt processing for the first CPU is transmitted from both the first physical layer device and the second physical layer device when receiving the first
25 signal, and the interrupt bus switching unit controls the interrupt bus switch to notify the first CPU that the interrupt signal for the first CPU is transmitted from only the first physical layer device when receiving the second signal.

7. The information processing device according to any one of claims 3 to 6,

wherein the switching controller generates the selection signal according to an instruction from the first CPU.

8. The information processing device according to any one of claims 3 to 7,
5 wherein at least one of the switching unit and the switching controller is included in the carrier board.

9. A communication switching method for switching connection between: a
first CPU board including a first CPU, a first LAN controller, and a second LAN
10 controller and a second CPU board including a second CPU and a third LAN
controller; and a first physical layer device that communicate with an outside and a
second physical layer device that communicates with the outside,
the communication switching method comprising:
switching a connection destination of the second physical layer device through
15 the second data bus to either the second LAN controller or the third LAN controller;
switching a connection of a control bus such that either the first LAN controller
or the third LAN controller accesses the second physical layer device according to the
connection destination of the second physical layer device through the second data bus;
and
20 switching a connection of an interrupt bus according to the connection
destination of the second physical layer device through the second data bus to notify
the first CPU that interrupt signal for the first CPU is transmitted from both the first
physical layer device and the second physical layer device or only from the first
physical layer device,
25 wherein the switching the connection of the data bus, the switching the
connection of the control bus, and the switching the connection of the interruption bus
are performed with a trigger, the trigger being identical.

10. The communication switching method according to claim 9, further

comprising generating a first signal and a second signal that are the trigger for determining the connection destination in the switching the connection of the second data bus at timing before execution of the switching the connection of the second data bus, the switching the connection of the control bus, and the switching the connection
5 of the interrupt bus,

wherein the first signal that is an instruction to bring the second physical layer device and the second LAN controller into a connected state through the second data bus or the second signal that is an instruction to bring the second physical layer device and the third LAN controller into the connected state through the second data bus is
10 generated in the switching control.

11. The communication switching method according to claim 10, further comprising checking whether the second CPU board is installed at timing before the switching control,

15 wherein only the first signal is generated in the switching control when it is confirmed in the installing confirmation that the second CPU board is not installed.