PLASMA PROCESSING APPARATUS AND PLASMA PROCESSING METHOD

Cross-Reference to Related Applications

This application claims priority to Japanese Patent Application No. 2017-177398, filed on September 15, 2017, the entire contents of which are incorporated herein by reference.

Field of the Invention

The present disclosure relates to a plasma processing apparatus and a plasma processing method.

Background of the Invention

In a semiconductor device manufacturing process, a plasma processing apparatus for performing processing such as etching or the like on a target substrate, e.g., a semiconductor wafer, by applying the plasma of a processing gas to the target substrate, is used. In the plasma processing apparatus, a target substrate is mounted on a central portion of an electrostatic chuck provided on a base (susceptor), and a focus ring is provided on an outer peripheral portion of the electrostatic chuck to surround the target substrate. The focus ring improves the

uniformity of the plasma processing such as etching or the like performed on the target substrate. A high frequency bias power for attracting ions in plasma may be applied to the target substrate.

In the semiconductor device manufacturing process, when high aspect ratio etching is performed on a semiconductor wafer, a phenomenon (tilting) in which a contact hole is inclined in a region of the wafer (e.g., a peripheral region of the wafer) may occur. This results in a decrease in yield.

Therefore, there is known a plasma processing apparatus in which a focus ring has a plurality of flat portions having different heights. By using the focus ring having a plurality of flat portions with different heights, tilting on the target substrate is suppressed (see, e.g., Japanese Patent Application Publication No. 2016-225588).

However, the above-described technique does not take into consideration suppressing the tilting that occurs on the target substrate during plasma processing that involves the changing of the magnitude of bias power.

It is generally known that when the magnitude of the bias power changes from a relatively low value to a relatively high value, for example, the height relation between a plasma sheath above the target substrate and that above the focus ring generally depends on a difference between the impedance between the target substrate and the

base and the impedance between the focus ring and the base. If there is a difference between the electrostatic capacitance of the central portion of the electrostatic chuck and the electrostatic capacitance of the outer peripheral portion of the electrostatic chuck, the impedance between the target substrate and the base is not matched with the impedance between the focus ring and the base. If the impedance between the target substrate and the base is not matched with the impedance between the focus ring and the base, the height relation between the plasma sheath above the target substrate and the plasma sheath above the focus ring tends to vary. As a result, variation in the inclination of an incidence angle of particles such as the ions in the plasma on the target substrate is increased, which makes it difficult to suppress the variation in the inclination of the hole formed in the target substrate within predetermined specifications. In this specification, the electrostatic capacitance indicates the electrostatic capacitance per unit area.

In the plasma processing apparatus using the focus ring having a plurality of flat portions having different heights, when the magnitude of the bias power is changed, the height relation between the plasma sheath above the target substrate and the plasma sheath above the focus ring may vary and the inclination of the hole formed in the target substrate may vary greatly. Therefore, it is desired

to suppress the tilting on the target substrate in the plasma processing that involves changing the magnitude of the bias power.

Summary of the Invention

In accordance with an aspect, there is provided a plasma processing apparatus including: a base to which a bias power, whose magnitude is changed during plasma processing on a target substrate, is applied; an electrostatic chuck, provided on the base, having a central portion on which the target substrate is mounted and an outer peripheral portion on which a focus ring is mounted to surround the target substrate; and a dielectric layer, provided between the outer peripheral portion of the electrostatic and the base or the focus ring, having an electrostatic capacitance that reduces a difference between an electrostatic capacitance of the central portion of the electrostatic chuck and an electrostatic capacitance of the outer peripheral portion of the electrostatic chuck.

In accordance with another aspect, there is provided a plasma processing apparatus including: a base to which a bias power, whose magnitude is changed during plasma processing on a target substrate, is applied; an electrostatic chuck, provided on the base, having a central portion on which the target substrate is mounted and an

outer peripheral portion on which a focus ring is mounted to surround the target substrate; and a dielectric layer, provided between the outer peripheral portion of the electrostatic and the base or the focus ring, having an electrostatic capacitance per unit area which reduces a difference between an electrostatic capacitance per unit area of the central portion of the electrostatic chuck and an electrostatic capacitance per unit area of the outer peripheral portion of the electrostatic chuck.

In accordance with still another aspect, there is provided a plasma processing method for performing plasma processing on a target substrate by using the plasma processing apparatus described above.

Brief Description of the Drawings

The objects and features of the present disclosure will become apparent from the following description of embodiments, given in conjunction with the accompanying drawings, in which:

Fig. 1 is a cross sectional view showing a schematic configuration of a plasma processing apparatus according to an embodiment;

Fig. 2 is an enlarged cross sectional view showing a base, an electrostatic chuck, a wafer and a focus ring;

Fig. 3 shows an example of an equivalent circuit in

the vicinity of the electrostatic chuck in the case where a dielectric layer is not disposed between an outer peripheral portion of the electrostatic chuck and the base;

Fig. 4 shows an example of an equivalent circuit in the vicinity of the electrostatic chuck in the case where a dielectric layer is disposed between the outer peripheral portion of the electrostatic chuck and the base;

Fig. 5 shows another example of the equivalent circuit in the vicinity of the electrostatic chuck in the case where a dielectric layer is disposed between the outer peripheral portion of the electrostatic chuck and the base;

Fig. 6 shows a modified arrangement of a dielectric layer;

Fig. 7 shows an exemplary measurement result of the relation between the magnitude of bias power and the inclination angle of a hole;

Fig. 8 shows a simulation result of the temperature distribution of a focus ring in a plasma processing apparatus (comparative example) in which a dielectric layer is not disposed between the outer peripheral portion of the electrostatic chuck and the base; and

Fig. 9 shows a simulation result of the temperature distribution of a focus ring in a plasma processing apparatus (test example) in which a dielectric layer is disposed between the outer peripheral portion of the electrostatic chuck and the base.

Detailed Description of the Embodiments

Hereinafter, embodiments will be described in detail with reference to the accompanying drawings. Like reference numerals will be given to like or corresponding parts throughout the drawings.

(Configuration of plasma processing apparatus)

Fig. 1 is a cross sectional view showing a schematic configuration of a plasma processing apparatus 1 according to an embodiment. The plasma processing apparatus 1 shown in Fig. 1 is configured as, e.g., a plasma etching apparatus using a capacitively coupled plasma (CCP).

Referring to Fig. 1, the plasma processing apparatus 1 includes a cylindrical processing chamber 10 made of a metal, e.g., aluminum or stainless steel. The processing chamber 10 is frame grounded. A disc-shaped base (susceptor) 11 is provided in the processing chamber 10. The base 11 is made of, e.g., aluminum, and is supported by a tubular support 13 extending vertically upward from a bottom portion of the processing chamber 10 via an insulating cylindrical holding member 12. The base 11 serves as a lower electrode.

A gas exhaust path 14 is formed between a sidewall of the processing chamber 10 and the cylindrical support 13. An annular baffle plate 15 is provided at an inlet of the gas exhaust path 14 or in the gas exhaust path 14. A gas

exhaust port 16 is provided at a bottom portion of the processing chamber 10. A gas exhaust unit 18 is connected to the gas exhaust port 16 through a gas exhaust line 17. The gas exhaust unit 18 includes a vacuum pump, and reduces the pressure in the processing space in the processing chamber 10 to a predetermined vacuum level. The gas exhaust line 17 has an automatic pressure control valve (hereinafter, referred to as "APC") (not shown) that is a variable butterfly valve. The APC automatically controls a pressure in the processing chamber 10. A gate valve 20 for opening/closing a loading/unloading port 19 for the wafer W is provided at the sidewall of the processing chamber 10.

A high frequency power supply 22a is electrically connected to the base 11 serving as the lower electrode via a matching unit 21a. A high frequency power supply 22b is electrically connected to the base 11 via a matching unit 21b. The high frequency power supply 22a is a power supply for plasma generation and applies a high frequency power having a predetermined high frequency to the base 11. The high frequency power supply 22b is a power supply for ion attraction and applies a high frequency power having a frequency lower than that of the high frequency power of the high frequency power supply 22a to the base 11. The high frequency power applied from the high frequency power supply 22b to the base 11 is a high frequency power for attracting ions in plasma to the wafer W that is an example of the

target substrate and also referred to as "bias power". The high frequency power supply 22b switches a magnitude of the bias power between a relatively low value and a relatively high value in response to an instruction from a control unit 43 during the plasma processing on the wafer W.

A shower head 24 serving as an upper electrode having a ground potential, which will be described later, is provided at a ceiling portion of the processing chamber 10. Accordingly, a high frequency voltage from the high frequency power supply 22a is applied to a space between the base 11 and the shower head 24.

An electrostatic chuck 25 for attracting and holding the wafer W by an electrostatic attraction force is provided on an upper surface of the base 11. The electrostatic chuck 25 has a disc-shaped central portion 25a and an annular outer peripheral portion 25b. The wafer W is mounted on the central portion 25a, and a focus ring 30 is mounted on the outer peripheral portion 25b to surround the wafer W. The central portion 25a protrudes upward in the drawing with respect to the outer peripheral portion 25b. The central portion 25a is thicker than the outer peripheral portion 25b. The central portion 25a is formed by embedding an electrode plate 25c made of a conductive film between two dielectric films. The outer peripheral portion 25b is formed by embedding an electrode plate 25d made of a conductive film between two dielectric films. A DC power supply 26 is

electrically connected to the electrode plate 25c through a switch 27. DC power supplies 28-1 and 28-2 are electrically connected to the electrode plate 25d through switches 29-1 and 29-2, respectively. An electrostatic attraction force such as Coulomb force or the like is generated by the voltage applied from the DC power supply 26 to the electrode plate 25c, and the wafer W is attracted to and held on the electrostatic chuck 25 by the electrostatic attraction force. Further, an electrostatic attraction force such as Coulomb force or the like is generated by the voltage applied from the DC power supplies 28-1 and 28-2 to the electrode plate 25d, and the focus ring 30 is attracted to and held on the electrostatic chuck 25 by the electrostatic attraction force. The structure in the vicinity of the electrostatic chuck 25 will be described later.

An annular coolant path 31 extending in, e.g., a circumferential direction, is provided in the base 11. A coolant, e.g., cooling water, of a predetermined temperature is supplied from a chiller unit 32 and circulated in the coolant path 31 through lines 33 and 34. A temperature of the wafer W on the central portion 25a of the electrostatic chuck 25 and a temperature of the focus ring 30 are controlled by a temperature of the coolant.

A heat transfer gas supply unit 35 is connected to the electrostatic chuck 25 through a gas supply line 36. The gas supply line 36 is branched into a wafer side line 36a

reaching the central portion 25a of the electrostatic chuck 25 and a focus ring side line 36b reaching the outer peripheral portion 25b of the electrostatic chuck 25. The heat transfer gas supply unit 35 supplies a heat transfer gas to the space between the central portion 25a of the electrostatic chuck 25 and the wafer W through the wafer side line 36a. The heat transfer gas supply unit 35 supplies the heat transfer gas to the space between the outer peripheral portion 25b of the electrostatic chuck 25 and the focus ring 30 through the focus ring side line 36b. A thermally conductive gas, e.g., He gas or the like, is suitable for the heat transfer gas.

The shower head 24 provided at the ceiling portion includes an electrode plate 37 as a bottom surface having a plurality of gas injection holes 37a and an electrode holder 38 detachably holding the electrode plate 37. A buffer space 39 is provided in the electrode holder 38. A gas supply line 41 from a processing gas supply unit 40 is connected to a gas inlet port 38a of the buffer space 39. A magnet 42 extending annularly or concentrically is provided around the processing chamber 10.

The operation of the plasma processing apparatus 1 configured as described above is integrally controlled by the control unit 43. The control unit 43 is, e.g., a computer, and controls the respective components of the plasma processing apparatus 1.

The control unit 43 includes a central processing unit (CPU) (not shown) and a storage device such as a memory. The control unit 43 reads out and executes a program and a processing recipe stored in the storage device to control the respective components of the plasma processing apparatus 1 and performpredetermined plasma processing on the wafer W.

In the plasma processing apparatus 1 configured as described above, in the case of performing etching on the wafer W, first, the gate valve 20 is opened and, then, the wafer W as an etching target is loaded into the processing chamber 10 and mounted on the electrostatic chuck 25. Next, a predetermined DC voltage is applied from the DC power supply 26 to the electrode plate 25c, and the wafer W is attracted to and held on the central portion 25a of the electrostatic chuck 25. A predetermined DC voltage is applied from the DC power supplies 28-1 and 28-2 to the electrode plate 25d, and the focus ring 30 is attracted to and held on the outer peripheral portion 25b of the electrostatic chuck 25.

Then, an etching gas is supplied at a predetermined flow rate from the processing gas supply unit 40 to the buffer space 39, and then supplied into the processing chamber 10 through the gas injection holes 37a. The processing chamber 10 is exhausted by the gas exhaust unit 18, and a pressure in the processing chamber 10 is controlled to a predetermined level. In a state where the

processing gas is supplied into the processing chamber 10, the high frequency power for plasma generation is applied from the high frequency power supply 22a to the base 11 and the high frequency power for ion attraction (i.e., bias power) is applied from the high frequency power supply 22b to the base 11.

The processing gas injected through the gas injection holes 37a of the shower head 24 is converted into plasma in glow discharge generated between the shower head 24 and the base 11 by the high frequency electric power applied to the base 11. A surface to be processed of the wafer W is etched by radicals or ions in the plasma of the processing gas, and a hole is formed on the surface to be processed of the wafer W.

In the present embodiment, the control unit 43 switches the magnitude of the bias power applied to the base 11 between a relatively low value and a relatively high value by controlling the high frequency power supply 22b during the plasma processing on the wafer W.

(Structure in the vicinity of electrostatic chuck)

Next, the structure in the vicinity of the electrostatic chuck 25 will be described with reference to Fig. 2. Fig. 2 is an enlarged cross sectional view showing the base 11, the electrostatic chuck 25, the wafer W, and the focus ring 30.

As shown in Fig. 2, the wafer W is mounted on the

central portion 25a of the electrostatic chuck 25, and the focus ring 30 is mounted on the outer peripheral portion 25b to surround the wafer W. The focus ring 30 is made of a conductive member, e.g., silicon or the like. The focus ring 30 is mounted on the outer peripheral portion 25b of the electrostatic chuck 25 in a state where an entire lower surface 30b of the focus ring 30 is in contact with the outer peripheral portion 25b of the electrostatic chuck 25. In a state where the wafer W is mounted on the central portion 25a of the electrostatic chuck 25 and the focus ring 30 is mounted on the outer peripheral portion 25b of the electrostatic chuck 25, a height of an upper surface 30a of the focus ring 30 is equal to that of the upper surface of the wafer W.

A dielectric layer 50 is disposed between the outer peripheral portion 25b of the electrostatic chuck 25 and the base 11. As described above, the central portion 25a of the electrostatic chuck 25 protrudes upward with respect to the outer peripheral portion 25b of the electrostatic chuck 25 and is thicker than the outer peripheral portion 25b. Due to the difference in the thickness between the central portion 25a and the outer peripheral portion 25b, the electrostatic capacitance of the central portion 25a is smaller than that of the outer peripheral portion 25b. Therefore, the dielectric layer 50 has an electrostatic capacitance that reduces the difference between the

electrostatic capacitance of the central portion 25a of the electrostatic chuck 25 and the electrostatic capacitance of the outer peripheral portion 25b of the electrostatic chuck 25. Specifically, a thickness and a relative dielectric constant of the dielectric layer 50 are selected such that a combined electrostatic capacitance of the electrostatic capacitance of the dielectric layer 50 and that of the outer peripheral portion 25b of the electrostatic chuck 25 is equal to the electrostatic capacitance of the central portion 25a of the electrostatic chuck 25. Accordingly, an impedance between the base 11 and the focus ring 30 with the outer peripheral portion 25b of the chuck 25 interposed therebetween is matched with the impedance between the base 11 and the wafer W with the central portion 25a of the electrostatic chuck 25 interposed therebetween.

Hereinafter, the effect of the dielectric layer 50 will be described by using an equivalent circuit in the vicinity of the electrostatic chuck 25. Fig. 3 shows an example of an equivalent circuit in the vicinity of the electrostatic chuck 25 in the case where the dielectric layer 50 is not disposed between the outer peripheral portion 25b of the electrostatic chuck 25 and the base 11. Fig. 4 shows an example of an equivalent circuit in the vicinity of the electrostatic chuck 25 in the case where the dielectric layer 50 is disposed between the outer peripheral portion 25b of the electrostatic chuck 25 and the base 11.

In Figs. 3 and 4, the electrostatic capacitance of the central portion 25a of the electrostatic chuck 25 is defined as Cw, and the electrostatic capacitance of the outer peripheral portion 25b of the electrostatic chuck 25 is defined as Cf. In Fig. 4, the electrostatic capacitance of the dielectric layer 50 is defined as Cd. Since the central portion 25a of the electrostatic chuck 25 is thicker than the outer peripheral portion 25b of the electrostatic chuck 25, the electrostatic capacitance Cw is smaller than the electrostatic capacitance Cf.

First, as shown in Fig. 3, it is assumed that the dielectric layer 50 is not disposed between the outer peripheral portion 25b of the electrostatic chuck 25 and the base 11. When the bias power applied to the base 11 is changed to a relatively low value (hereinafter, referred to as "low bias power value") during the plasma processing, both of the height of the plasma sheath above the focus ring 30 and the height of the plasma sheath above the wafer W are decreased. Here, the height of the upper surface 30a of the focus ring 30 is equal to that of the upper surface of the wafer W and, thus, the height of the plasma sheath above the focus ring 30 is substantially equal to that of the plasma sheath above the wafer W, as indicated by the dashed line of Fig. 3. Then, in the vicinity of the edge portion of the wafer W, ions in the plasma are incident vertically on the surface to be processed of the wafer W. In the etching

process, a hole is formed along the ion incidence direction. Therefore, in the vicinity of the edge portion of the wafer W, the hole formed on the processed surface of the wafer W has a shape in a depth direction which extends along the vertical direction.

Thereafter, when the bias power applied to the base 11 is changed to a relatively high value (hereinafter, referred to as "high bias power value"), both of the height of the plasma sheath above the focus ring 30 and the height of the plasma above the wafer W are increased. Here, it is known that when the bias power is changed to the high bias power value, the height relation between the plasma sheath above the wafer W and the plasma sheath above the focus ring 30 depends on a difference between the impedance between the wafer W and the base 11 and the impedance between the focus ring 30 and the base 11. When the dielectric layer 50 is not disposed, the impedance between the wafer W and the base 11 is proportional to a reciprocal of the electrostatic capacitance Cw, and the impedance between the focus ring 30 and the base 11 is proportional to a reciprocal of the electrostatic capacitance Cf. The electrostatic capacitance Cw is smaller than the electrostatic capacitance Cf. Therefore, the impedance between the wafer W and the base 11 is greater than the impedance between the focus ring 30 and the base 11. Accordingly, the height of the plasma sheath above the focus ring 30 is greater than the height of the

plasma sheath above the wafer W, as indicated by the solid line of Fig. 3. Then, in the vicinity of the edge portion of the wafer W, ions in the plasma are incident on the surface to be processed of the wafer W while being inclined obliquely toward the edge portion of the wafer W. Therefore, in the vicinity of the edge portion of the wafer W, the hole formed on the processed surface of the wafer W has a shape that is obliquely inclined toward the edge portion of the wafer W with respect to the vertical direction. As a result, the tilting on the wafer W is increased.

On the other hand, as shown in Fig. 4, it is assumed that the dielectric layer 50 is disposed between the outer peripheral portion 25b of the electrostatic chuck 25 and the base 11. When the bias power applied to the base 11 is changed to the low bias power value during the plasma processing, both of the height of the plasma sheath above the focus ring 30 and the height of the plasma sheath above the wafer W are decreased. Here, the height of the upper surface 30a of the focus ring 30 is equal to that of the upper surface of the wafer W and, thus, the height of the plasma sheath above the focus ring 30 is equal to that of the plasma sheath above the wafer W. Then, in the vicinity of the edge portion of the wafer W, ions in the plasma are incident vertically to the surface to be processed of the wafer W. In the etching process, a hole is formed along the ion incidence direction. Therefore, in the vicinity of the

edge portion the wafer W, the hole formed on the processed surface of the wafer W has a shape in a depth direction which extends along the vertical direction.

Thereafter, when the bias power applied to the base 11 is changed to the high bias power value, both of the height of the plasma sheath above the focus ring 30 and the height of the plasma sheath above the wafer W are increased. Here, it is known that when the bias power is changed to the high bias power value, the height relation between the plasma sheath above the wafer W and the plasma sheath above the focus ring 30 depends on the difference between the impedance between the wafer W and the base 11 and the impedance between the focus ring 30 and the base 11. When the dielectric layer 50 is disposed, the impedance between the wafer W and the base 11 is proportional to a reciprocal of the electrostatic capacitance Cw, and the impedance between the focus ring 30 and the base 11 is proportional to a reciprocal of the combined electrostatic capacitance $(Cf \cdot Cd)/(Cf+Cd)$ of the electrostatic capacitance Cf and the electrostatic capacitance Cd. In the present embodiment, a thickness and a relative dielectric constant of the dielectric layer 50 are selected such that the combined electrostatic capacitance $(Cf \cdot Cd)/(Cf+Cd)$ is equal to the electrostatic capacitance Cw. Accordingly, the impedance between the base 11 and the focus ring 30 with the dielectric layer 50 and the outer peripheral portion 25b of

the electrostatic chuck 25 interposed therebetween is matched with the impedance between the base 11 and the wafer W with the central portion 25a of the electrostatic chuck 25 interposed therebetween. Thus, the height of the plasma sheath above the focus ring 30 is equal to that of the plasma sheath above the wafer W, as indicated by the solid line of Fig. 4. Then, in the vicinity of the edge portion of the wafer W, ions in the plasma are incident vertically to the surface to be processed of the wafer W. Therefore, in the vicinity of the edge portion of the wafer W, the hole formed on the processed surface of the wafer W has a shape in a depth direction which extends along the vertical direction. In other words, by disposing the dielectric layer 50 as in this embodiment, it is possible to suppress tilting caused by the change in the magnitude of the bias power in the plasma processing in which the bias power is changed between a low bias power value and a high bias power value.

In the above description, the thickness and the relative dielectric constant of the dielectric layer 50 are selected such that the combined electrostatic capacitance $(Cf \cdot Cd)/(Cf+Cd)$ is equal to the electrostatic capacitance Cw. However, the present disclosure is not limited thereto, and it is also possible to select the thickness and the relative dielectric constant of the dielectric layer 50 while considering that a part of the lower surface 30b of

the focus ring 30 is in contact with the outer peripheral portion 25b of the electrostatic chuck 25. Fig. 5 shows another example of an equivalent circuit in the vicinity of the electrostatic chuck in the case where the dielectric layer is disposed between the outer peripheral portion of the electrostatic chuck and the base. In the example shown in Fig. 5, the focus ring 30 is mounted on the outer peripheral portion 25b of the electrostatic chuck 25 in a state where a part of the lower surface 30b of the focus ring 30 is in contact with the outer peripheral portion 25b of the electrostatic chuck 25. In Fig. 5, an area of the upper surface 30a of the focus ring 30 which is exposed to the plasma is defined as S1, and an area of a part of the lower surface 30b of the focus ring 30 which is in contact with the outer peripheral portion 25b of the electrostatic chuck 25 is defined as S2. In that case, the thickness and the relative dielectric constant of the dielectric layer 50 are selected such that a value obtained by multiplying the combined electrostatic capacitance $(Cf \cdot Cd)/(Cf+Cd)$ by a ratio of the area S2 to the area S1 is equal to the electrostatic capacitance Cw. Accordingly, the impedance between the base 11 and the focus ring 30 with the dielectric layer 50 and the outer peripheral portion 25b of the electrostatic chuck 25 interposed therebetween is more accurately matched with the impedance between the base 11 and the wafer W with the central portion 25a of the

electrostatic chuck 25 interposed therebetween.

Referring back to Fig. 2, the dielectric layer 50 is formed on the base 11 without an adhesive interposed therebetween. Specifically, as shown in Fig. 2, the dielectric layer 50 is formed in a recess formed on a region of the upper surface of the base 11 which corresponds to the outer peripheral portion 25b of the electrostatic chuck 25 by thermal spraying or coating.

Since the dielectric layer 50 is formed on the base 11 without the adhesive interposed therebetween, the heat transfer from the focus ring 30 to the base 11 is not hindered. Accordingly, the increase in the temperature of the focus ring 30 can be suppressed.

Next, modified arrangement of the dielectric layer 50 will be described. Fig. 6 shows the modified arrangement of the dielectric layer 50. In the above embodiment, the dielectric layer 50 is disposed between the outer peripheral portion 25b of the electrostatic chuck 25 and the base 11. However, as shown in Fig. 6, for example, the dielectric layer 50 may be disposed between the outer peripheral portion 25b of the electrostatic chuck 25 and the focus ring 30. Similarly to the dielectric layer 50 shown in Fig. 2, the dielectric layer 50 shown in Fig. 6 has an electrostatic capacitance that reduces the difference between the electrostatic capacitance of the central portion 25a of the electrostatic chuck 25 and the electrostatic capacitance of

the outer peripheral portion 25b of the electrostatic chuck 25. Specifically, the thickness and the relative dielectric constant of the dielectric layer 50 are selected such that the combined electrostatic capacitance of the electrostatic capacitance of the dielectric layer 50 and the electrostatic capacitance of the outer peripheral portion 25b of the electrostatic chuck 25 is equal to the electrostatic capacitance of the central portion 25a of the electrostatic chuck 25. Accordingly, the impedance between the base 11 and the focus ring 30 with the dielectric layer 50 and the outer peripheral portion 25b of the electrostatic chuck 25 interposed therebetween is matched with the impedance between the base 11 and the wafer W with the central portion 25a of the electrostatic chuck 25 interposed therebetween.

In the above description, the impedance is matched by the thickness and the relative dielectric constant of the dielectric layer 50. However, the present disclosure is not limited thereto. For example, the impedance may be matched by adjusting the thickness of the base for the wafer or the thickness of the base for the focus ring.

(Relation between magnitude of bias power and inclination angle of hole)

Next, an effect of the plasma processing apparatus 1 according to an embodiment (measurement result of the relation between the magnitude of the bias power and the inclination angle of the hole) will be described. Fig. 7

shows an exemplary measurement result of the relation between the magnitude of the bias power and the inclination angle of the hole.

In Fig. 7, "Comparative Example" shows a measurement result of an inclination angle θ of a hole in the case of performing etching that involveschanging of the magnitude of the bias power by using a plasma processing apparatus in which the dielectric layer 50 is not disposed between the outer peripheral portion 25b of the electrostatic chuck 25 and the base 11. "Test Example 1" shows a measurement result of an inclination angle θ of a hole in the case of performing etching that involves changing of the magnitude of the bias power by using the plasma processing apparatus 1 in which the dielectric layer 50 is disposed between the outer peripheral portion 25b of the electrostatic chuck 25 and the base 11. "Test Example 2" shows a measurement result of an inclination angle θ of a hole in the case of performing etching that involves changing of the magnitude of the bias power by using the plasma processing apparatus 1 in which the dielectric layer 50 is disposed between the outer peripheral portion 25b of the electrostatic chuck 25 and the focus ring 30. In the "comparative example", the height of the focus ring 30 is adjusted such that the inclination angle θ of the hole in the case of changing the bias power applied to the base 11 to 14000 W that is the high bias electric power value becomes approximately the

same.

In Fig. 7, it is assumed that the bias power applied to the base 11 is changed to 2000 W that is the low bias electric power value and 14000 W that is the high bias electric power value. Further, in Fig. 7, the inclination angle θ of the hole is defined as an angle in a depth direction of the hole with respect to the vertical direction. In other words, when the hole formed in the wafer W is inclined obliquely toward the outer peripheral portion of the surface to be processed of the wafer W, the inclination angle θ of the hole has a positive value. On the other hand, when the hole formed in the wafer W is inclined obliquely toward the central portion of the surface to be processed of the wafer W, the hole inclination angle θ has a negative value.

As shown in Fig. 7, in the comparative example, when the magnitude of the bias power was changed, the variation Δθ in the inclination angle θ of the hole was 0.48 deg.

On the other hand, in the test example 1, when the magnitude of the bias power was changed, the variation Δθ of the inclination angle θ of the hole was 0.06 deg. In the test example 2, when the magnitude of the bias power was changed, the variation Δθ of the inclination angle θ of the hole was 0.35 deg. In other words, in the test examples 1 and 2, tilting on the wafer W can be suppressed in the etching involving changing of the magnitude of the bias

power, compared to the comparative example.

In the test example 2, the variation $\Delta\theta$ of the inclination angle θ of the hole is greater than that in the test example 1. This is because the impedance between the base 11 and the focus ring 30 in the test example 2 is higher than the impedance between the base 11 and the wafer W with the central portion 25a of the electrostatic chuck 25 interposed therebetween. If the impedance between the base 11 and the focus ring 30 is too high, the variation $\Delta\theta$ in the inclination angle θ of the hole is increased, which is not preferable.

(Simulation result of temperature distribution of focus ring 30)

Next, an effect (simulation result of temperature distribution of the focus ring 30) of the plasma processing apparatus 1 according to an embodiment will be described. Fig. 8 shows a simulation result of the temperature distribution of the focus ring 30 in the plasma processing apparatus (comparative example) in which the dielectric layer 50 is not disposed between the outer circumferential portion 25b of the electrostatic chuck 25 and the base 11. Fig. 9 shows a simulation result of the temperature distribution of the focus ring 30 in the plasma processing apparatus 1 (test example) in which the dielectric layer 50 is disposed between the outer peripheral portion 25b of the electrostatic chuck 25 and the base 11.

As shown in Figs. 8 and 9, the temperature distribution of the focus ring 30 in the test example is substantially the same as that in the comparative example. In other words, in the test embodiment, the dielectric layer 50 is formed on the base 11 without an adhesive interposed therebetween. Therefore, the heat transfer from the focus ring 30 to the base 11 is not hindered, and the increase in the temperature of the focus ring 30 can be suppressed.

In accordance with the above embodiment, the dielectric layer 50 is disposed between the base 11 and the outer peripheral portion 25b of the electrostatic chuck 25 provided on the base 11 to which the bias power whose magnitude is changed during the plasma processing on the wafer W is applied or between the focus ring 11 and the outer peripheral portion 25b of the electrostatic chuck 25. Accordingly, tilting on the wafer W can be suppressed in the plasma processing that involves changing the magnitude of the bias power.

Further, in accordance with the above embodiment, the dielectric layer 50 is formed on the base 11 without an adhesive interposed therebetween. Therefore, the heat transfer from the focus ring 30 to the base 11 is not hindered, and the increased in the temperature of the focus ring 30 can be suppressed.

The present disclosure is not limited to the above-described embodiments, and various modifications can be made

within the scope of the gist of the present disclosure.

For example, in the above-described embodiment, the electrostatic chuck 25 attracts and holds the focus ring 30 by the electrostatic attraction force. However, the electrostatic chuck 25 may not attract and hold the focus ring 30. In that case, the electrode plate 25d is omitted from the electrostatic chuck 25.

In the above embodiment, the plasma processing apparatus 1 is configured as a CCP type plasma etching apparatus. However, the plasma processing apparatus 1 may employ any plasma source. For example, the plasma processing apparatus 1 may employ as the plasma source an inductively coupled plasma (ICP), a radial line slot antenna, an electron cyclotron resonance plasma (ECR), a helicon wave plasma (HWP), and the like.

While the present disclosure has been shown and described with respect to the embodiments, it will be understood by those skilled in the art that various changes and modifications may be made without departing from the scope of the present disclosure as defined in the following claims.

What is claimed is:

1. A plasma processing apparatus comprising:

a base to which a bias power, whose magnitude is changed during plasma processing on a target substrate, is applied;

an electrostatic chuck, provided on the base, having a central portion on which the target substrate is mounted and an outer peripheral portion on which a focus ring is mounted to surround the target substrate, the central portion protruding upward with respect to the outer peripheral portion and being thicker than the outer peripheral portion; and

a dielectric layer, provided between the outer peripheral portion of the electrostatic chuck and the base, having an electrostatic capacitance that reduces a difference between an electrostatic capacitance of the central portion of the electrostatic chuck and an electrostatic capacitance of the outer peripheral portion of the electrostatic chuck.

2. The plasma processing apparatus of claim 1, wherein a thickness and a relative dielectric constant of the dielectric layer are selected such that a combined electrostatic capacitance of the electrostatic capacitance of the dielectric layer and the electrostatic capacitance of the outer peripheral portion of the electrostatic chuck is equal to the electrostatic capacitance of the central portion of the electrostatic chuck.

3. The plasma processing apparatus of claim 1 or 2, wherein the focus ring is mounted on the outer peripheral portion of the electrostatic chuck in a state where a part of a lower surface of the focus ring is in contact with the outer peripheral portion of the electrostatic chuck, and

a thickness and a relative dielectric constant of the dielectric layer are selected such that a value obtained by multiplying a combined electrostatic capacitance of the electrostatic capacitance of the dielectric layer and the electrostatic capacitance of the outer peripheral portion of the electrostatic chuck by a ratio of an area of the part of the lower surface of the focus ring to an area of an upper

surface of the focus ring is equal to the electrostatic capacitance of the central portion of the electrostatic chuck.

4. The plasma processing apparatus of any one of claims 1 to 3, wherein in a state where the target substrate is mounted on the central portion of the electrostatic chuck and the focus ring is mounted on the outer peripheral portion of the electrostatic chuck, a height of an upper surface of the focus ring is equal to a height of an upper surface of the target substrate.

5. The plasma processing apparatus of any one of claims 1 to 4, wherein the dielectric layer is formed on the base without an adhesive interposed therebetween.

6. A plasma processing method for performing plasma processing on a target substrate by using the plasma processing apparatus described in any one of claims 1 to 5.