

ABSTRACT

A semiconductor package includes a processor, a lower memory including a plurality of lower memory chips that are vertically stacked, an interposer mounted on the processor and the lower memory, and an upper memory mounted on the interposer, the upper memory including a plurality of upper memory chips that are vertically stacked. The interposer includes a first physical layer (PHY) transmitting and receiving a signal between the processor and the lower memory and transmitting and receiving a signal between the processor and the upper memory, and the processor includes a second PHY communicating with the first PHY and a first through silicon via (TSV) electrically connecting the first PHY to the second PHY.

FIG. 1A