ABSTRACT

METHOD OF FABRICATING CMOS DEVICE WITH DUAL GATE ELECTRODE

A method of fabricating dual gate oxide thicknesses comprising the following steps. A substrate is provided having a first pillar and a second pillar. A gate dielectric layer is formed over the substrate and the first and second pillars. First and second thin spacers are formed over the gate dielectric layer covered side walls of the first and second pillars respectively. The second pillar is masked leaving the first pillar unmasked. The first thin spacers are removed from the unmasked first pillar. The mask is removed from the masked second pillar. The structure is oxidized to convert the second thin spacers to second preliminary gate oxide over the previously masked second pillar and to form first preliminary gate oxide over the unmasked first pillar. The second gate oxide over the second pillar being thicker than the first gate oxide over the first pillar. The thinner first preliminary gate oxide is removed from over the first pillar and the thicker second preliminary gate oxide is thinned from over the second pillar. First final gate oxide is formed over the first pillar and second final gate oxide is formed on the second pillar. The second final gate oxide including the thinned second preliminary gate oxide. The second final gate oxide over the second pillar being thicker than the first final gate oxide over the first pillar.

FIGURE 8



