Fig. 1

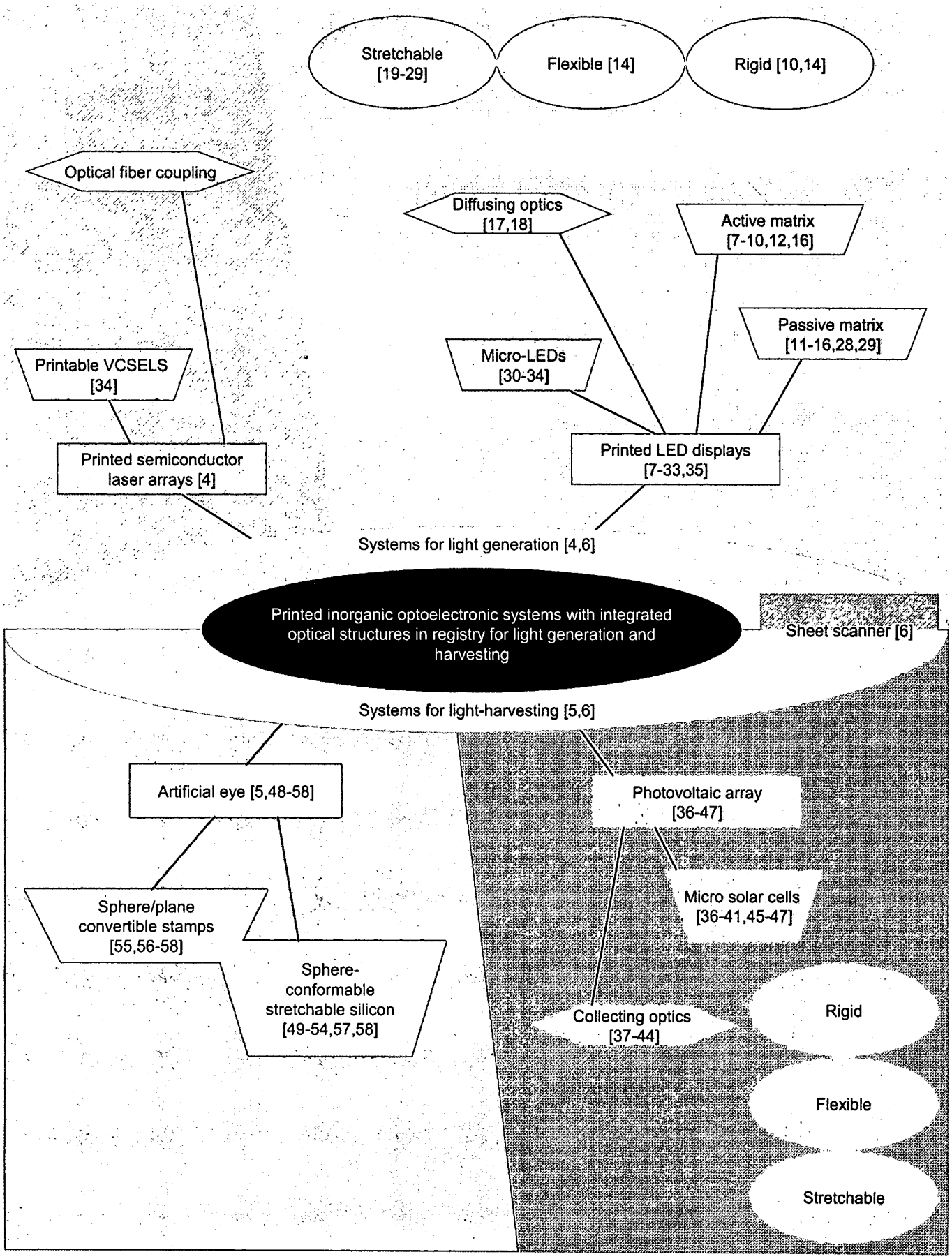

Stretchable [19-29]
Flexible [14]
Rigid [10,14]
Optical fiber coupling
Diffusing optics [17,18]
Active matrix [7-10,12,16]
Passive matrix [11-16,28,29]
Micro-LEDs [30-34]
Printable VCSELS [34]
Printed semiconductor laser arrays [4]
Printed LED displays [7-33,35]
Systems for light generation [4,6]
Printed inorganic optoelectronic systems with integrated optical structures in registry for light generation and harvesting
Sheet scanner [6]
Systems for light-harvesting [5,6]
Artificial eye [5,48-58]
Photovoltaic array [36-47]
Sphere/plane convertible stamps [55,56-58]
Micro solar cells [36-41,45-47]
Sphere-conformable stretchable silicon [49-54,57,58]
Collecting optics [37-44]
Rigid
Flexible
Stretchable

Fig. 2A

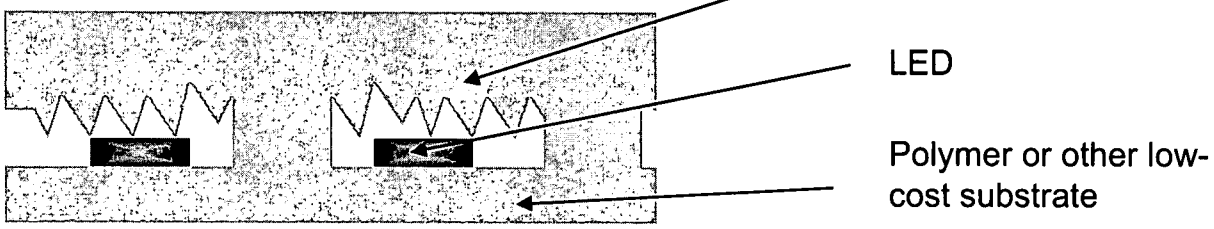

Diffusing optics
LED
Polymer or other low-cost substrate

Fig. 2B

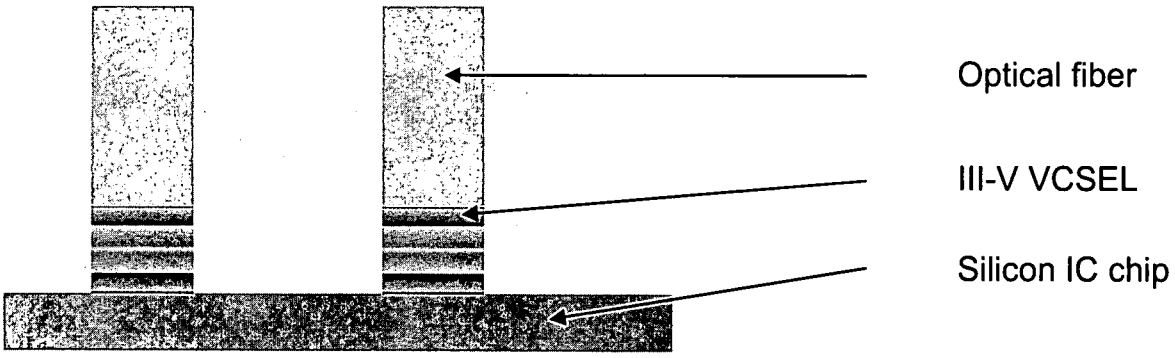

Optical fiber
III-V VCSEL
Silicon IC chip

Fig. 2C

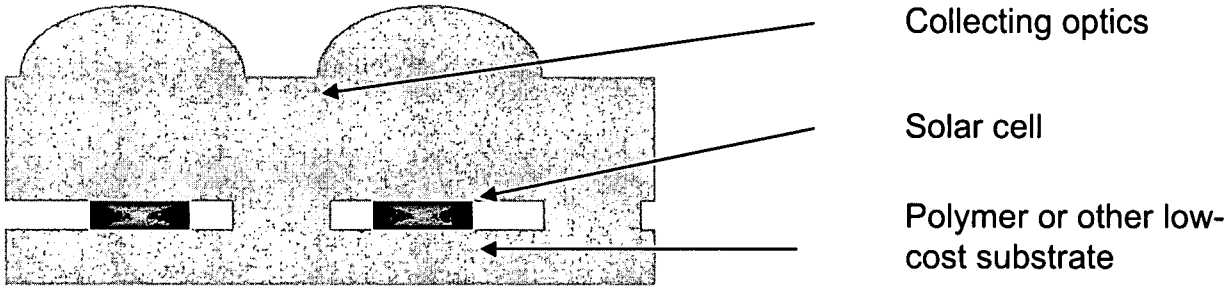

Collecting optics
Solar cell
Polymer or other low-cost substrate

Fig. 2D

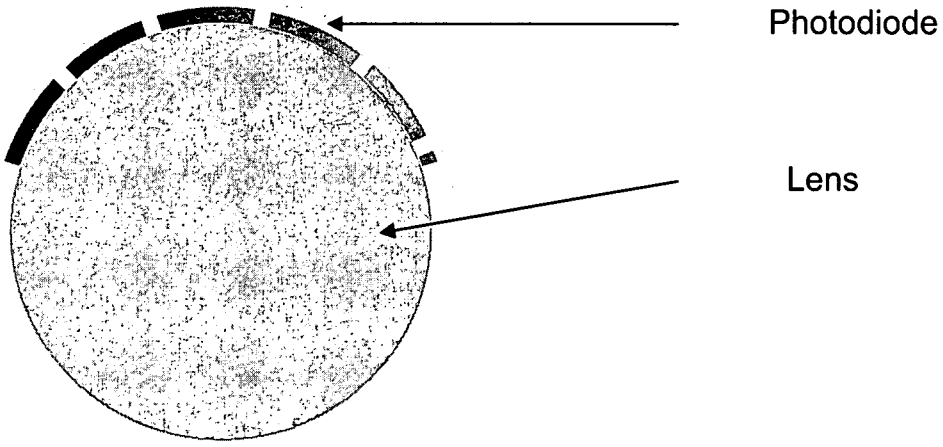
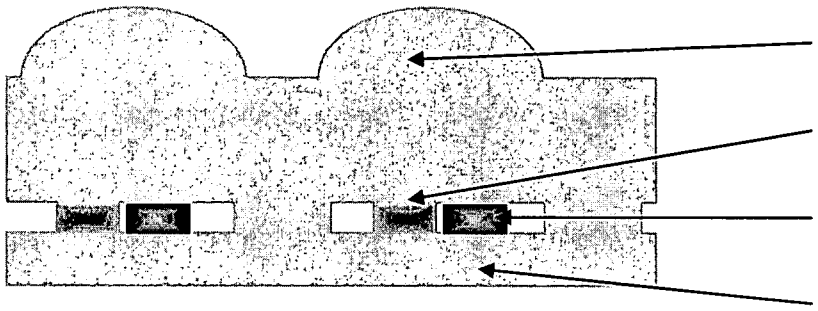

Photodiode
Lens

Fig. 2E



1)



2)

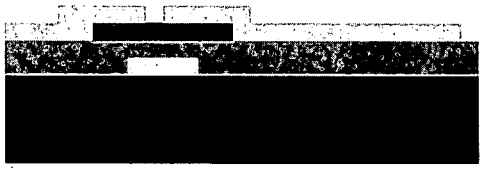


3)

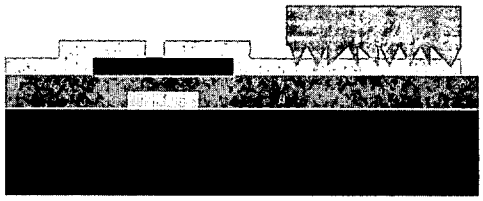


Fig. 3

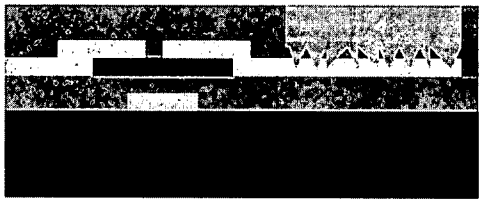
4)



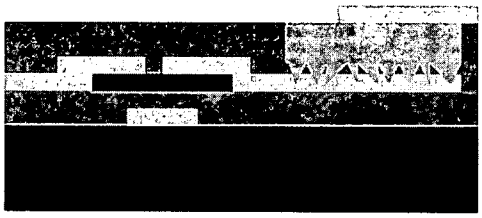
5)



6)



7)



As shown, 100 pixels, ~11' display. Not to scale.

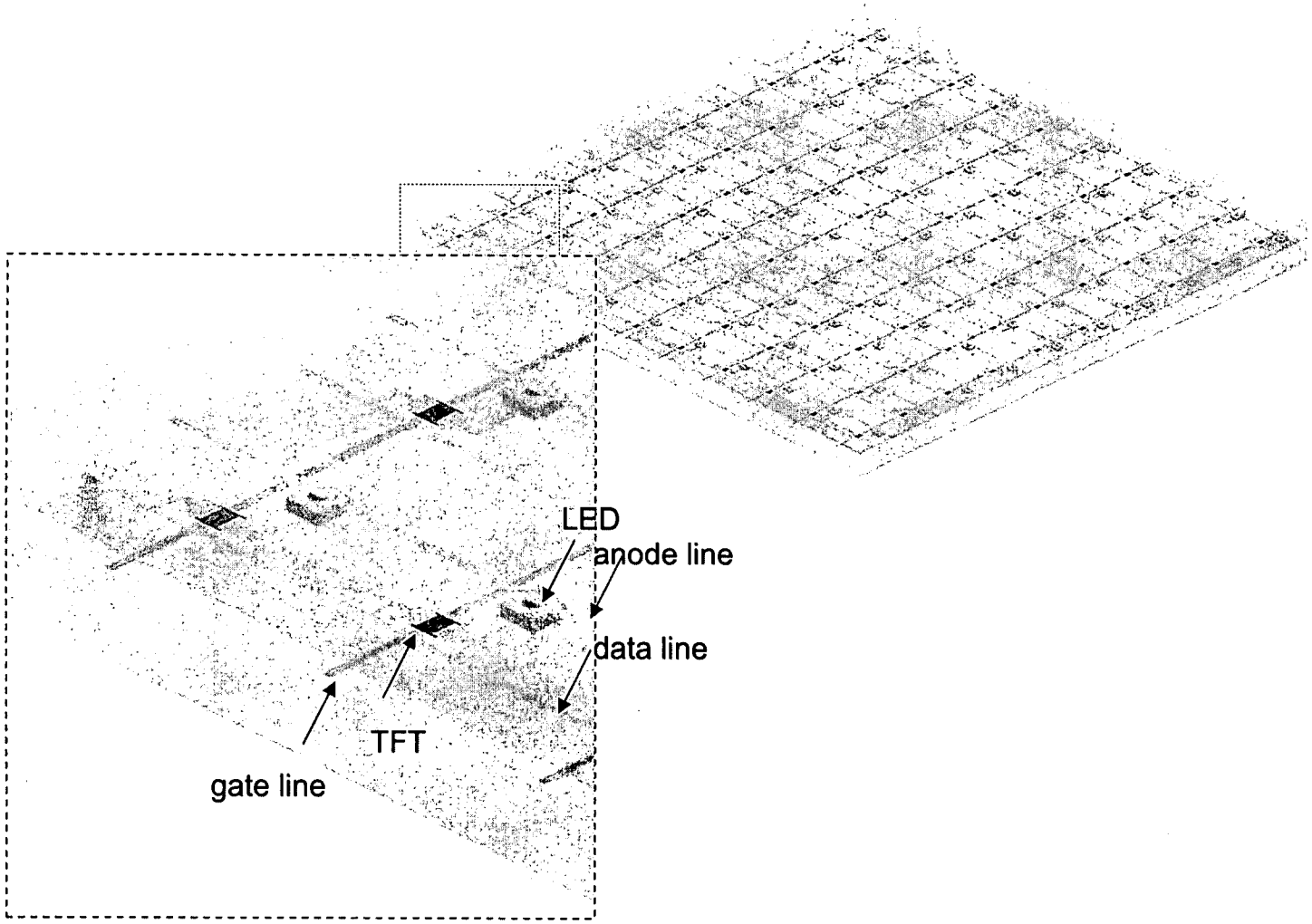


Fig. 4

Fig. 5A

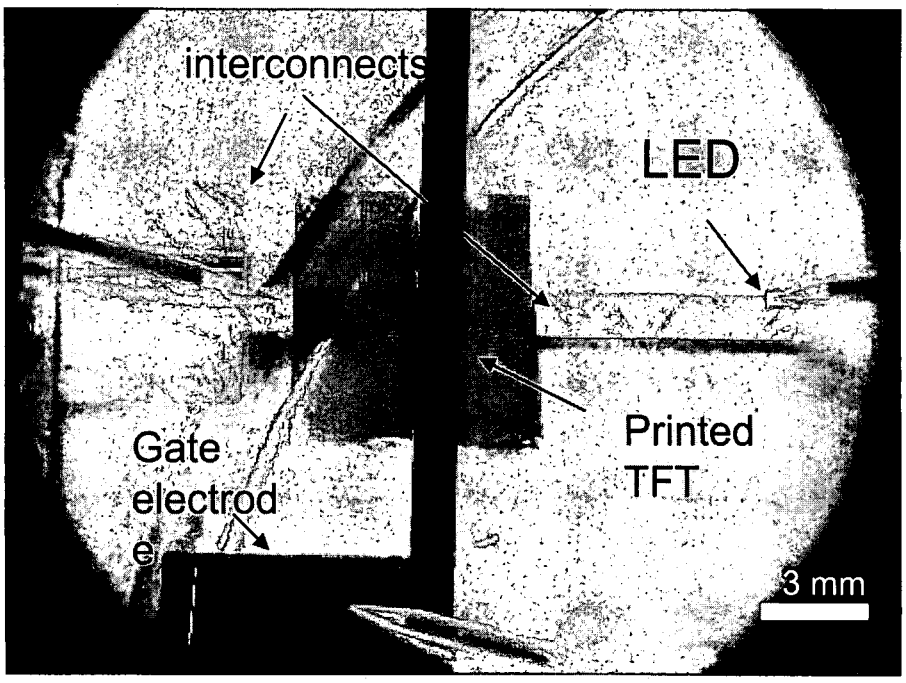

interconnects
LED
Printed
TFT
Gate
electrod
e
3 mm

Fig. 5B

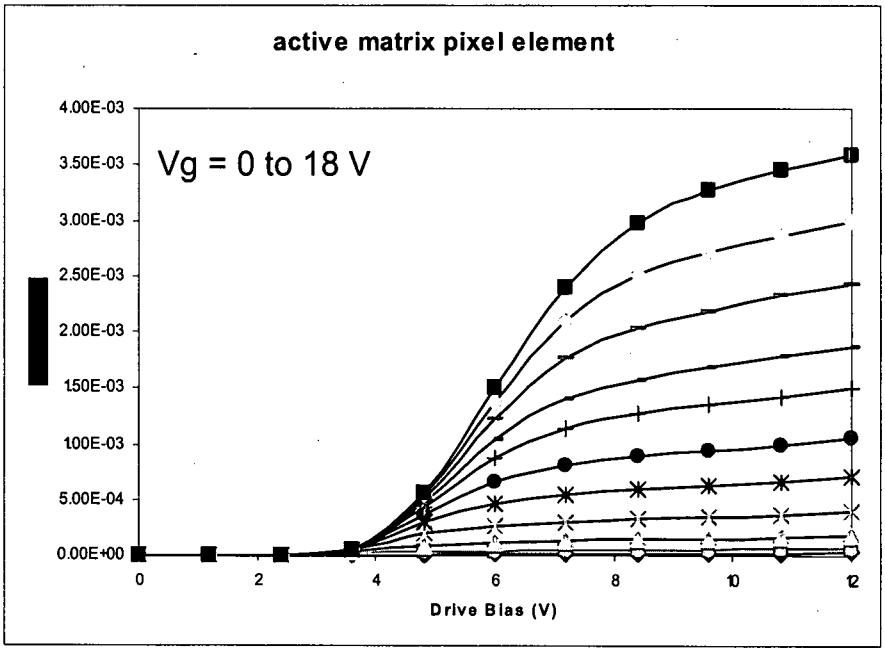

active matrix pixel element
Vg = 0 to 18 V
4.00E-03
3.50E-03
3.00E-03
2.50E-03
2.00E-03
1.50E-03
1.00E-03
5.00E-04
0.00E+00
0
2
4
6
8
10
12
Drive Bias (V)

Fig. 6A

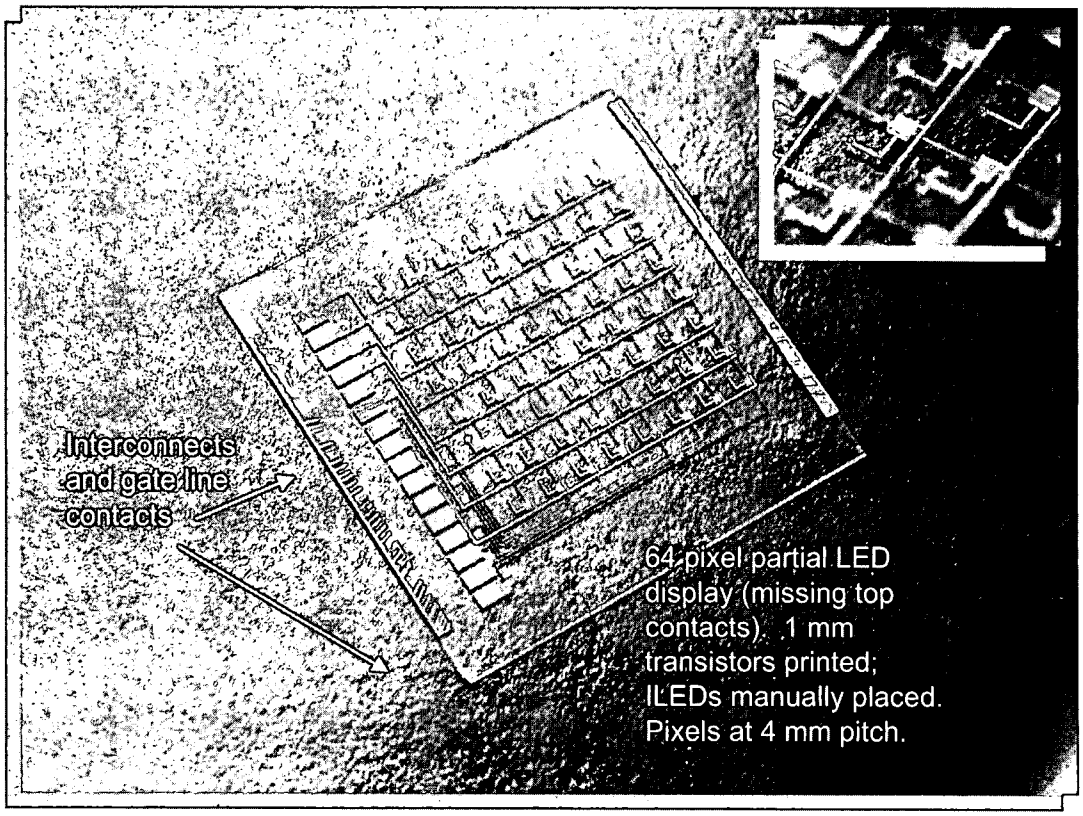
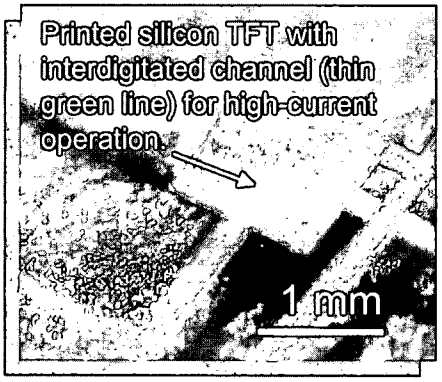
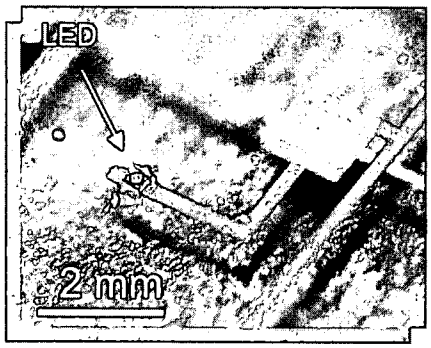


Fig. 6B





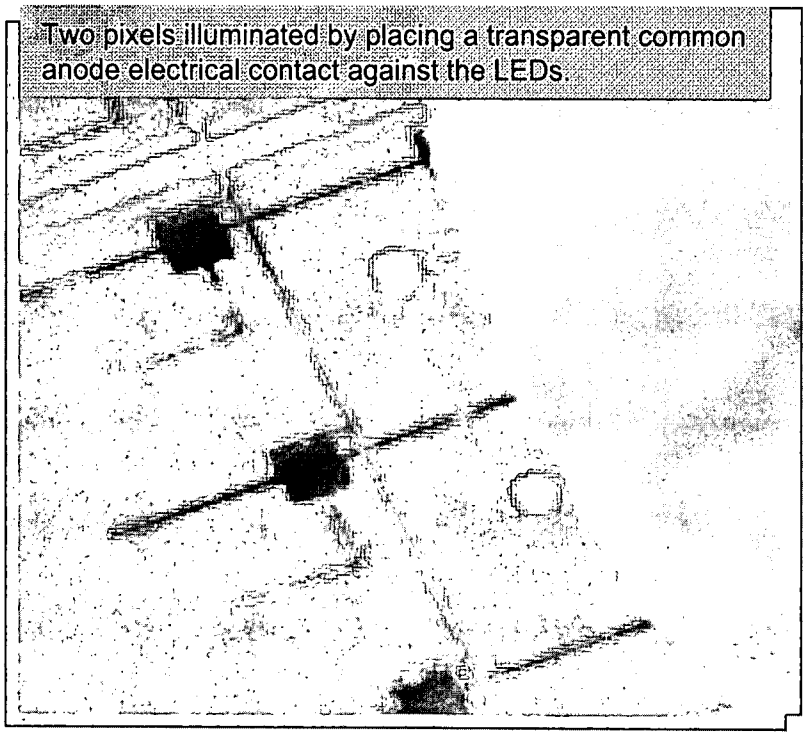


Fig. 6C

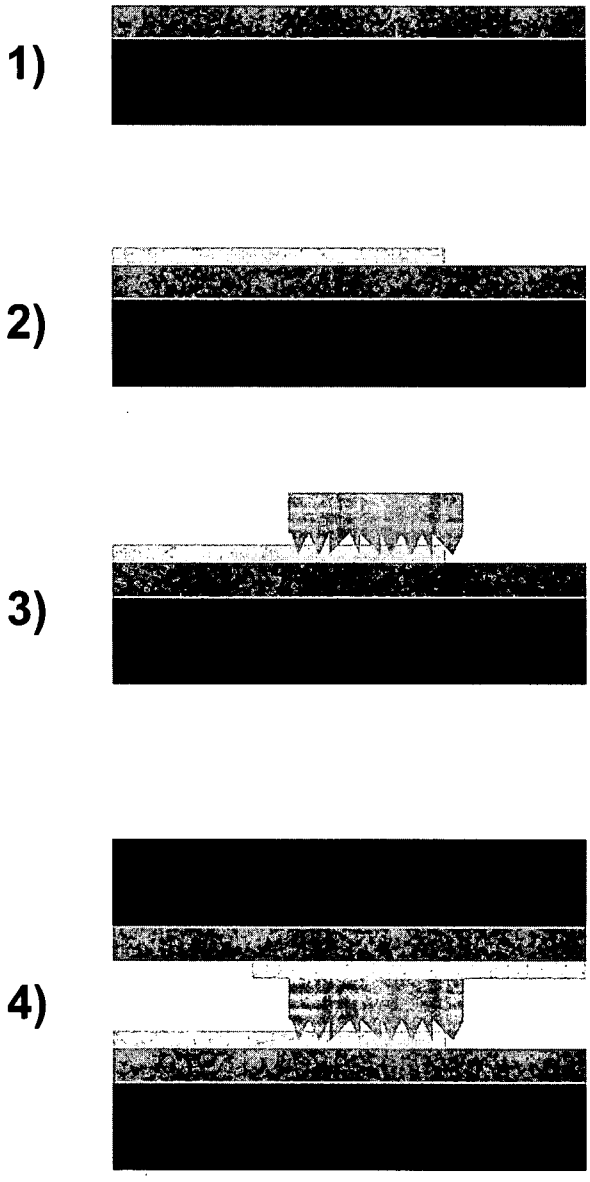


Fig. 7A

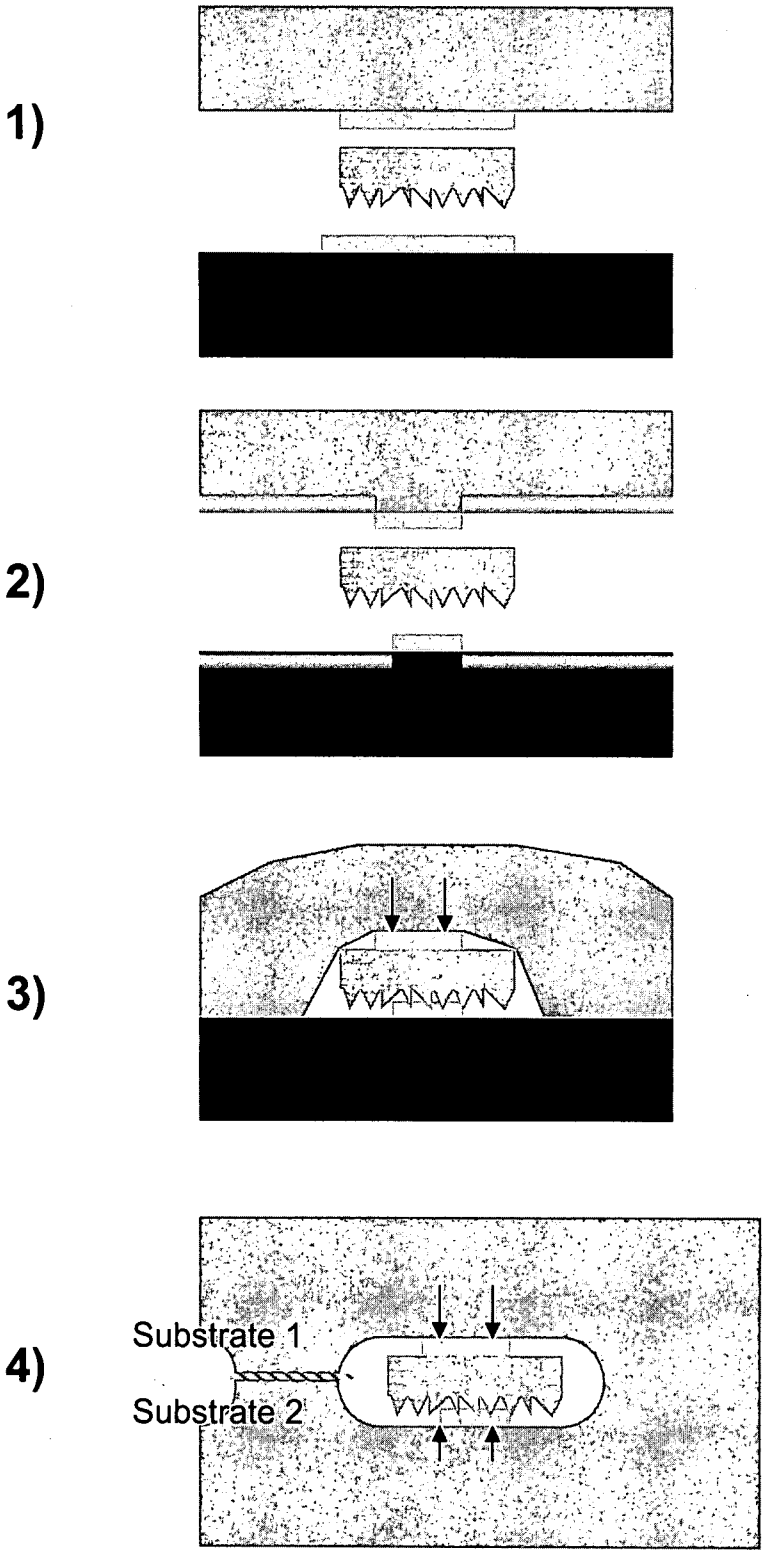


Fig. 7B

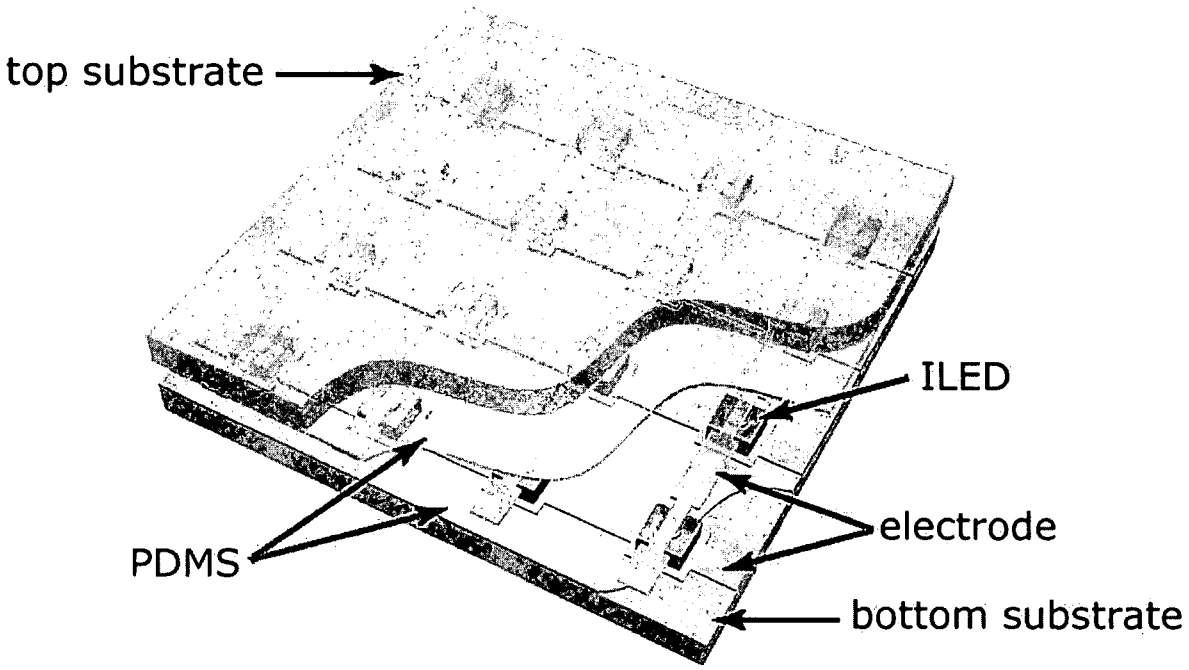


Fig. 8

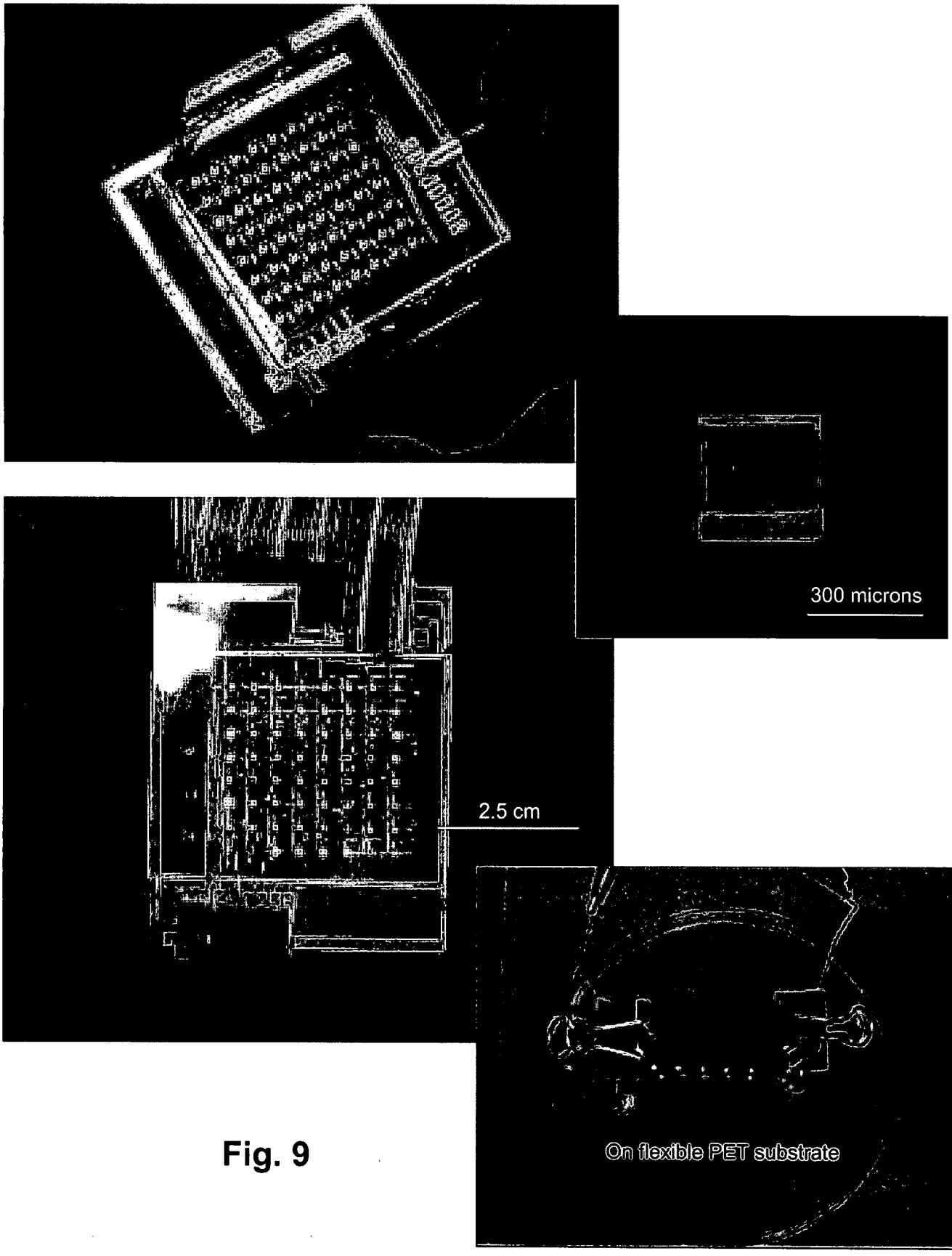


Fig. 9

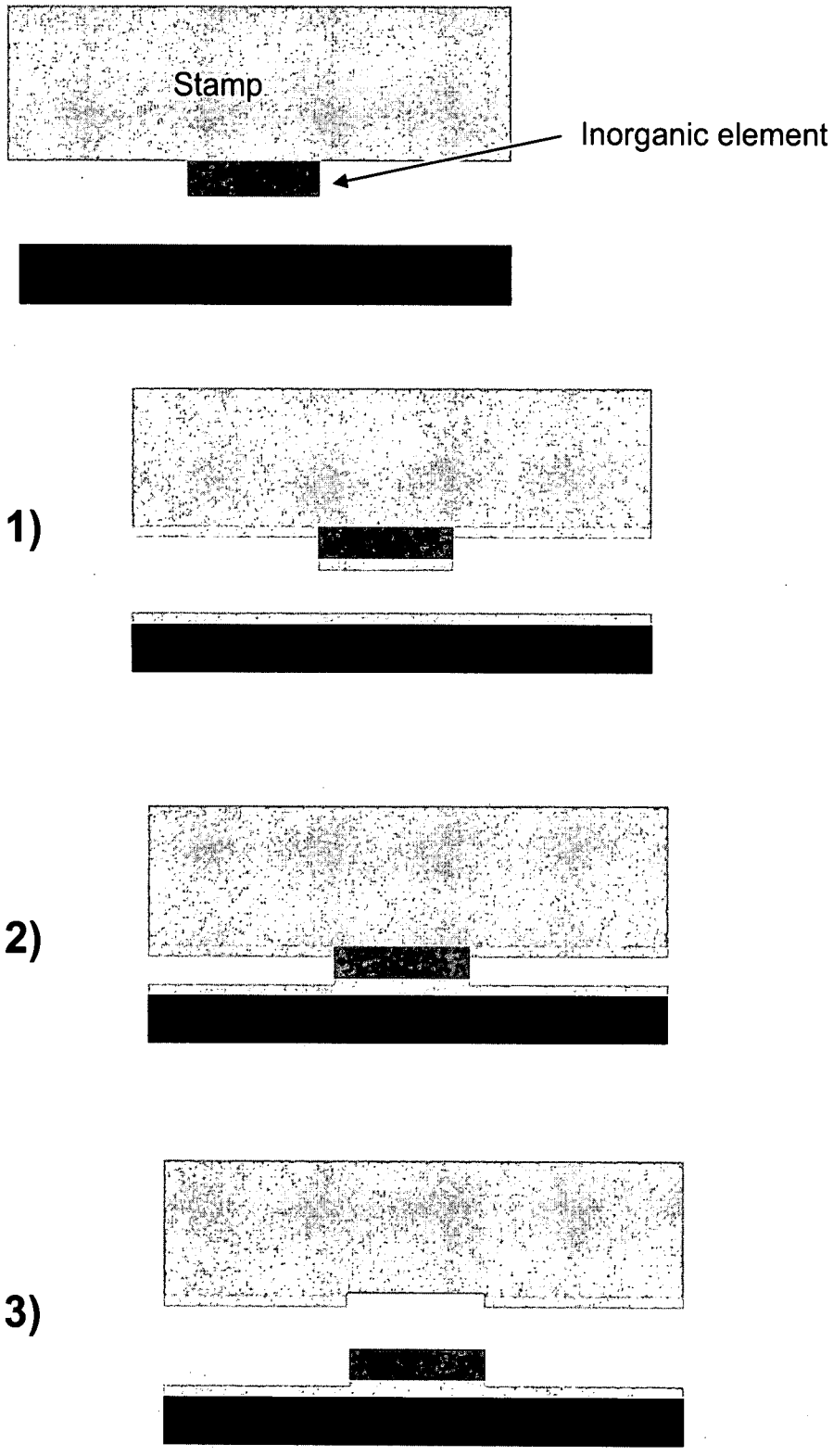


Fig. 10

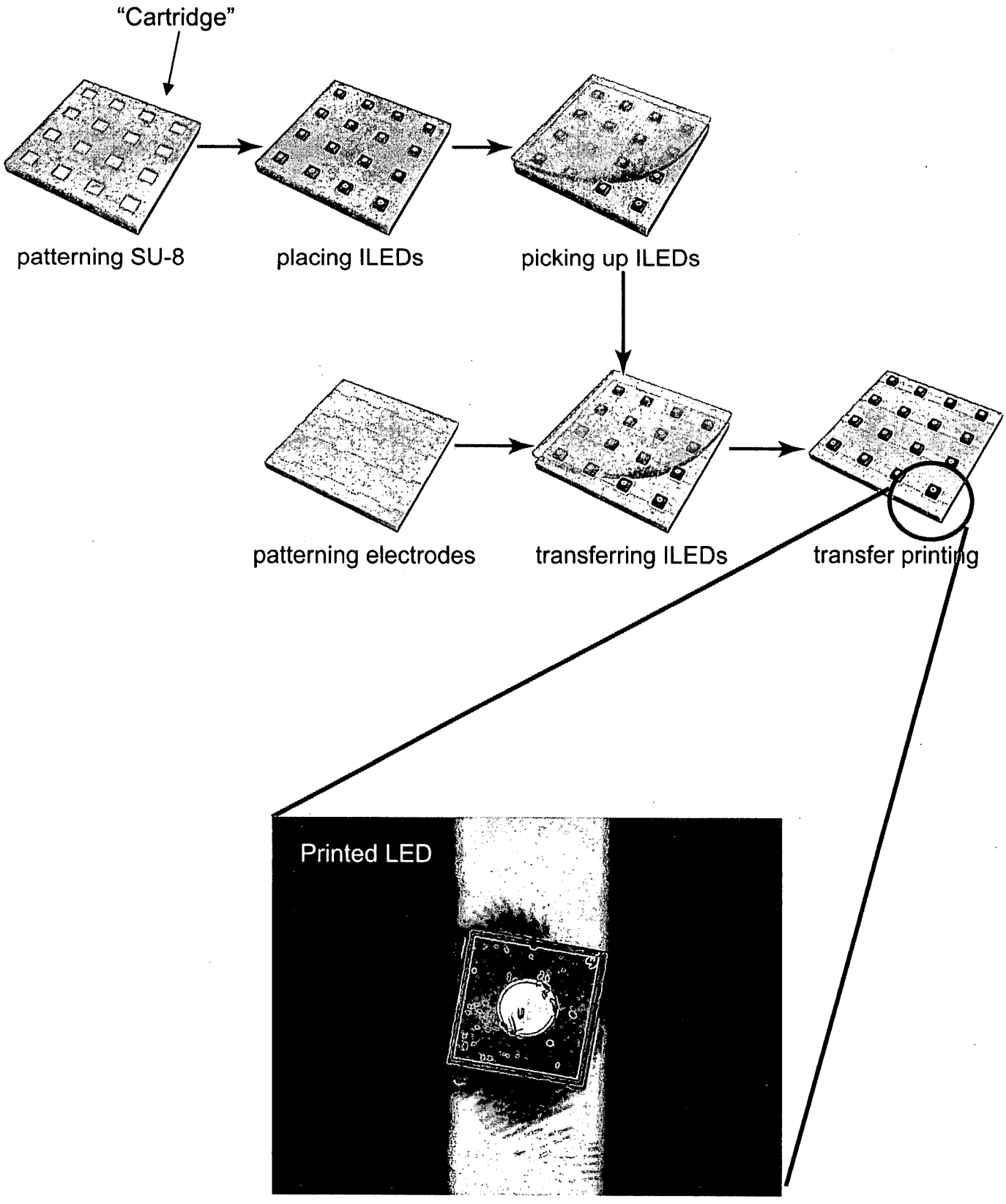
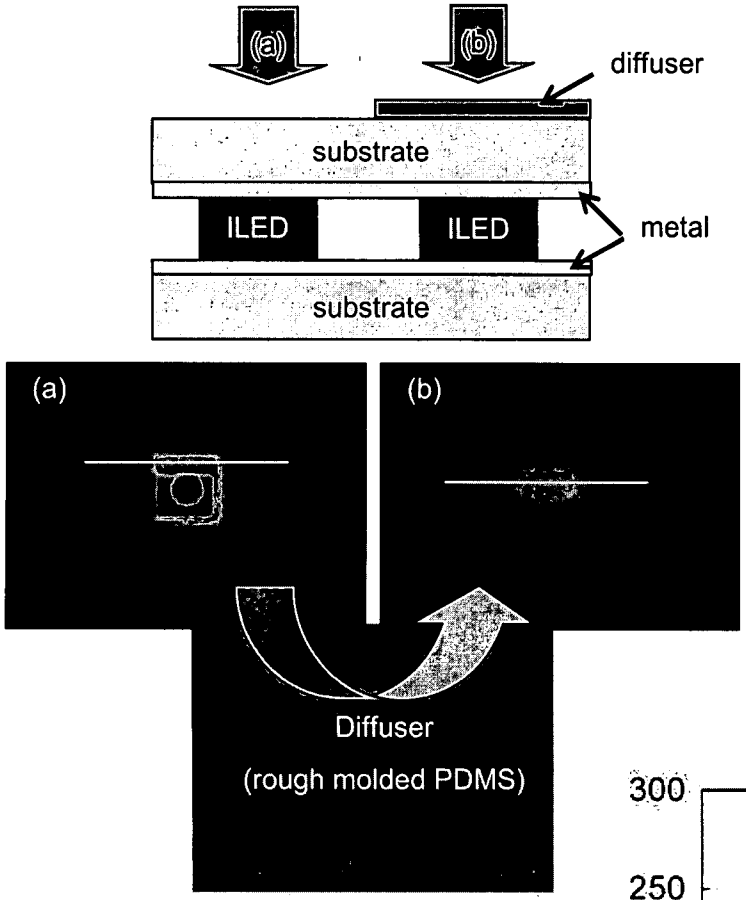

"Cartridge"
patterning SU-8
placing ILEDs
picking up ILEDs
patterning electrodes
transferring ILEDs
transfer printing
Printed LED

Fig. 11



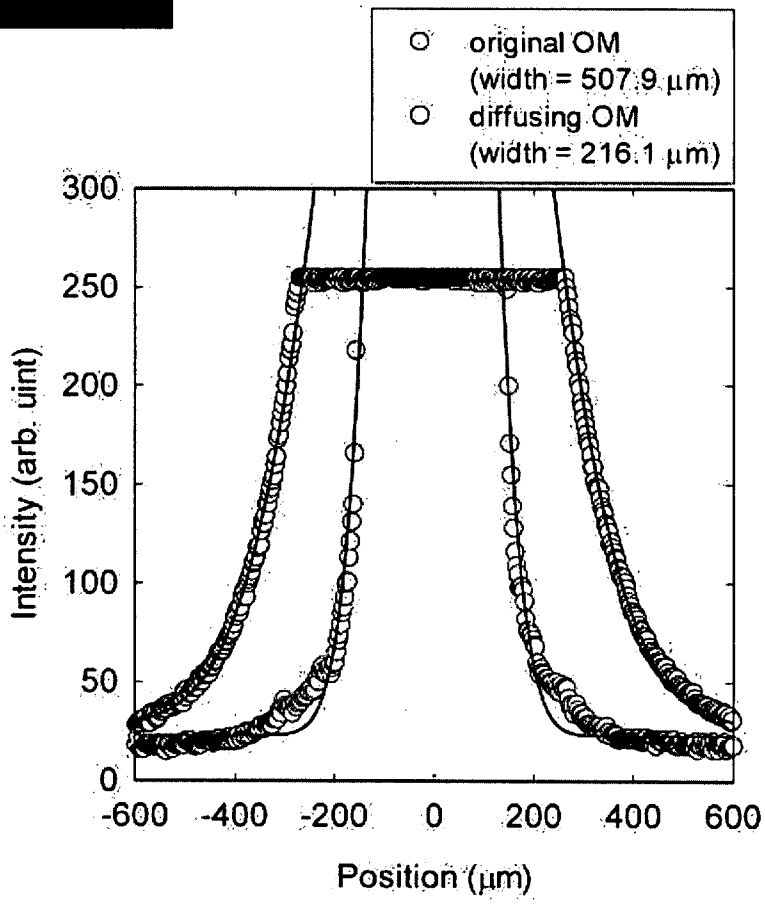
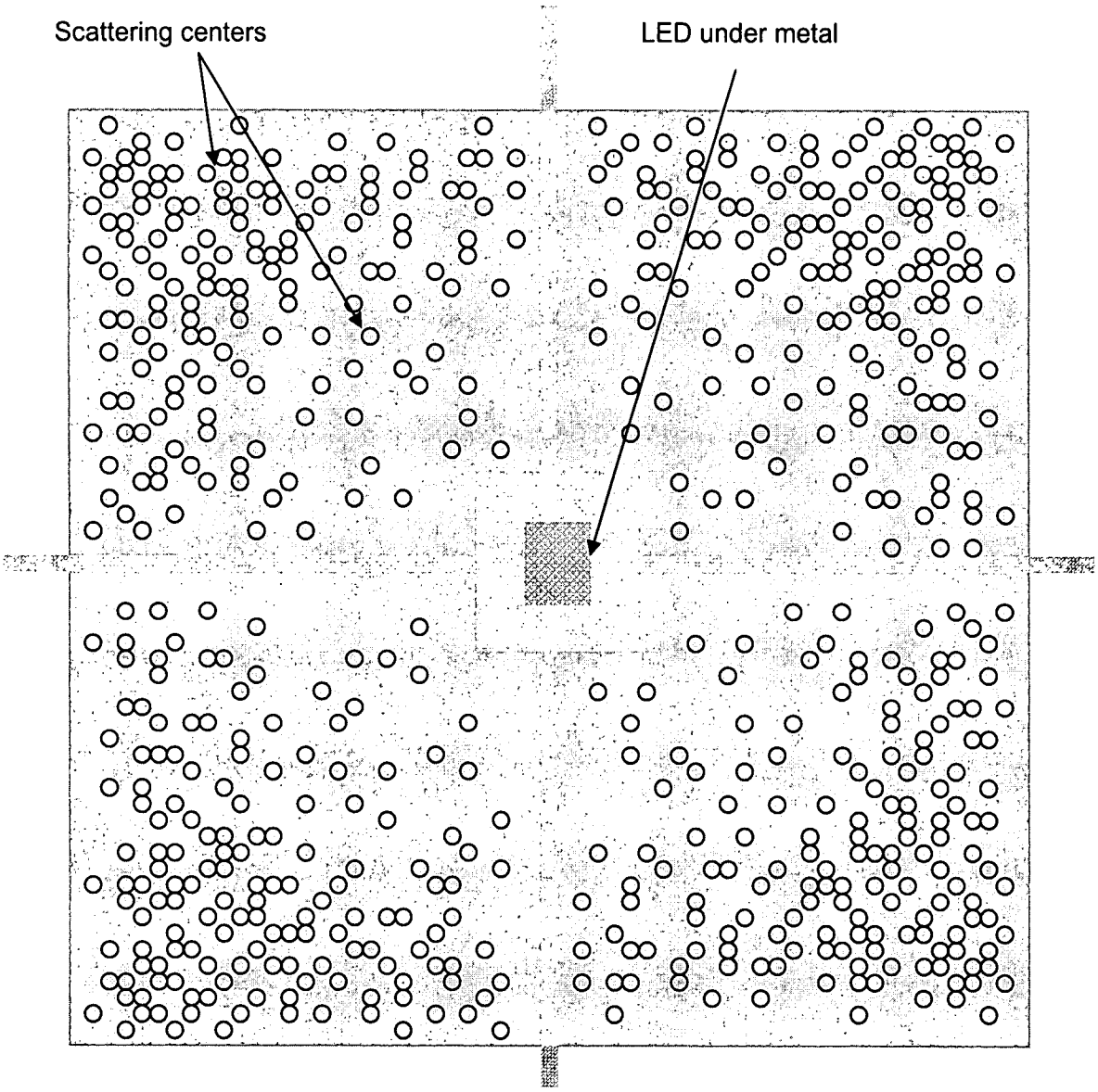


Fig. 12

Assume : Gaussian distribution



Scattering centers cross section: relief features in transparent substrate

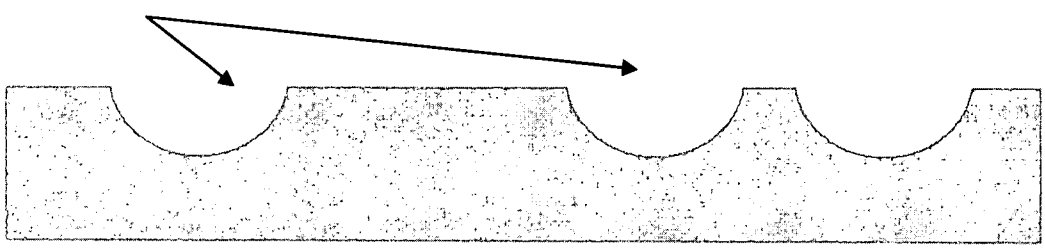
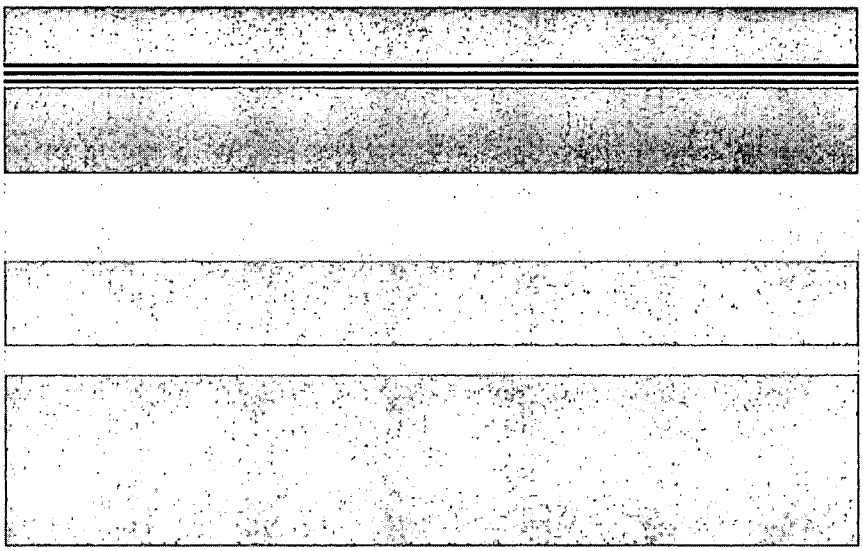
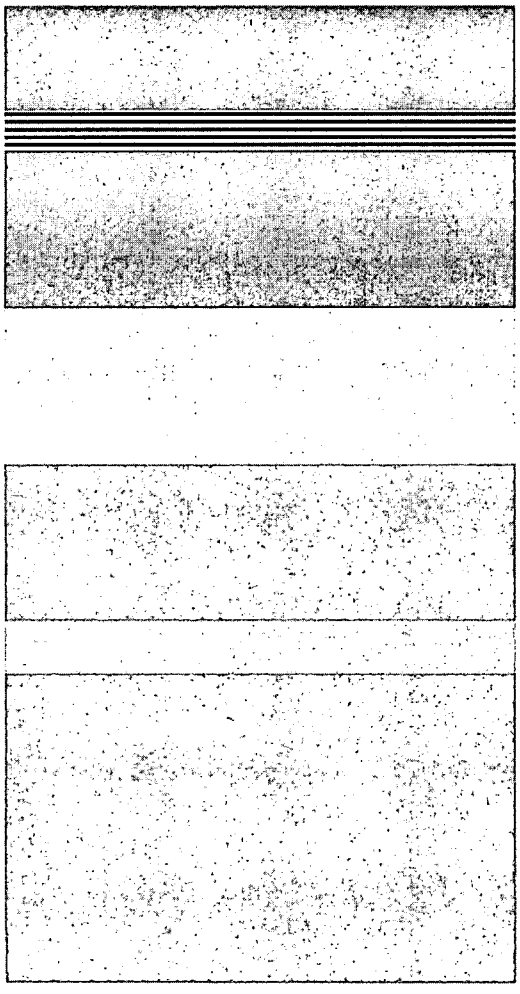


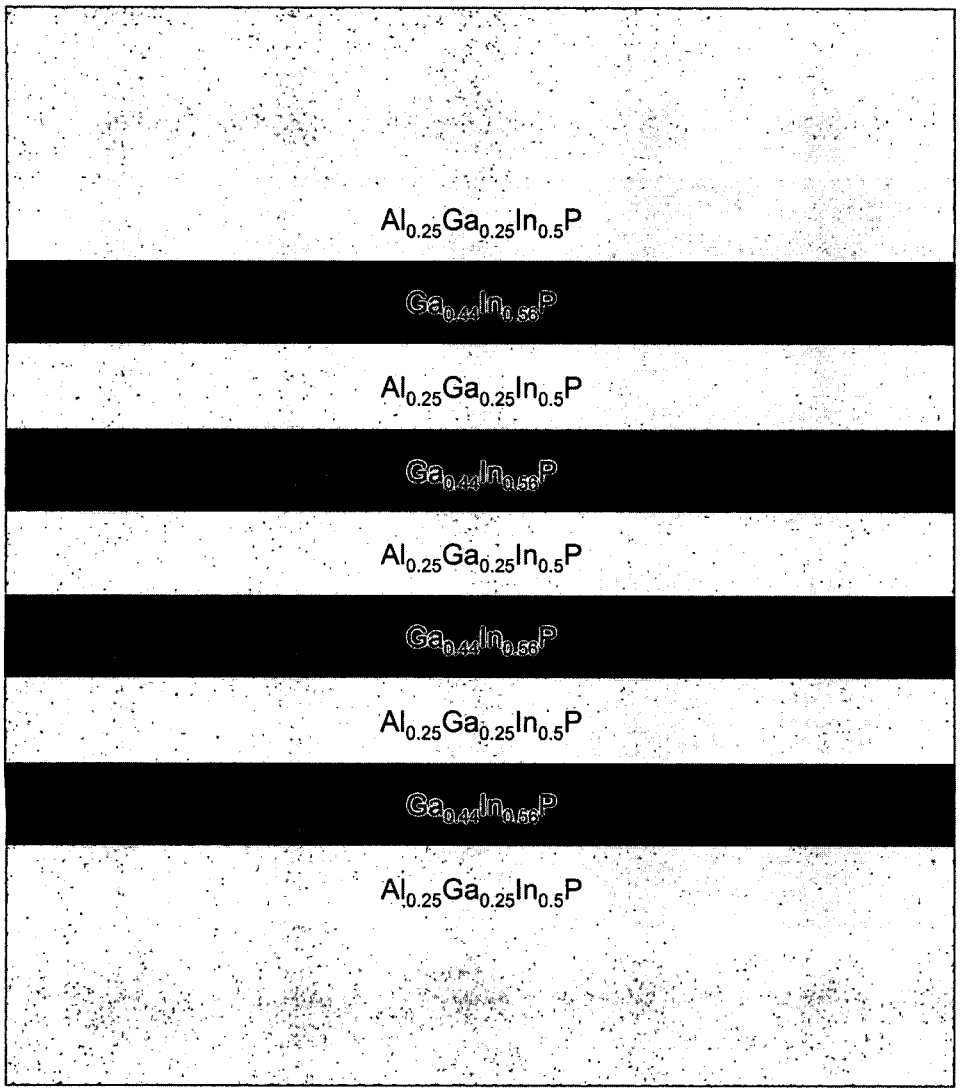
Fig. 13





1. GaAs:C, 5 nm p-contact layer; cap
2. $Al_{0.45}Ga_{0.55}As$:C, 800 nm p-contact and spreading layer
3. $Al_{0.5}In_{0.5}P$:Zn, 200 nm cladding layer
4-12. Cladding and Active region: see next slide for details
13. $Al_{0.5}In_{0.5}P$, 200 nm cladding
14. $Al_{0.45}Ga_{0.55}As$:Si, 800 nm n-spreading layer
15. GaAs:Si, 500 nm n-contact layer
16. $Al_{0.96}Ga_{0.04}As$, 1500 nm.
17. GaAs, 1500 nm
18. $Al_{0.96}Ga_{0.04}As$, 500 nm
19. GaAs substrate

Fig. 14A



3. $Al_{0.5}In_{0.5}P$:Mg, 200 nm p-cladding layer

4-12. From top to bottom, each layer 6 nm

$Al_{0.25}Ga_{0.25}In_{0.5}P$

$Ga_{0.44}In_{0.56}P$

$Al_{0.25}Ga_{0.25}In_{0.5}P$

$Ga_{0.44}In_{0.56}P$

$Al_{0.25}Ga_{0.25}In_{0.5}P$

$Ga_{0.44}In_{0.56}P$

$Al_{0.25}Ga_{0.25}In_{0.5}P$

$Ga_{0.44}In_{0.56}P$

$Al_{0.25}Ga_{0.25}In_{0.5}P$

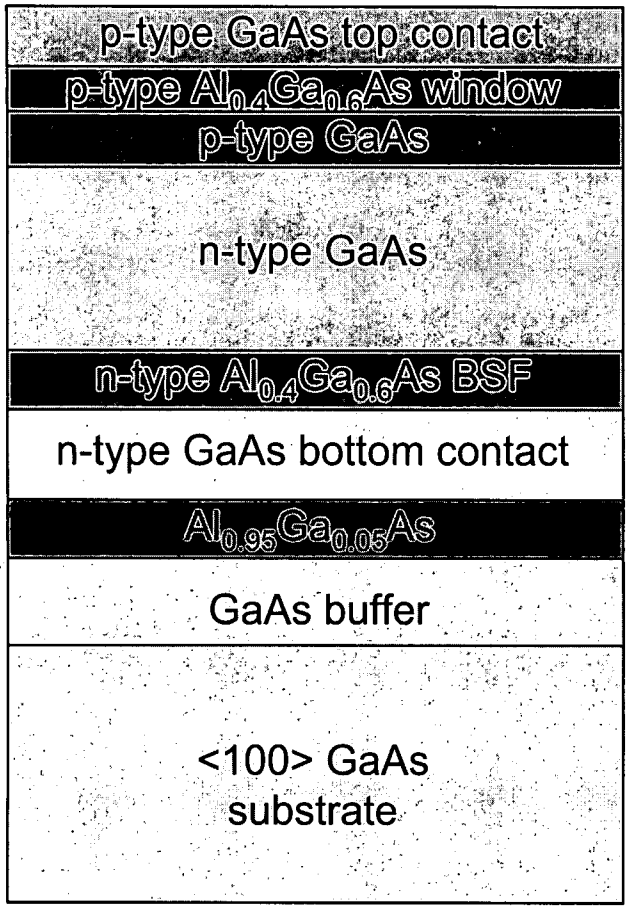
13. $Al_{0.5}In_{0.5}P$, 200 nm n-cladding layer

Fig. 14B

1	GaAs:C	5 nm	10^{19}	P-contact
2	$Al_{0.45}Ga_{0.55}As$:C	800 nm	10^{18}	P-spreader
3	$Al_{0.5}In_{0.5}P$:Zn	200 nm	3×10^{17}	Cladding
4	$Al_{0.25}Ga_{0.25}In_{0.5}P$	6 nm	Undoped	Barrier
5	$Ga_{0.44}In_{0.56}P$	6 nm	Undoped	Q-well
6	$Al_{0.25}Ga_{0.25}In_{0.5}P$	6 nm	Undoped	Barrier
7	$Ga_{0.44}In_{0.56}P$	6 nm	Undoped	Q-well
8	$Al_{0.25}Ga_{0.25}In_{0.5}P$	6 nm	Undoped	Barrier
9	$Ga_{0.44}In_{0.56}P$	6 nm	Undoped	Q-well
10	$Al_{0.25}Ga_{0.25}In_{0.5}P$	6 nm	Undoped	Barrier
11	$Ga_{0.44}In_{0.56}P$	6 nm	Undoped	Q-well
12	$Al_{0.25}Ga_{0.25}In_{0.5}P$	6 nm	undoped	Barrier
13	$Al_{0.5}In_{0.5}P$	200 nm	10^{18}	Cladding
14	$Al_{0.45}Ga_{0.55}As$:Si	800 nm	10^{18}	N-spreader
15	GaAs:Si	500 nm	$4x10^{18}$	N-contact
16	$Al_{0.96}Ga_{0.04}As$	1500 nm	10^{17}	N-doped
17	GaAs	1500 nm	10^{17}	N-doped
18	$Al_{0.96}Ga_{0.04}As$	500 nm	10^{17}	N-doped
19	GaAs	Substr.	$>10^{18}$	N-doped

Fig. 14C

✸ Structure of *p-on-n* type GaAs solar cell



9. p-type GaAs top contact layer
0.1 μm, Zn-doped, $8x10^{18}$ cm^{-3}

8. p-type $Al_{0.4}Ga_{0.6}As$ window layer
0.020 μm, C-doped, $5x10^{18}$ cm^{-3}

7. p-type GaAs layer (emitter)
0.3 μm, Zn-doped, $5x10^{18}$ cm^{-3}

6. n-type GaAs layer (base)
2 μm, Si-doped, $2x10^{17}$ cm^{-3}

5. n-type $Al_{0.4}Ga_{0.6}As$ back-surface-field layer
0.1 μm, Si-doped, $3x10^{18}$ cm^{-3}

4. n-type GaAs bottom contact layer
1.0 μm, Si-doped, $8x10^{18}$ cm^{-3}

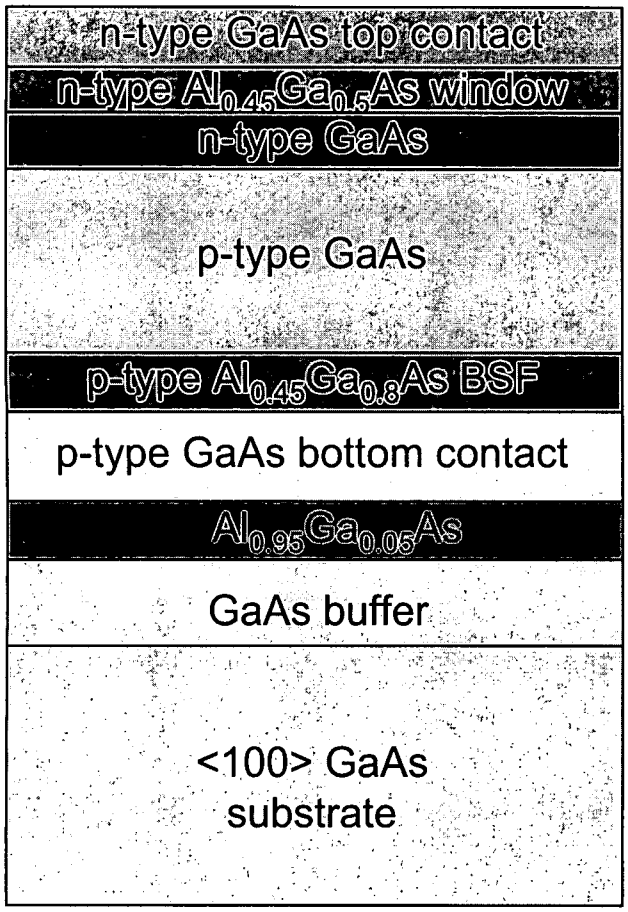
3. $Al_{0.96}Ga_{0.04}As$ sacrificial release layer
0.5 μm

2. GaAs buffer layer
0.2 μm

1. n-type GaAs substrate

Fig. 14D

✸ Structure of *n-on-p* type GaAs solar cell



9. n-type GaAs top contact layer
0.1 μm, Si-doped, $8x10^{18}$ cm^{-3}

8. n-type $Al_{0.45}Ga_{0.5}As$ window layer
0.050 μm, Si-doped, $3x10^{17}$ cm^{-3}

7. n-type GaAs layer
0.1 μm, Si-doped, $2x10^{18}$ cm^{-3}

6. p-type GaAs layer
2 μm, Zn-doped, $3x10^{17}$ cm^{-3}

5. p-type $Al_{0.45}Ga_{0.8}As$ back-surface-field layer
0.1 μm, C-doped, ~ $1x10^{19}$ cm^{-3}

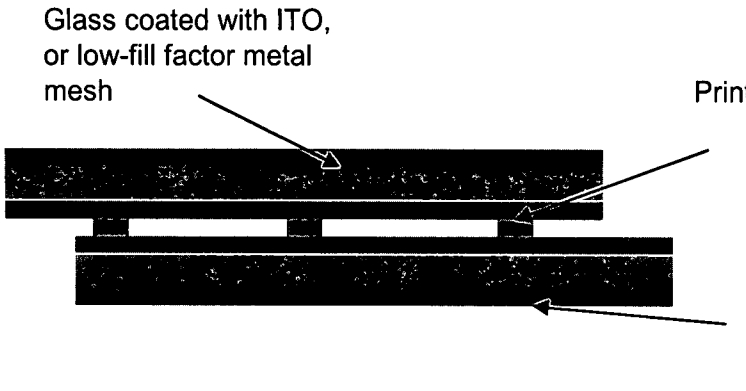
4. p-type GaAs bottom contact layer
1.0 μm, C-doped, $2x10^{18}$ cm^{-3}

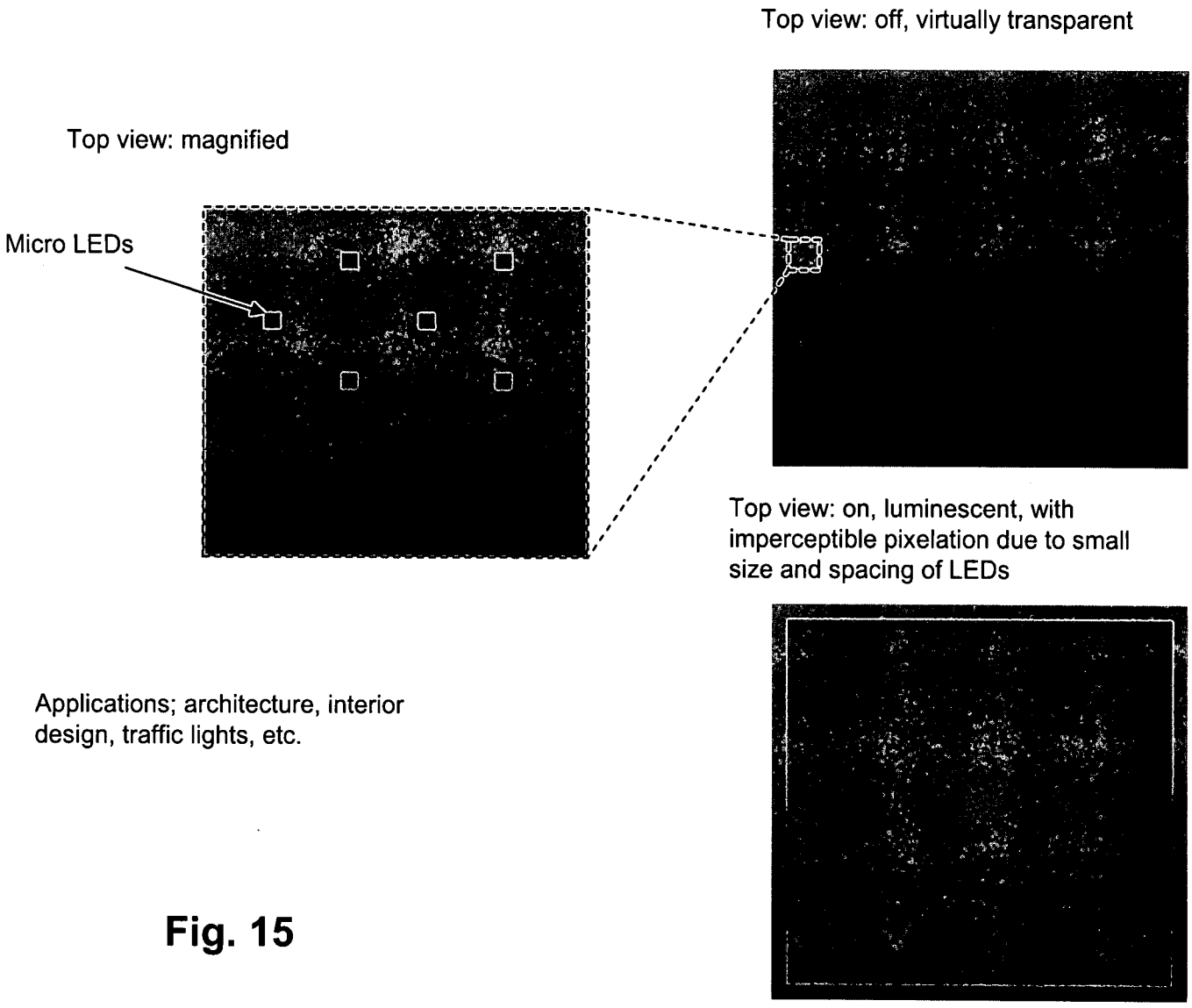
3. Al0.96GaAs sacrificial release layer
0.5 μm

2. GaAs buffer layer
0.2 μm

1. GaAs substrate

Fig. 14E





Applications; architecture, interior design, traffic lights, etc.

Fig. 15

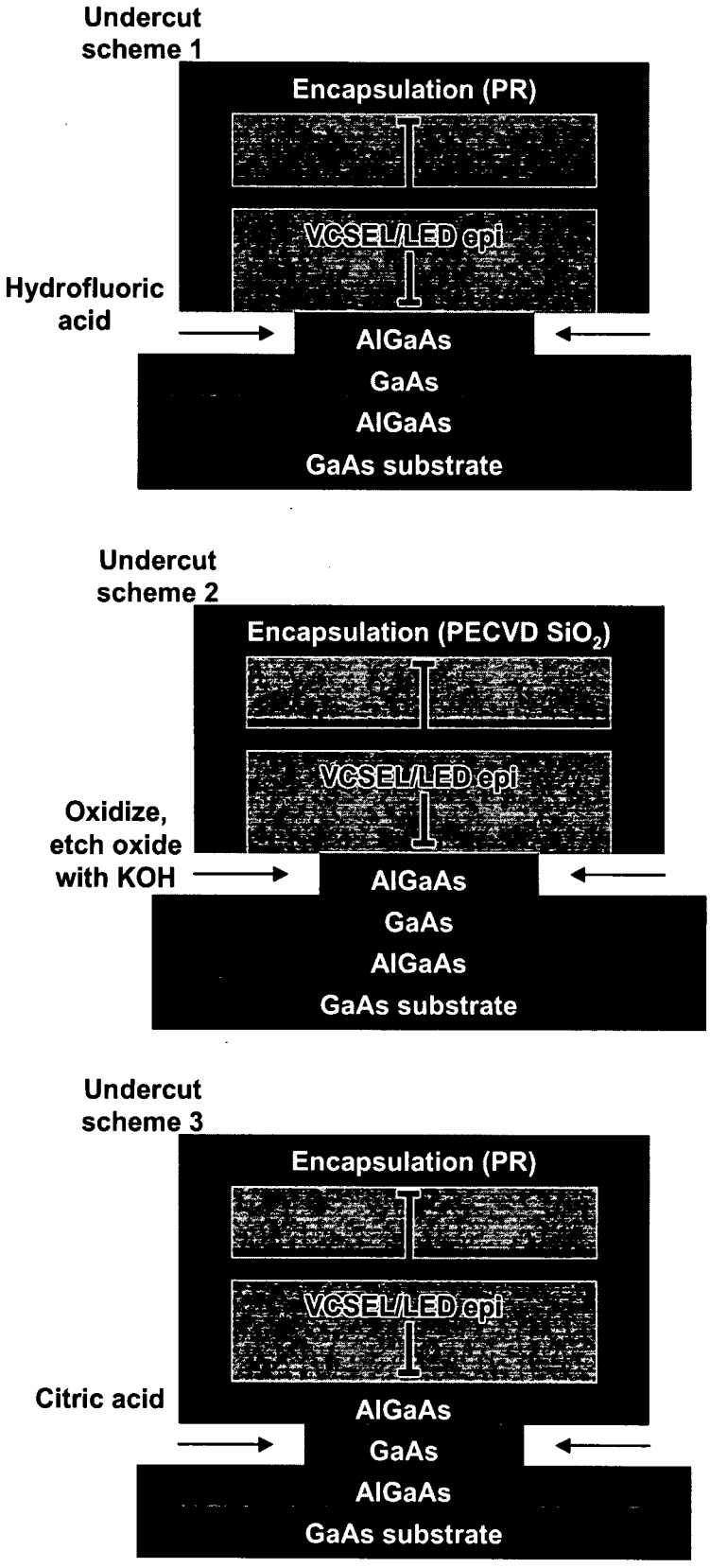

Undercut scheme 1
Encapsulation (PR)
VCSEL/LED epi
Hydrofluoric acid
AlGaAs
GaAs
AlGaAs
GaAs substrate
Undercut scheme 2
Encapsulation (PECVD SiO_2)
VCSEL/LED epi
Oxidize, etch oxide with KOH
AlGaAs
GaAs
AlGaAs
GaAs substrate
Undercut scheme 3
Encapsulation (PR)
VCSEL/LED epi
Citric acid
AlGaAs
GaAs
AlGaAs
GaAs substrate

Fig. 16

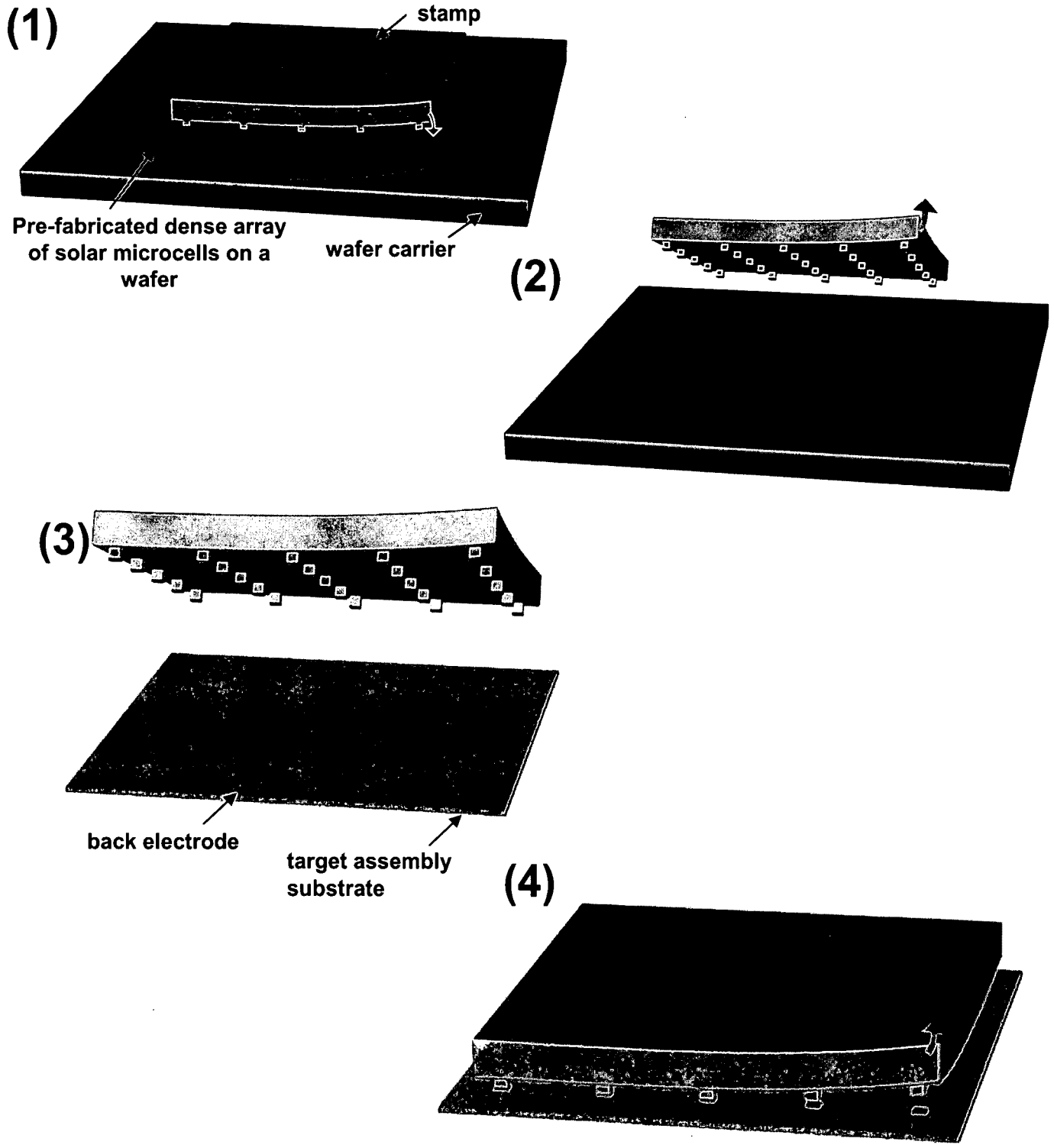

(1)
stamp
Pre-fabricated dense array of solar microcells on a wafer
wafer carrier
(2)
(3)
back electrode
target assembly substrate
(4)

Fig. 17A

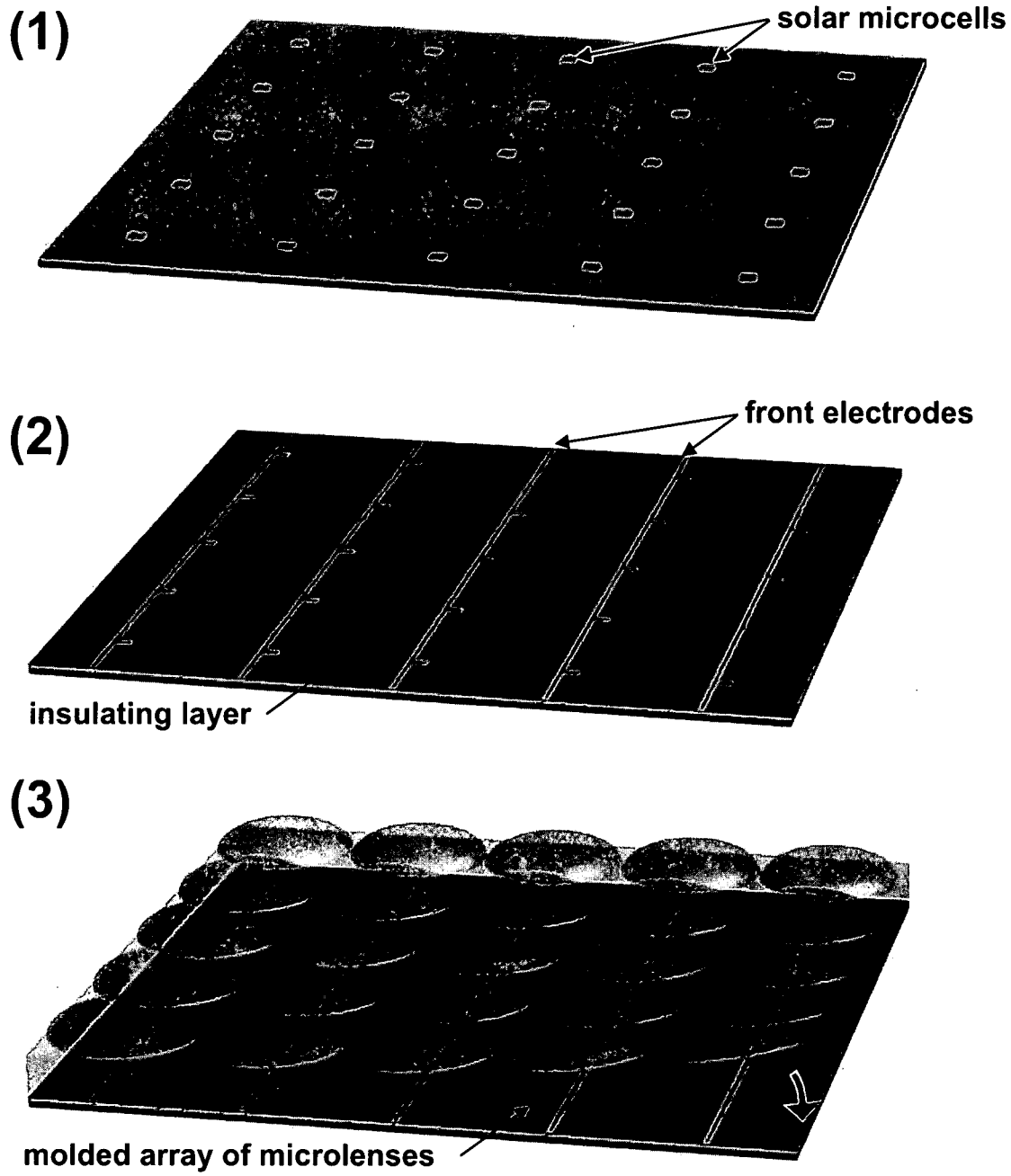
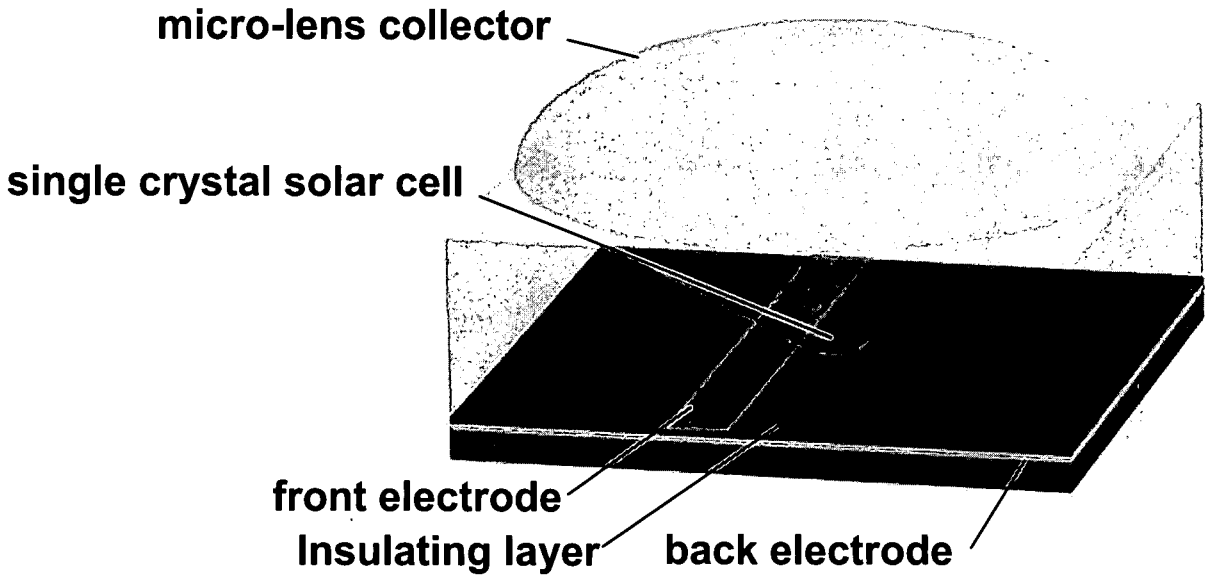

(1)
solar microcells
(2)
front electrodes
insulating layer
(3)
molded array of microlenses

Fig. 17B


micro-lens collector
single crystal solar cell
front electrode
Insulating layer
back electrode

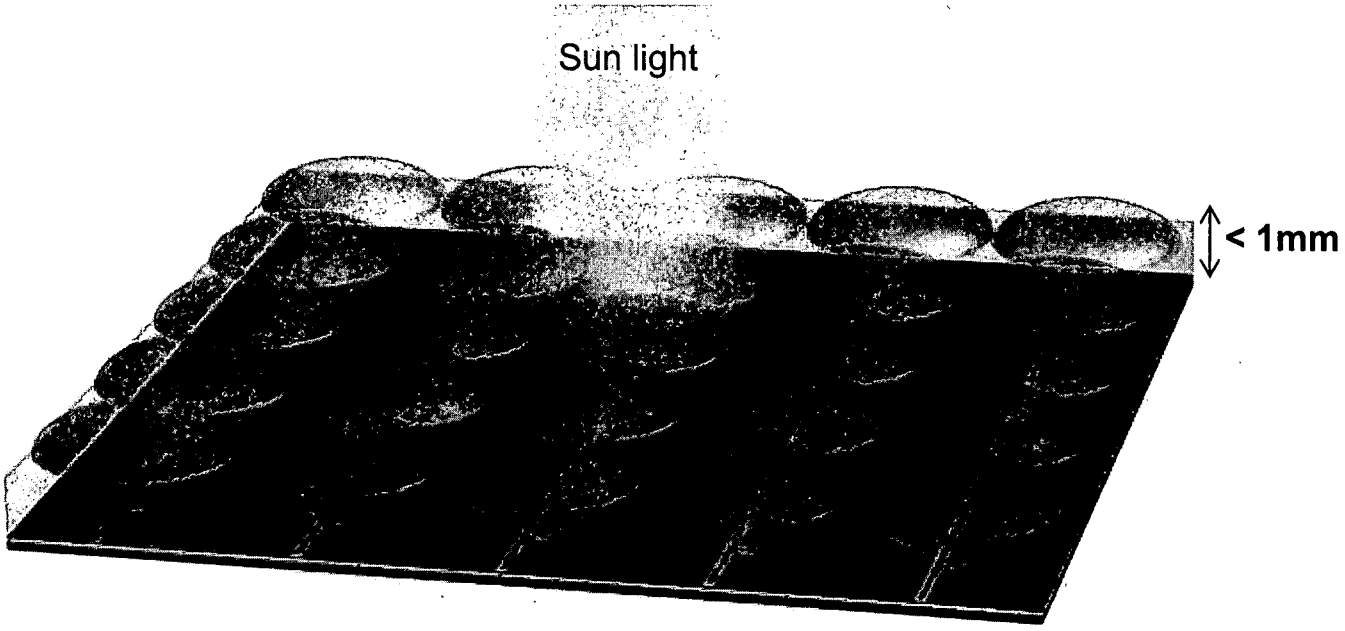

Sun light
< 1mm

Fig. 17C

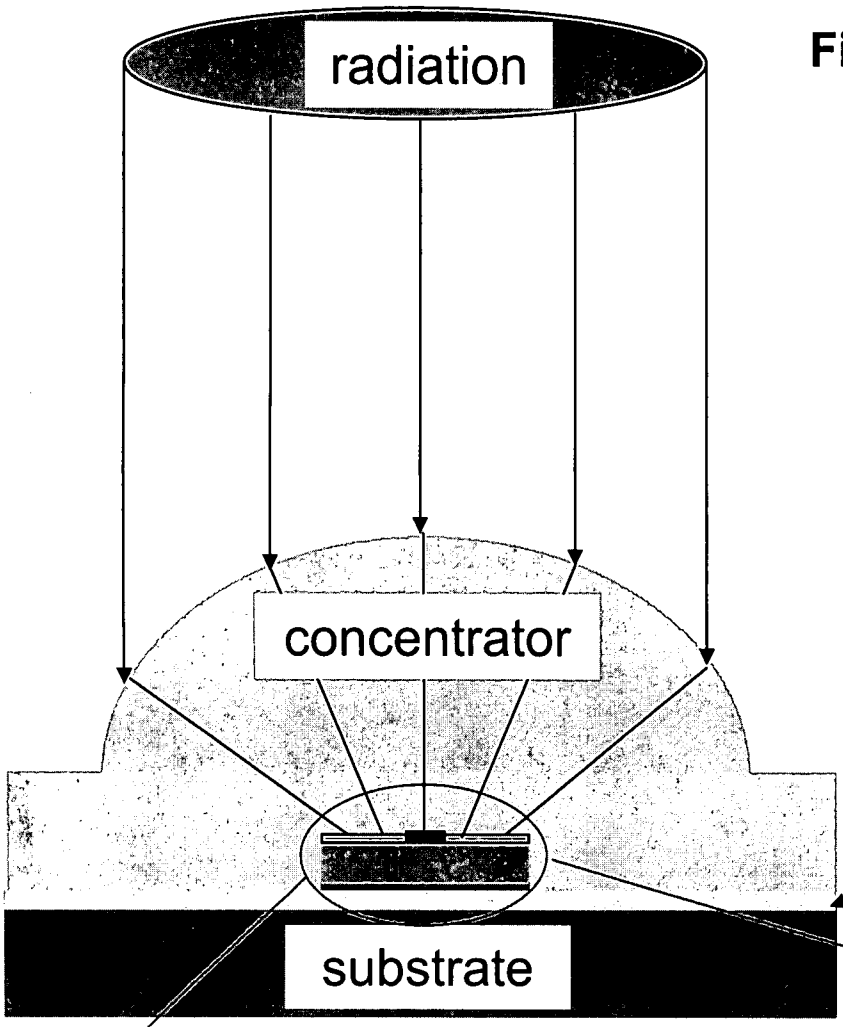
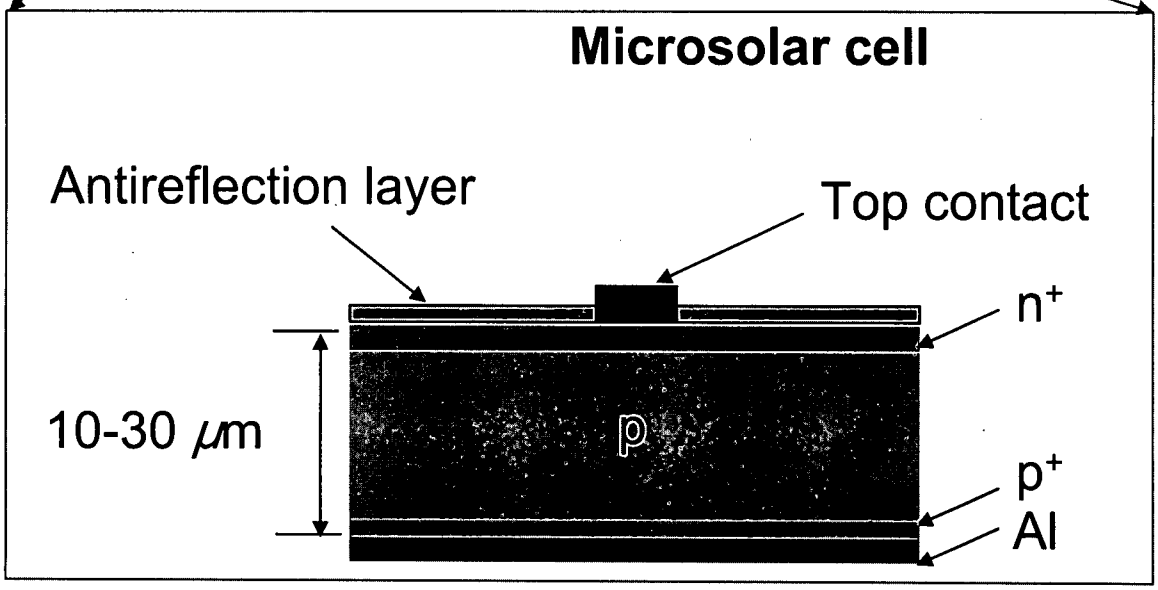
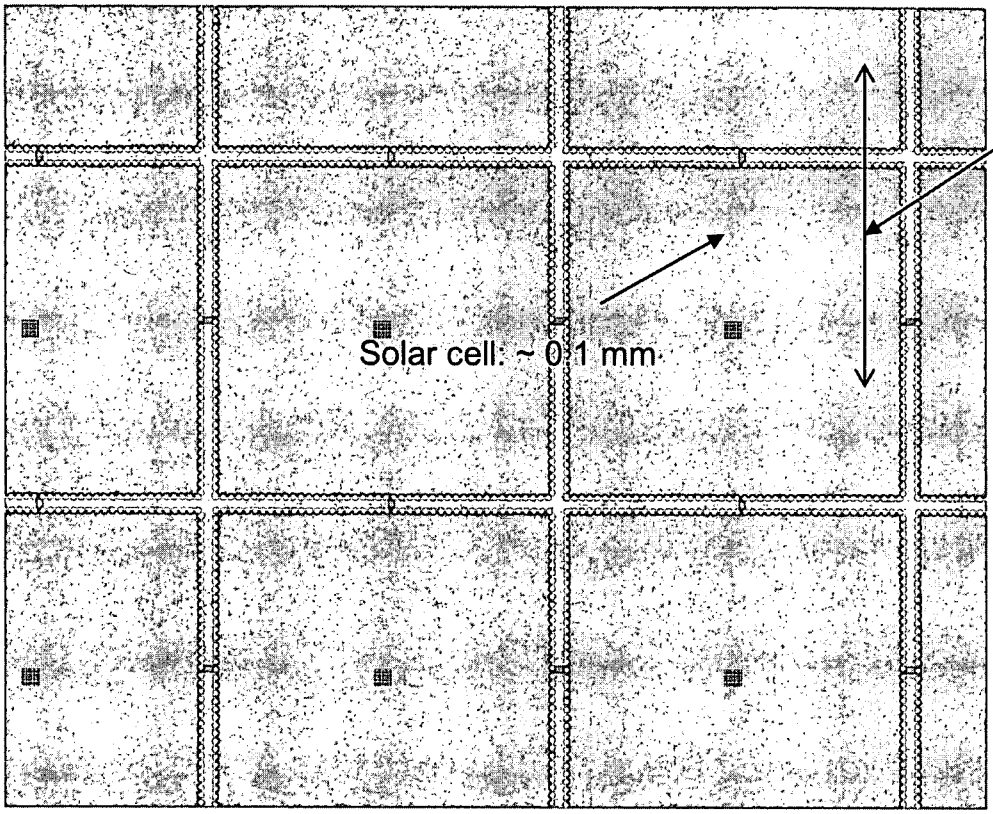


Fig. 18A

Not to scale

Fig. 18B





$$Area_Multiplication = \frac{Collector_Area}{SolarCell_Area} = \sim 400$$

1 ft^2 of processed semiconductor wafer → ~400 ft^2 of light-harvesting area.

Fig. 19

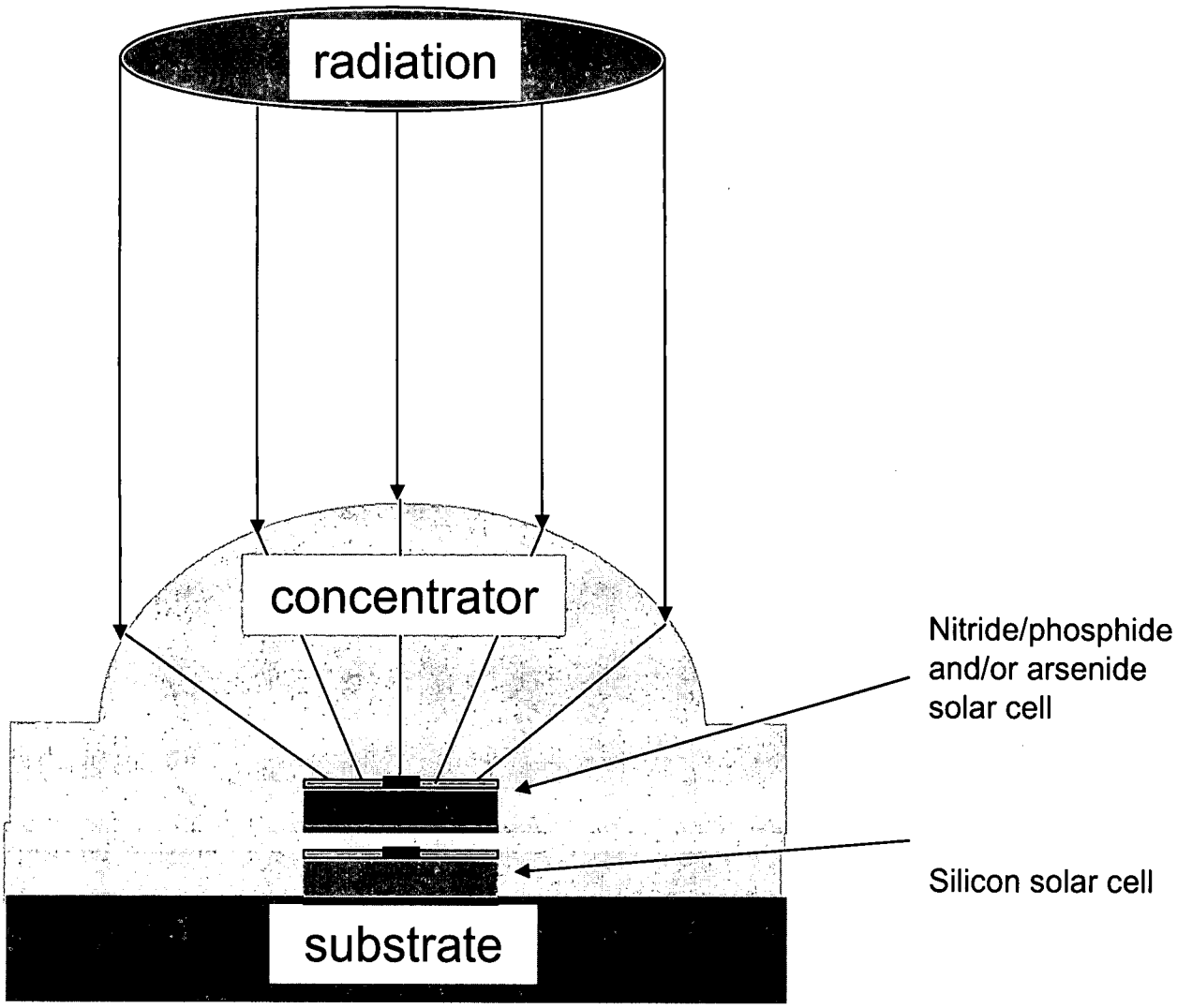

radiation
concentrator
Nitride/phosphide and/or arsenide solar cell
Silicon solar cell
substrate

Fig. 20

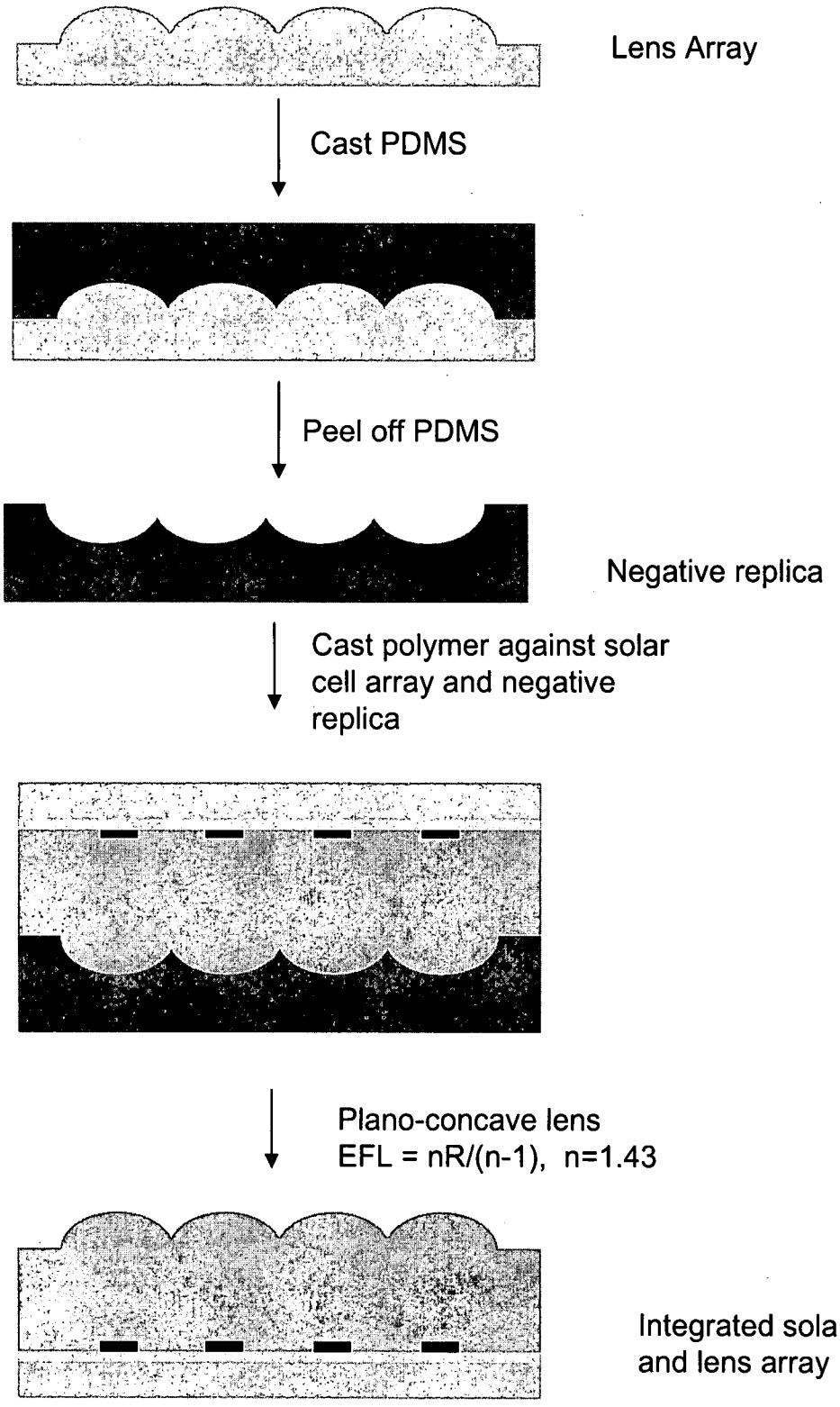

Lens Array
Cast PDMS
Peel off PDMS
Negative replica
Cast polymer against solar cell array and negative replica
Plano-concave lens
EFL = nR/(n-1), n=1.43
Integrated solar cell and lens array

Fig. 21

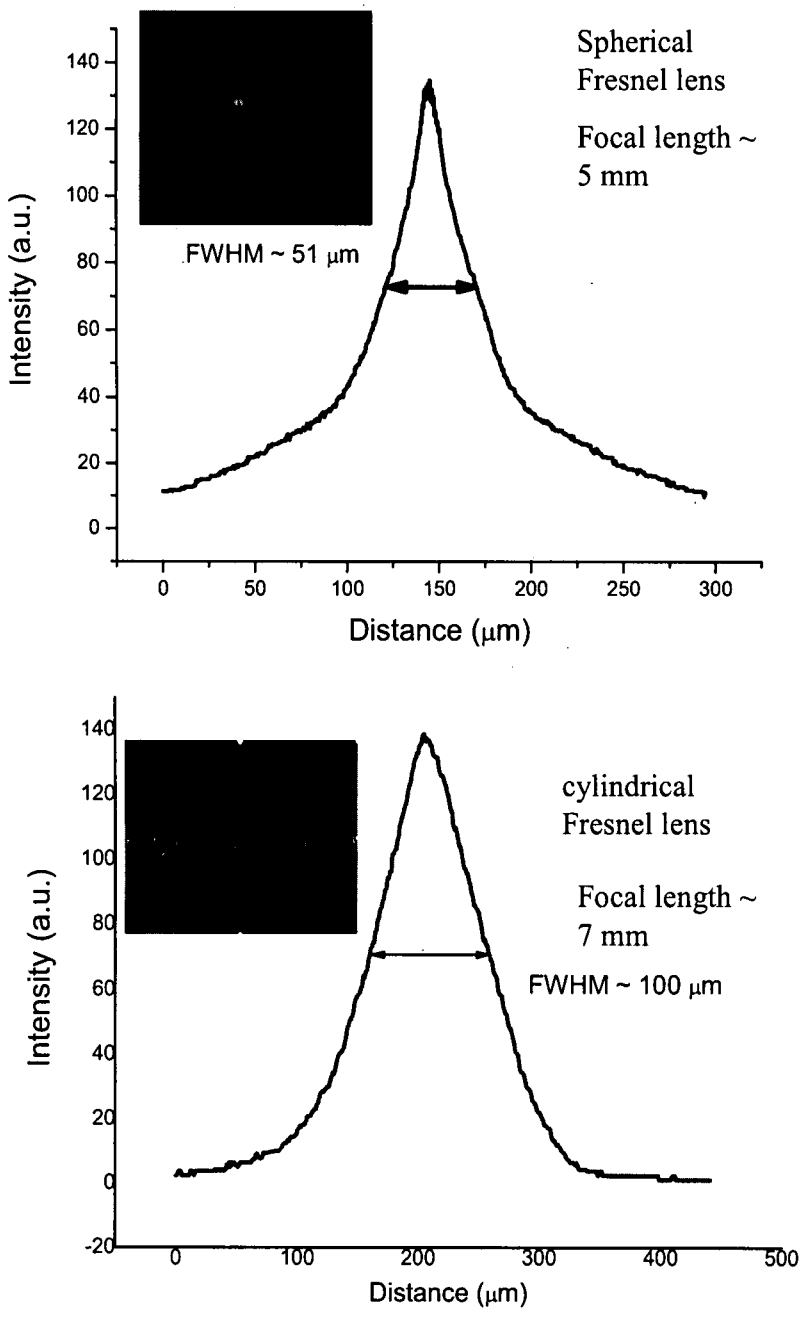

Spherical
Fresnel lens
Focal length ~
5 mm
FWHM ~ 51 μm
Intensity (a.u.)
Distance (μm)
cylindrical
Fresnel lens
Focal length ~
7 mm
FWHM ~ 100 μm
Intensity (a.u.)
Distance (μm)

Fig. 22

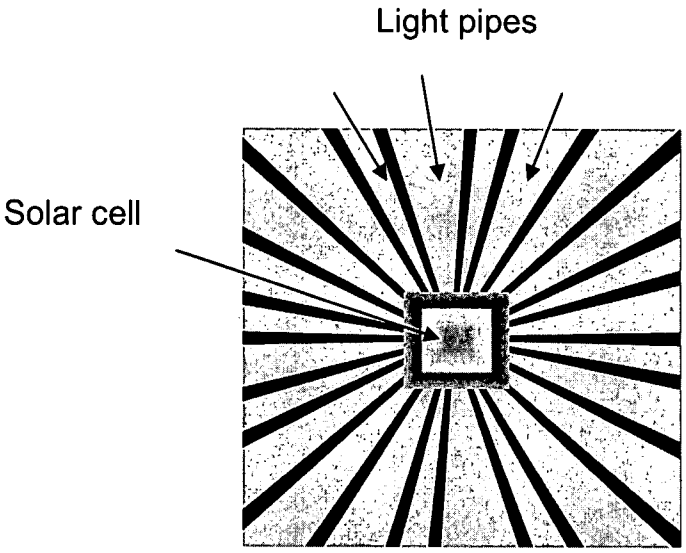


Fig. 23

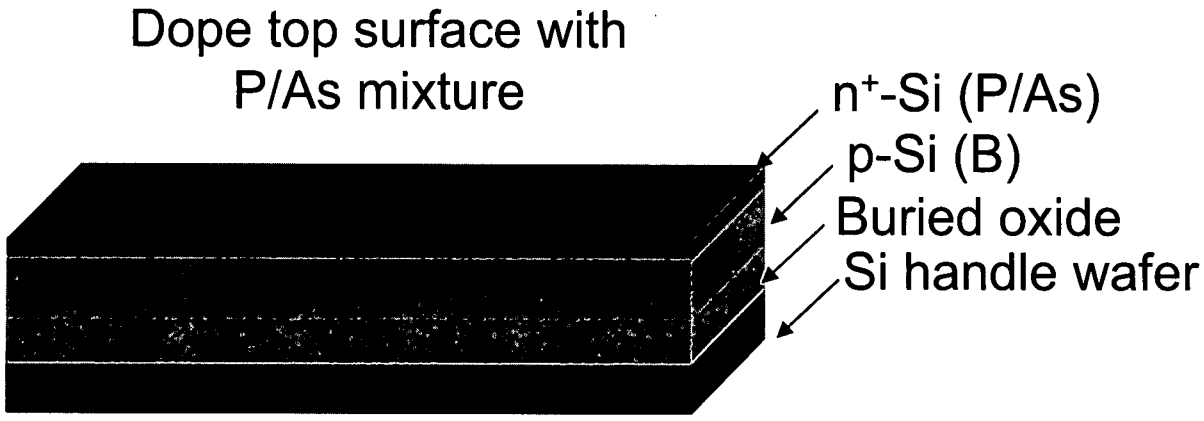

Dope top surface with
P/As mixture
n+-Si (P/As)
p-Si (B)
Buried oxide
Si handle wafer

Fig. 24

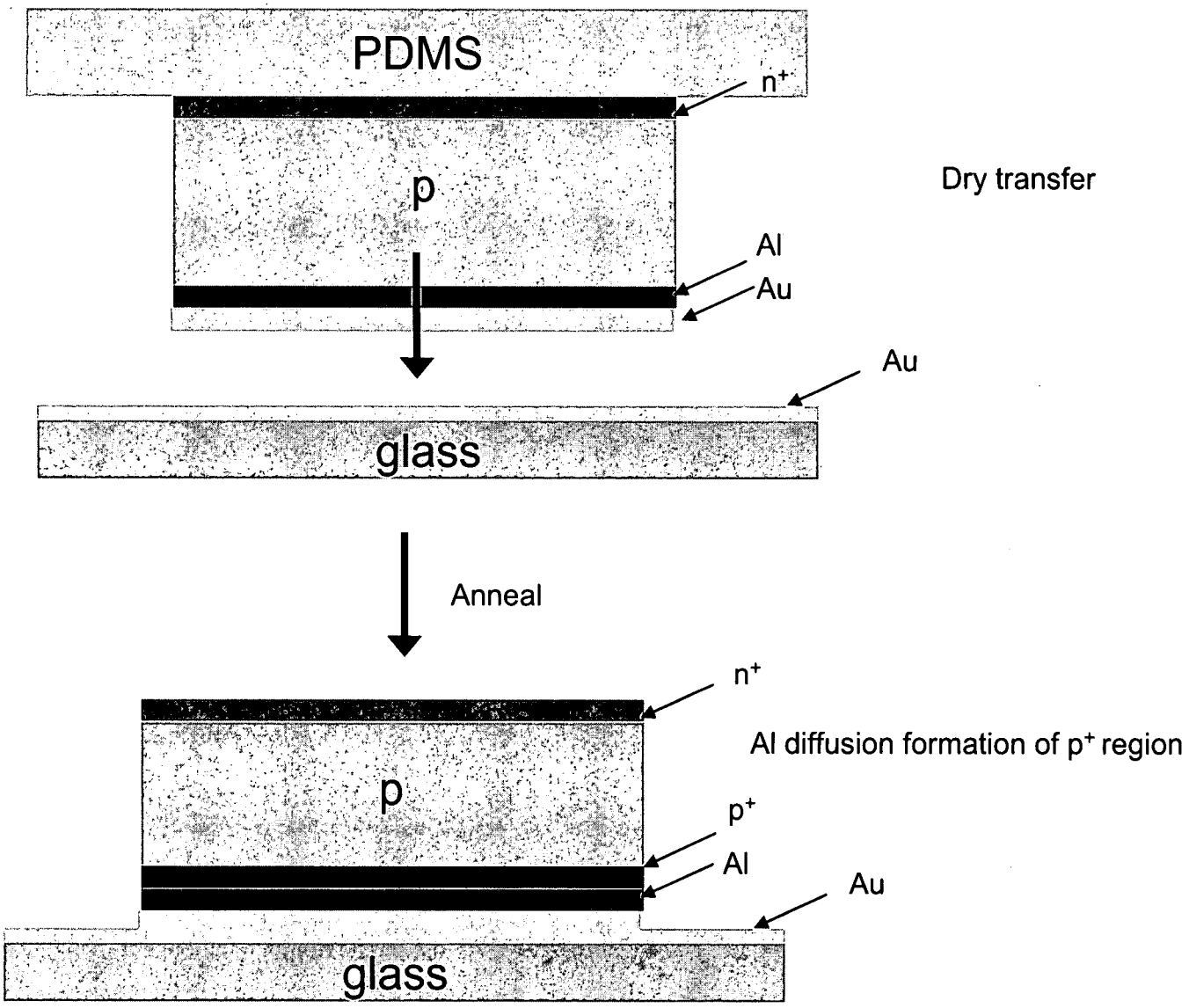
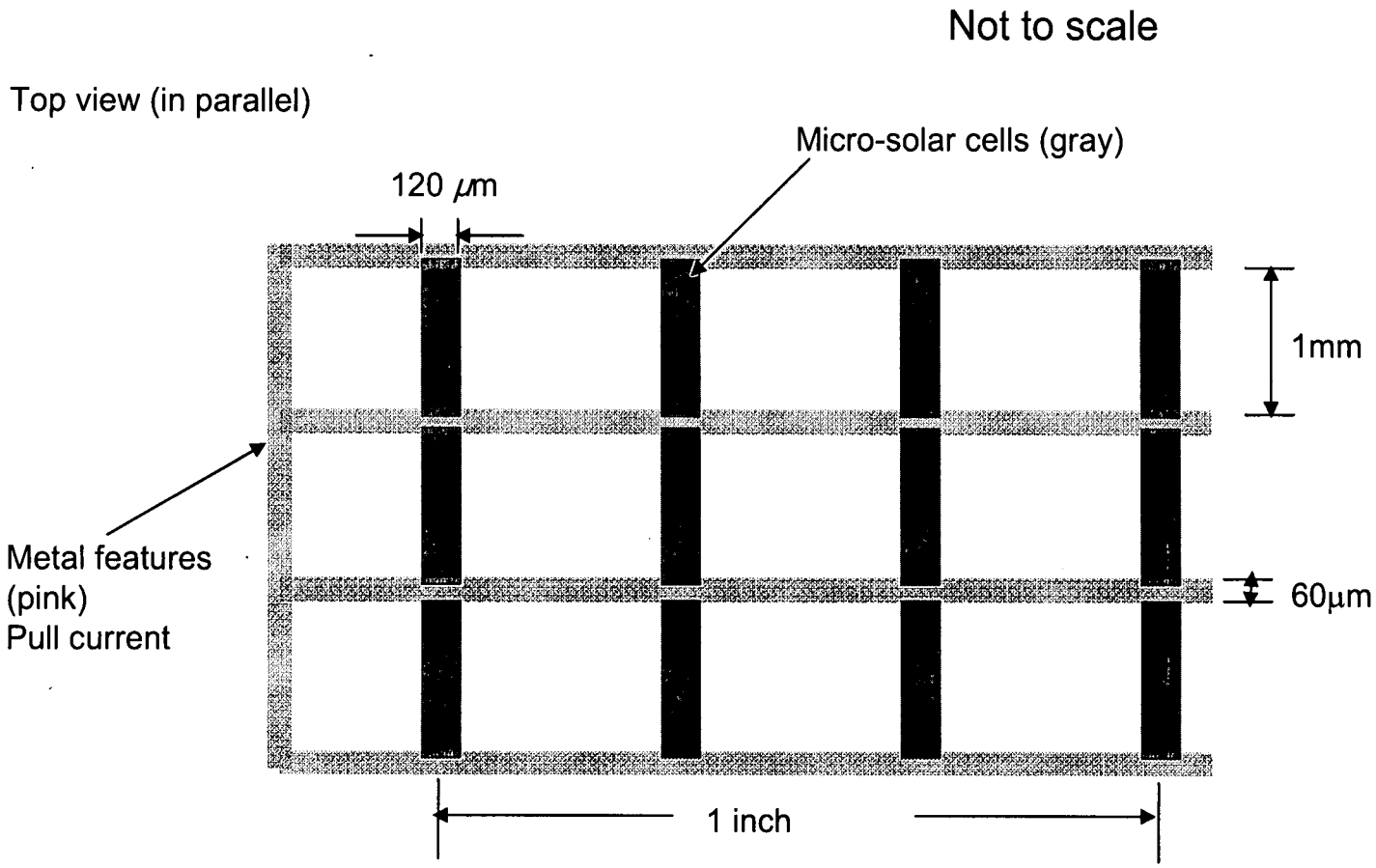

PDMS
n+
p
Al
Au
Dry transfer
Au
glass
Anneal
n+
Al diffusion formation of p+ region
p
p+
Al
Au
glass

Fig. 25



• Shadowing factor not too high!

Fig. 26

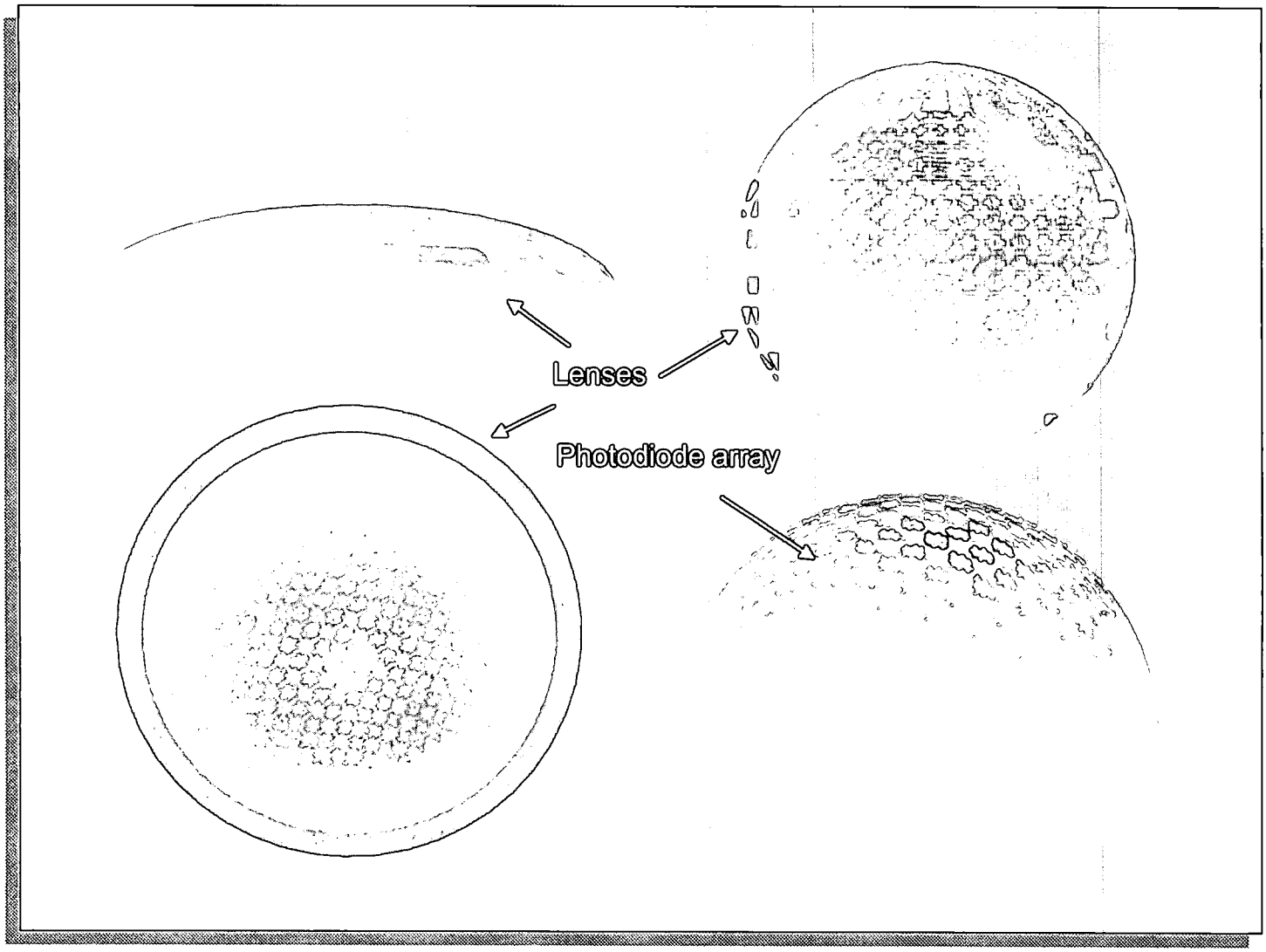


Fig. 27

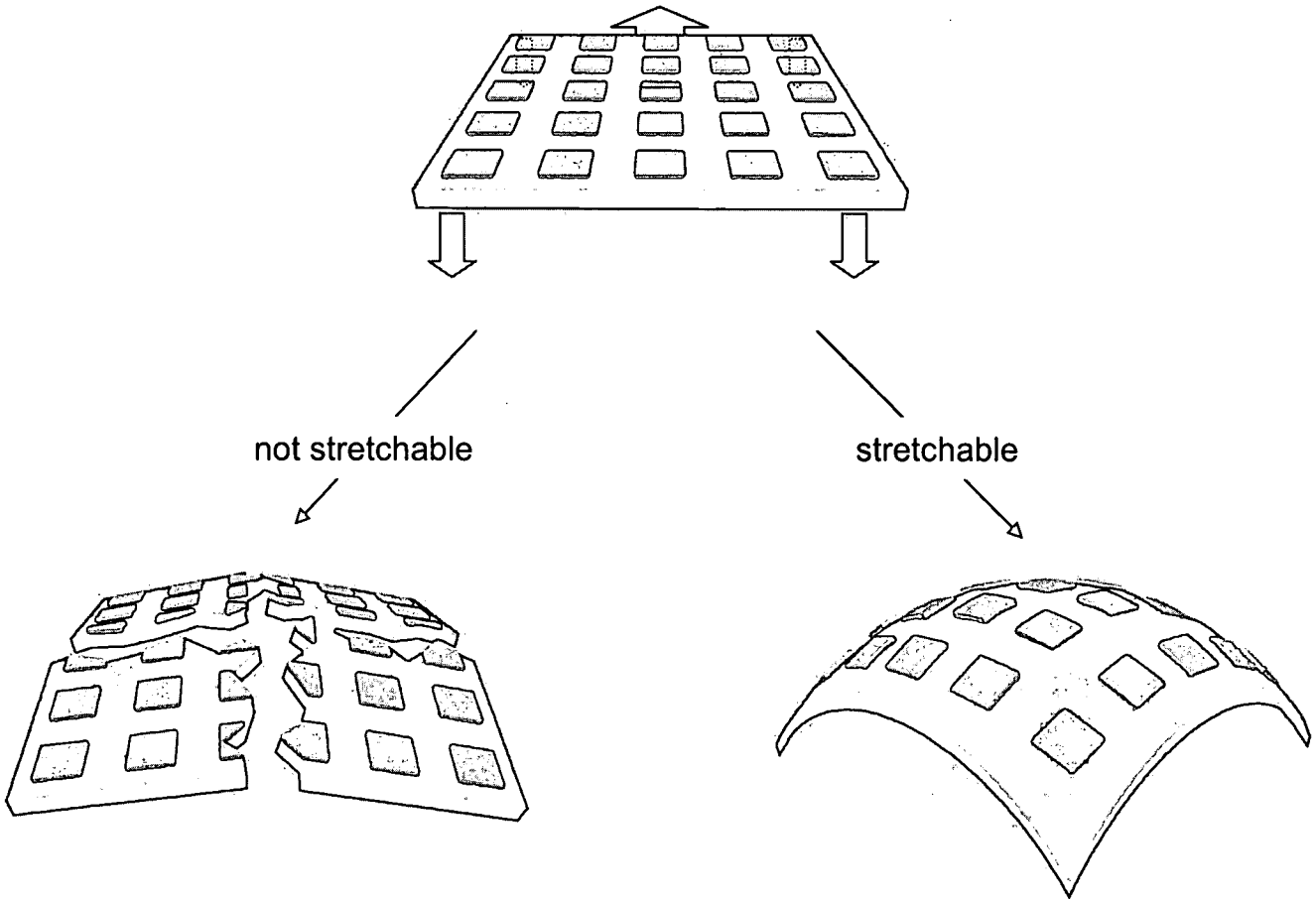


Fig. 28

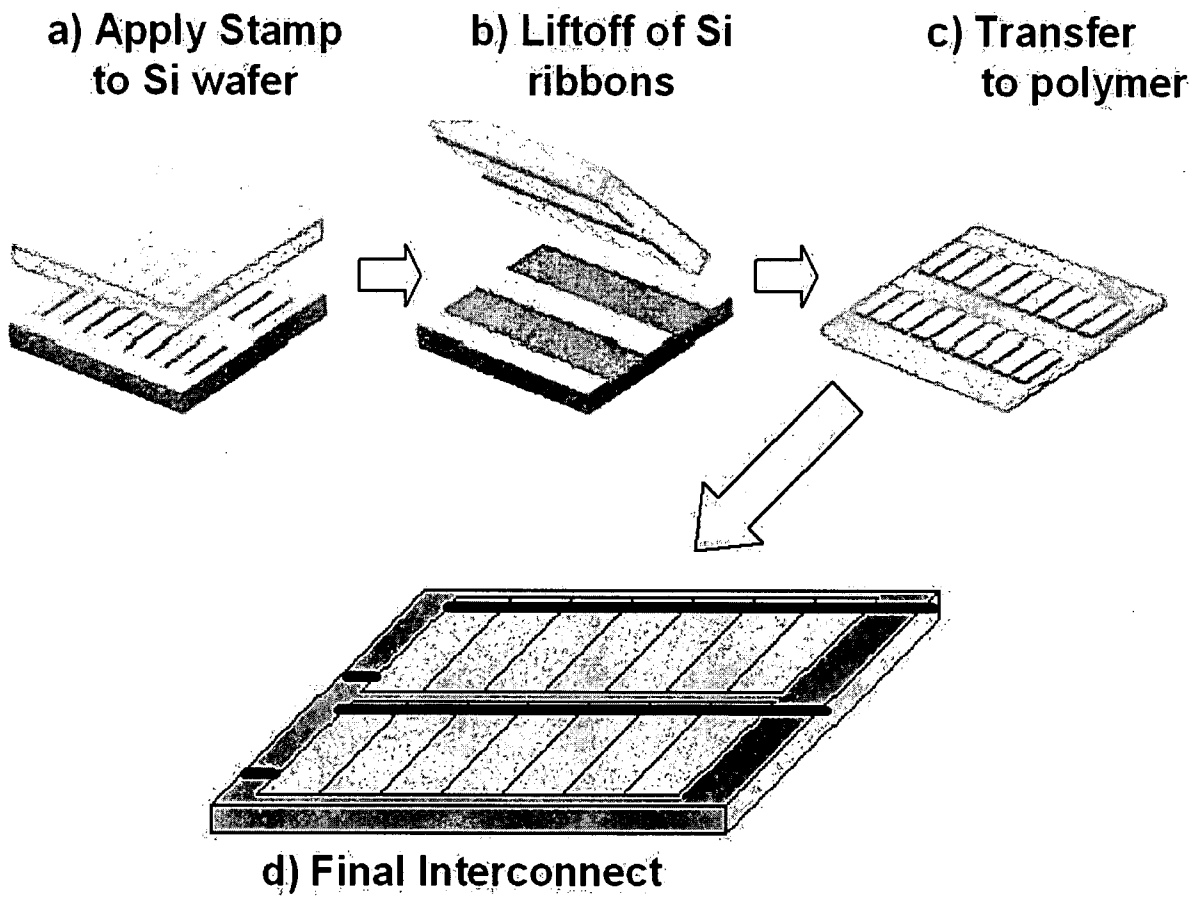

a) Apply Stamp to Si wafer
b) Liftoff of Si ribbons
c) Transfer to polymer
d) Final Interconnect

Fig. 29

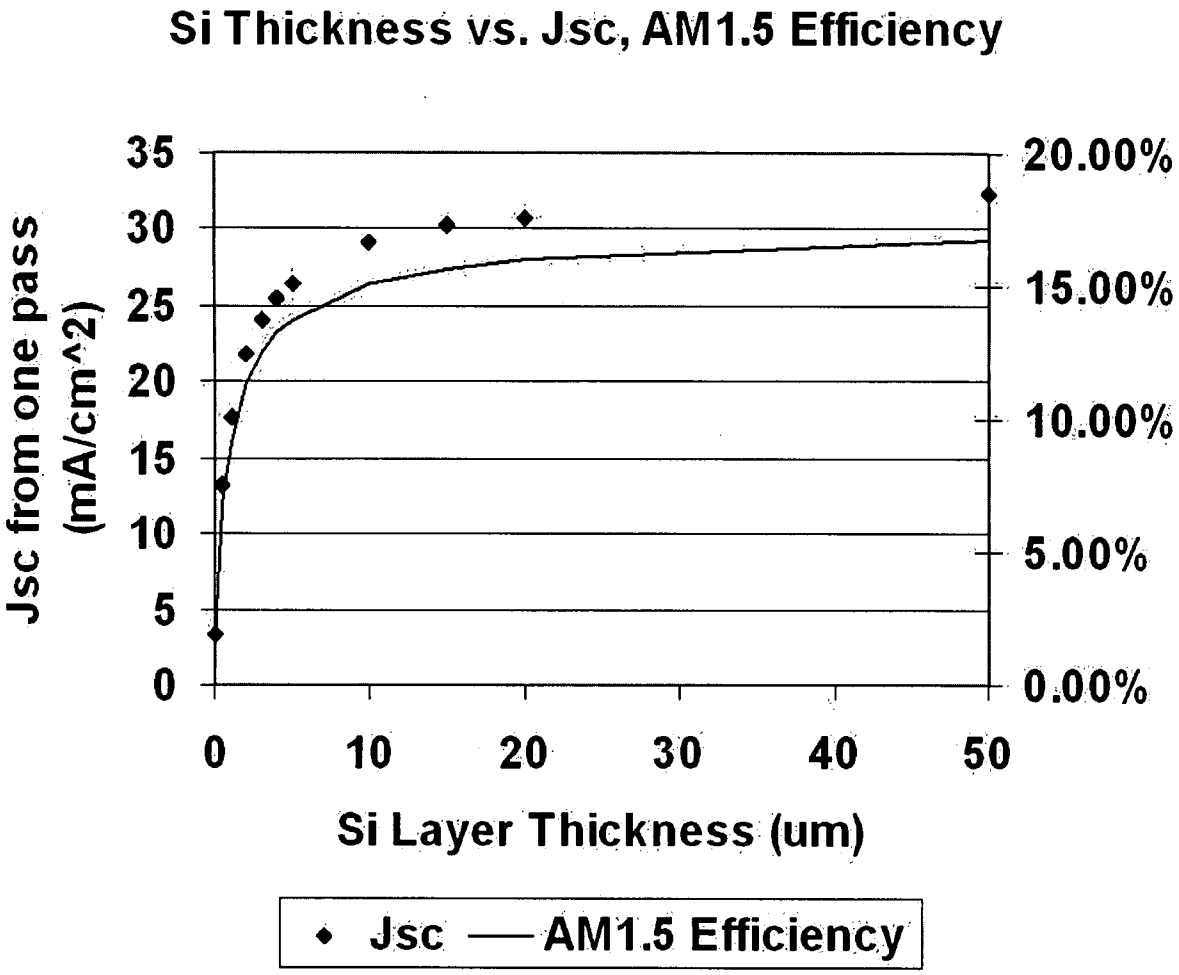

Si Thickness vs. Jsc, AM1.5 Efficiency
Jsc from one pass (mA/cm^2)
35
30
25
20
15
10
5
0
20.00%
15.00%
10.00%
5.00%
0.00%
0
10
20
30
40
50
Si Layer Thickness (um)
Jsc
AM1.5 Efficiency

Fig. 30

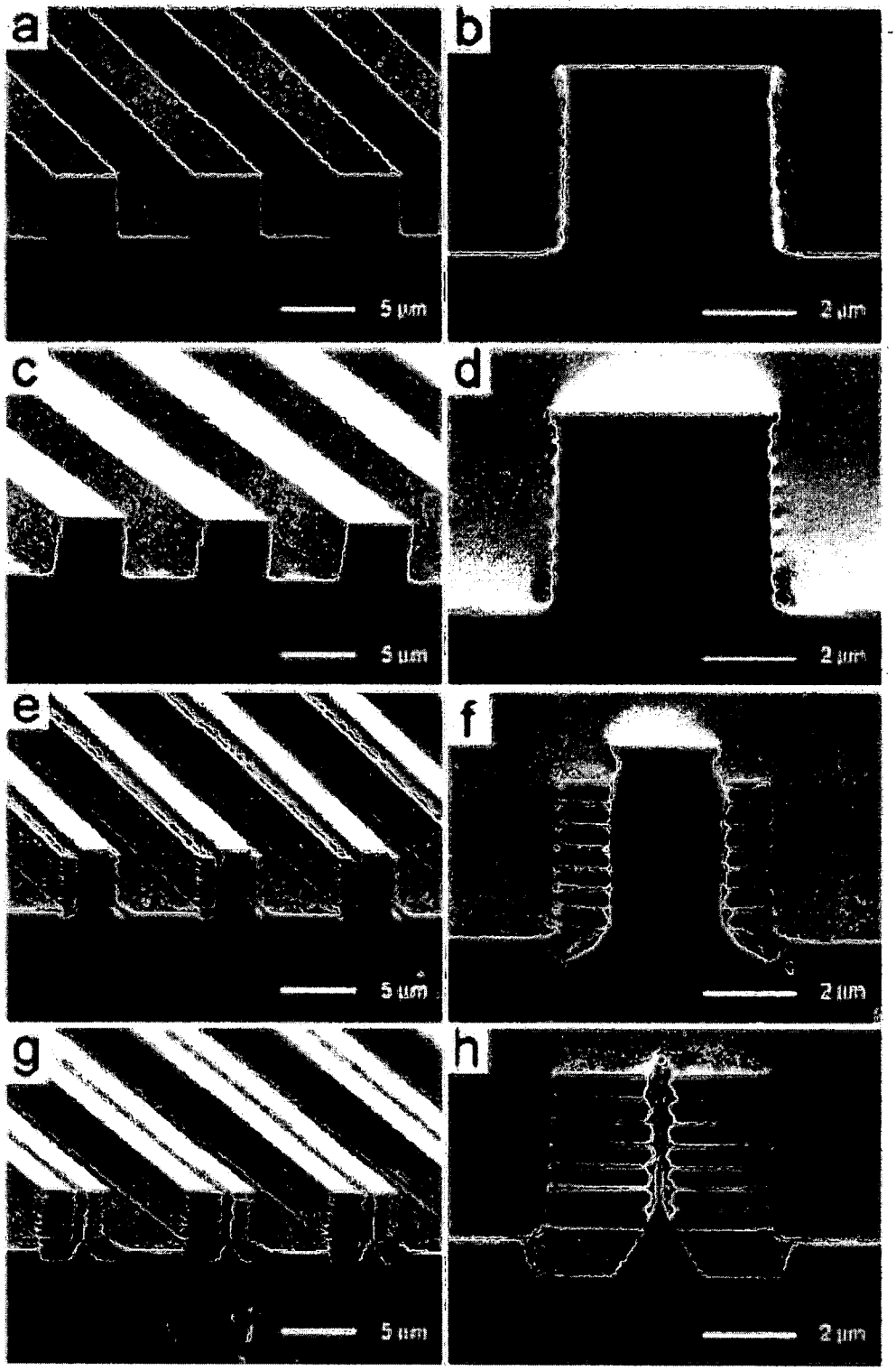


Fig. 31

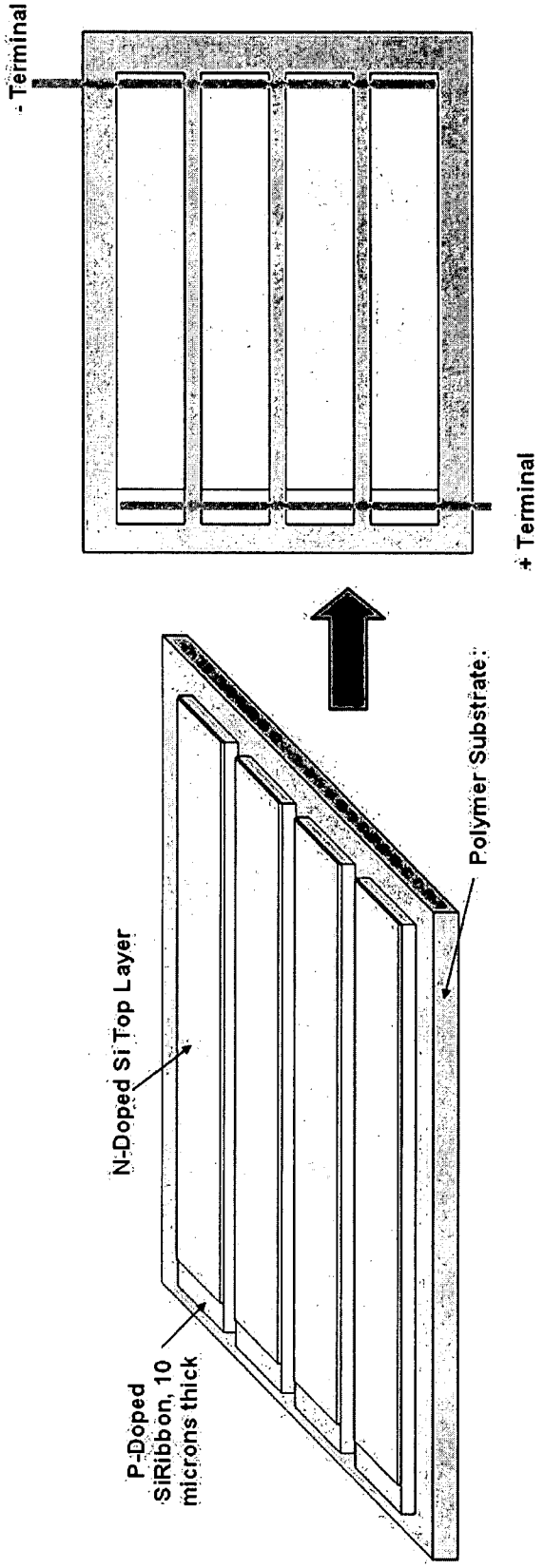

- Terminal
+ Terminal
Polymer Substrate
N-Doped Si Top Layer
P-Doped SiRibbon, 10 microns thick

Fig. 32

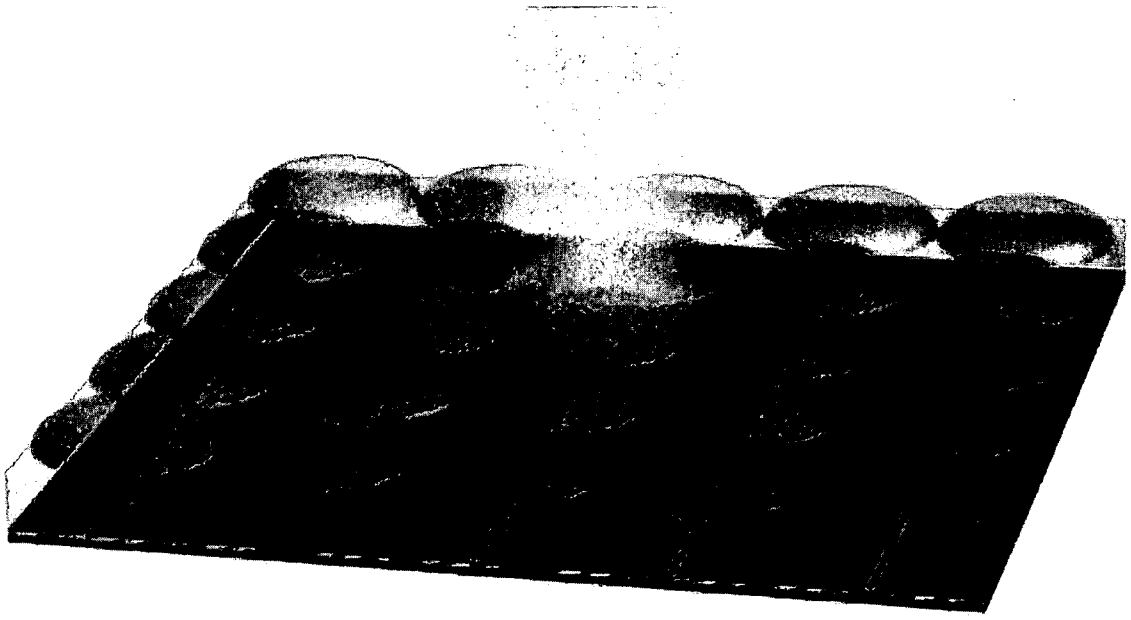


Fig. 33

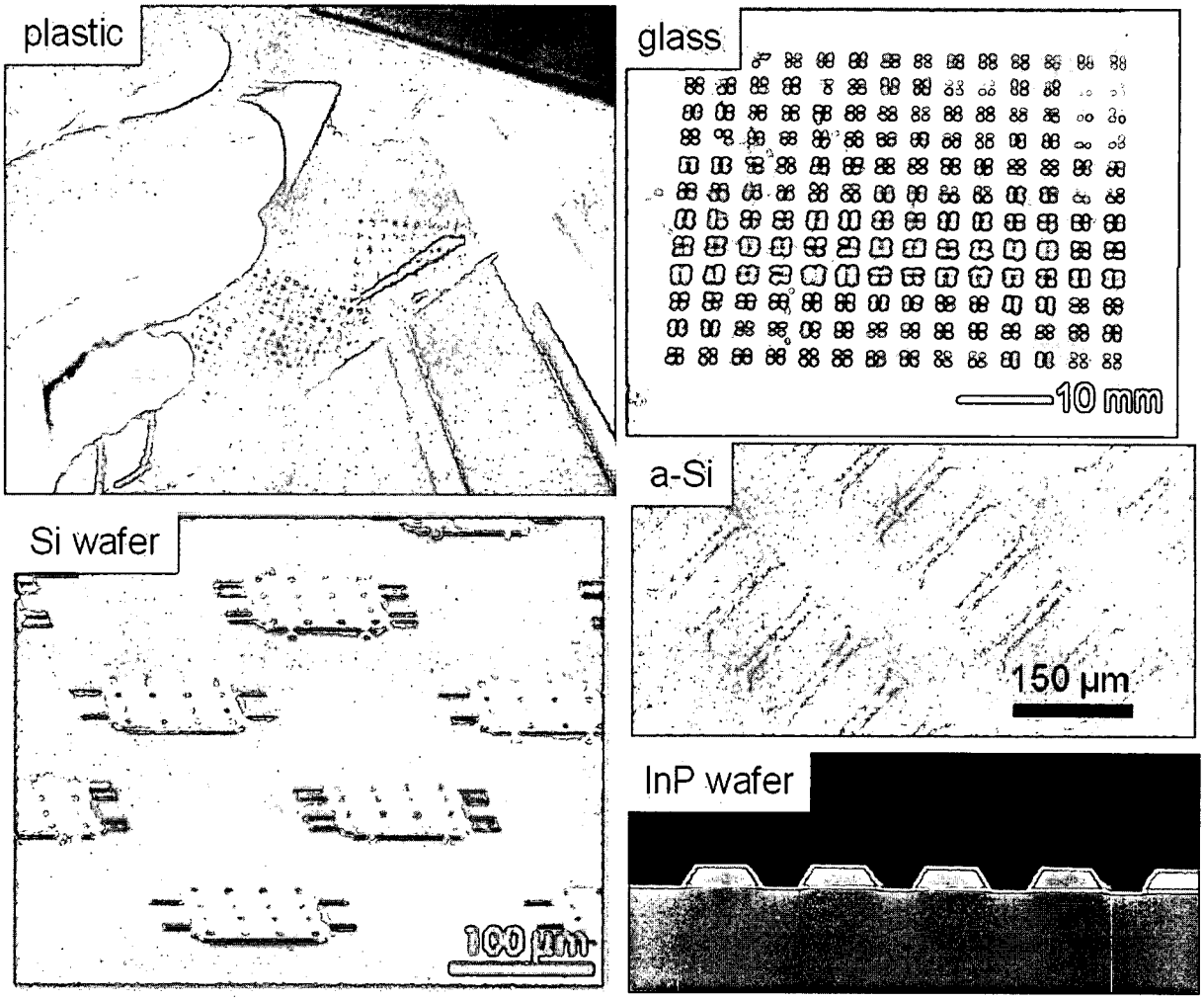


Fig. 34

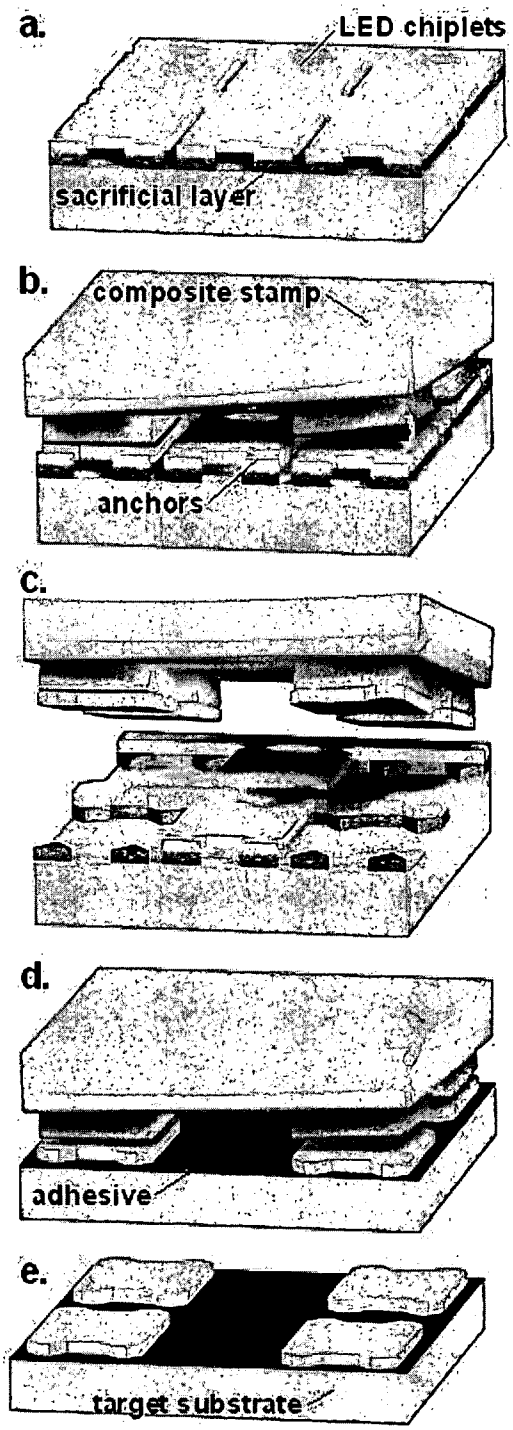

a.
LED chiplets
sacrificial layer
b.
composite stamp
anchors
c.
d.
adhesive
e.
target substrate

Fig. 35

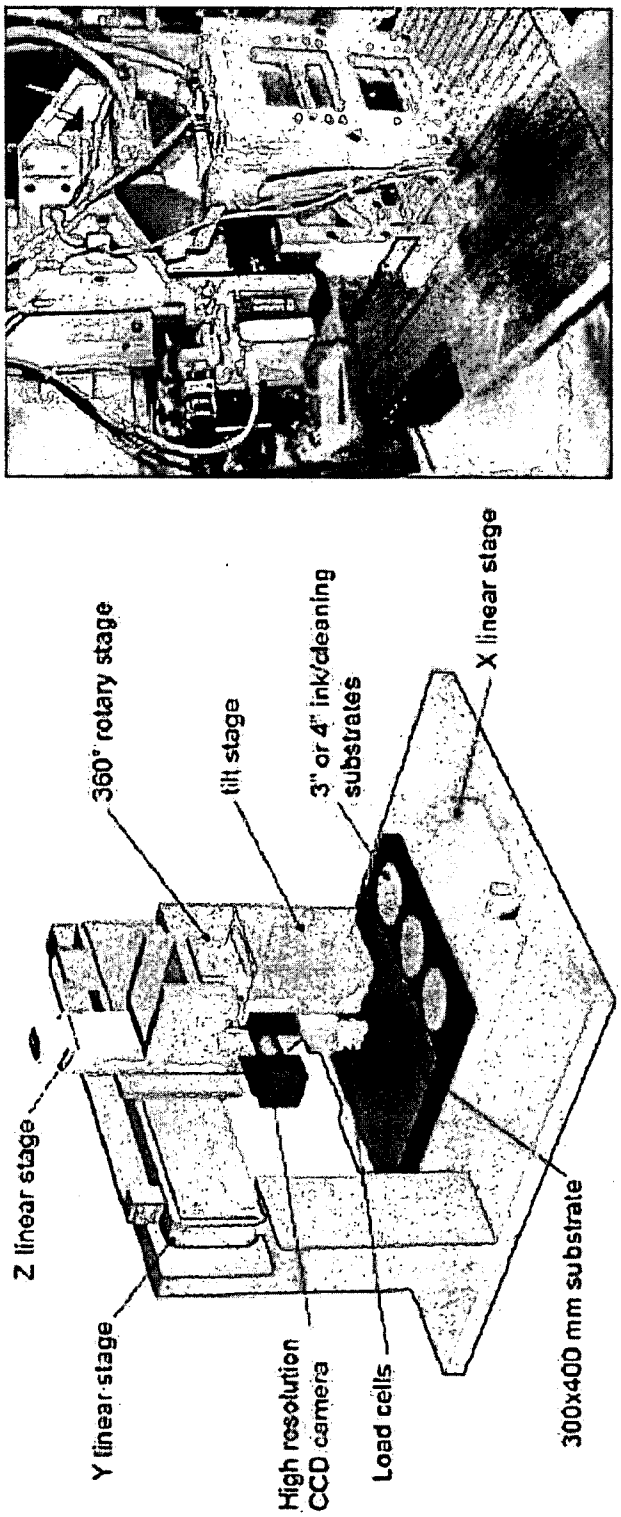
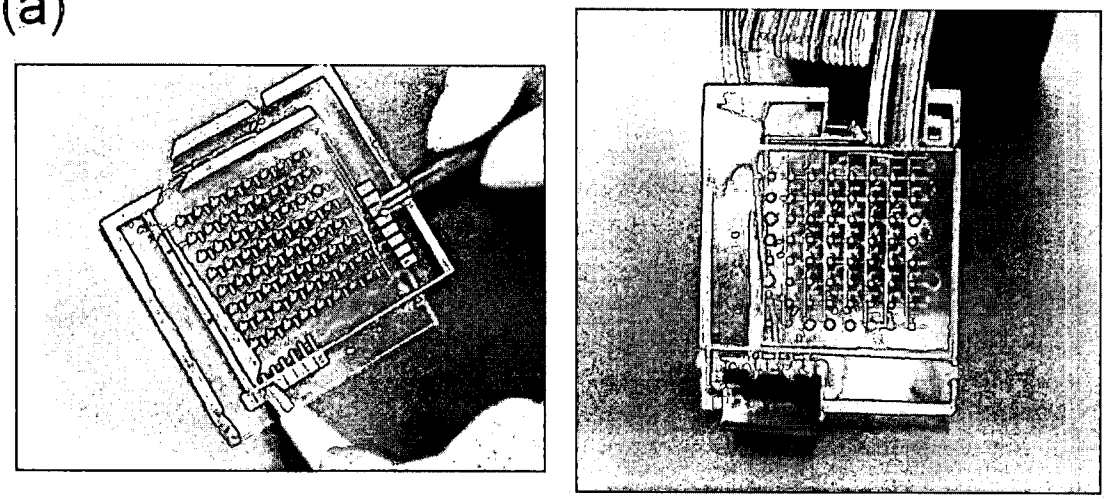

360° rotary stage
tilt stage
3" or 4" ink/cleaning substrates
X linear stage
Z linear stage
Y linear stage
High resolution CCD camera
Load cells
300x400 mm substrate

Fig. 36

(a)



(b)

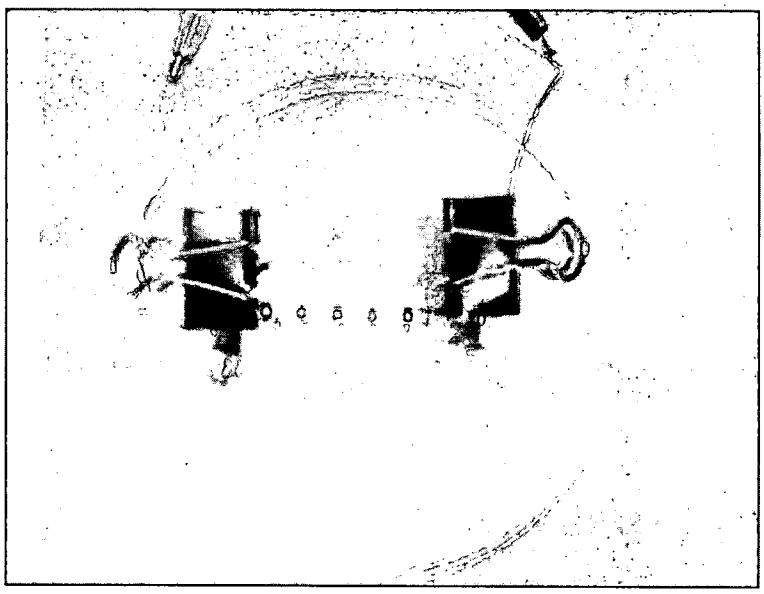


Fig. 37

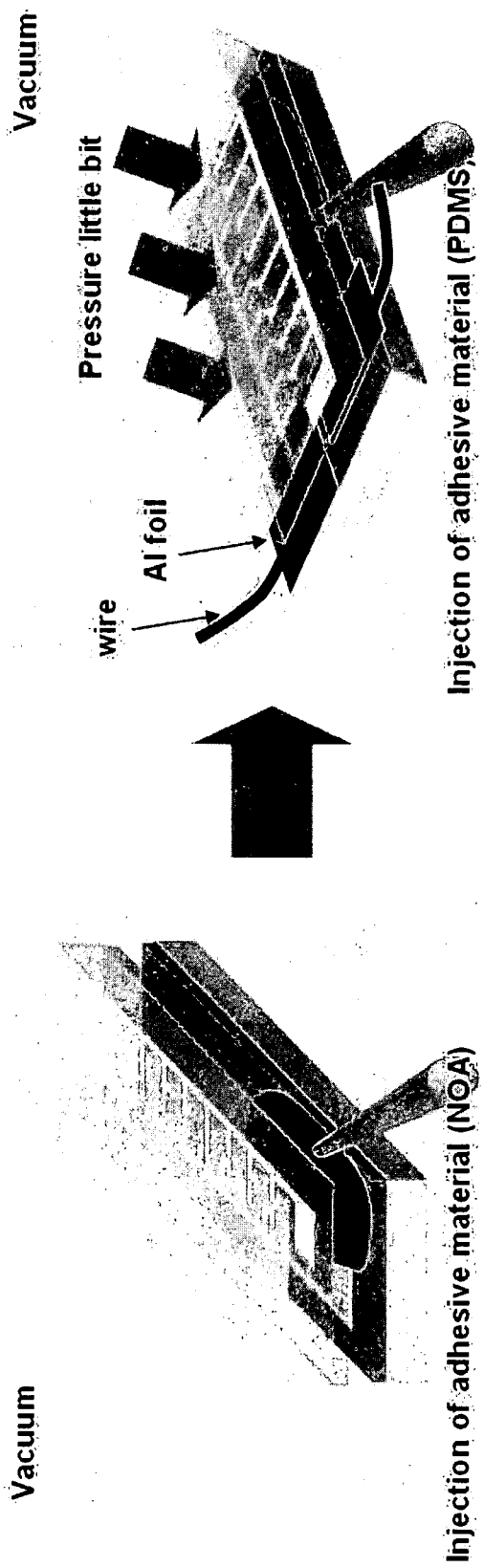

Vacuum
Pressure little bit
Al foil
wire
Injection of adhesive material (PDMS)
Vacuum
Injection of adhesive material (NOA)

Fig. 38

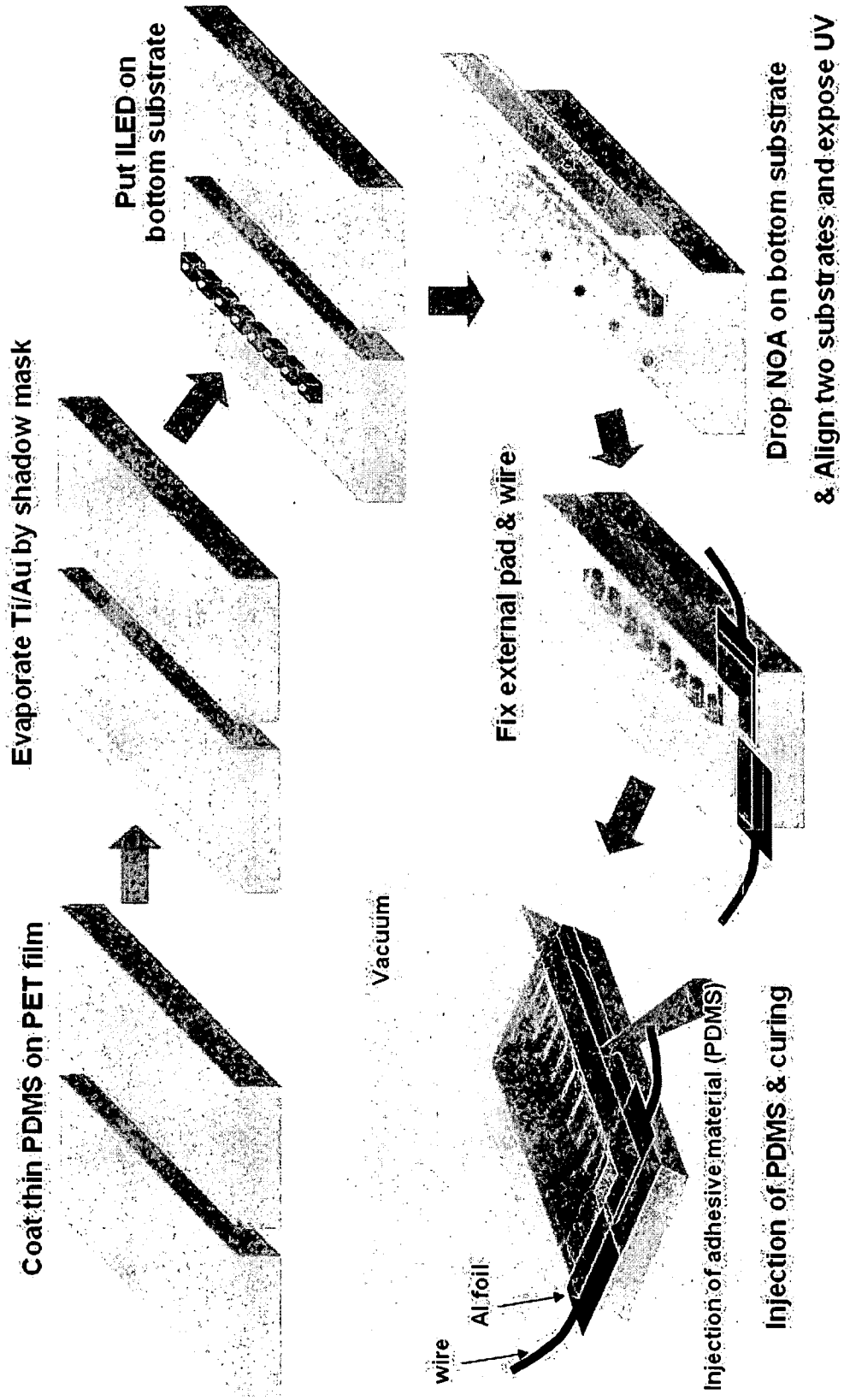

Coat thin PDMS on PET film
Evaporate Ti/Au by shadow mask
Put ILED on bottom substrate
Drop NOA on bottom substrate
& Align two substrates and expose UV
Fix external pad & wire
Vacuum
wire
Al foil
Injection of adhesive material (PDMS)
Injection of PDMS & curing

Fig. 39

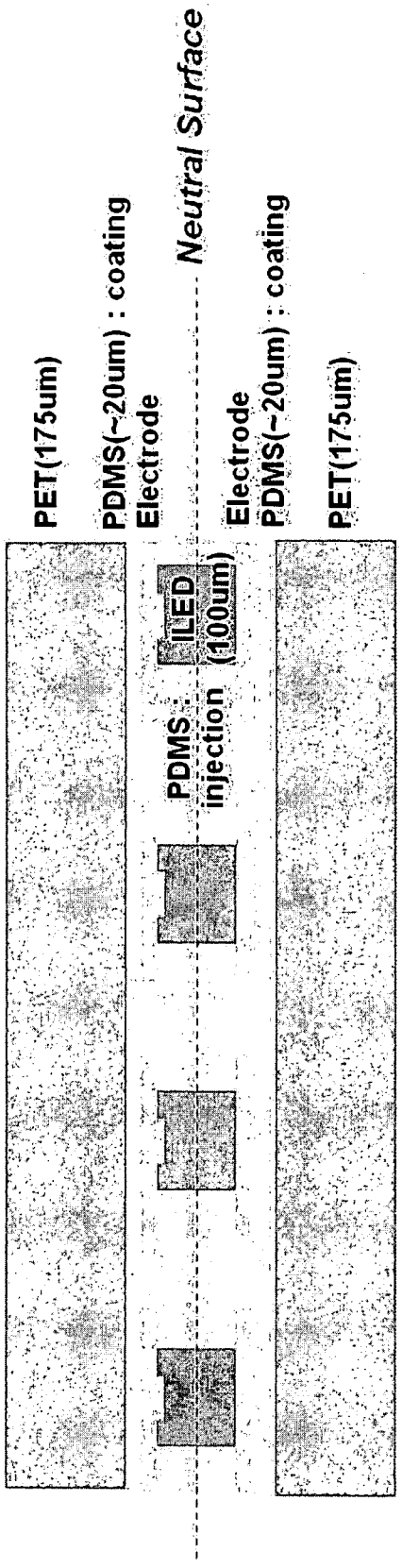

PET(175um)
PDMS(~20um) : coating
Electrode
Neutral Surface
Electrode
PDMS(~20um) : coating
PET(175um)
ILED
(100um)
PDMS :
injection

Fig. 40

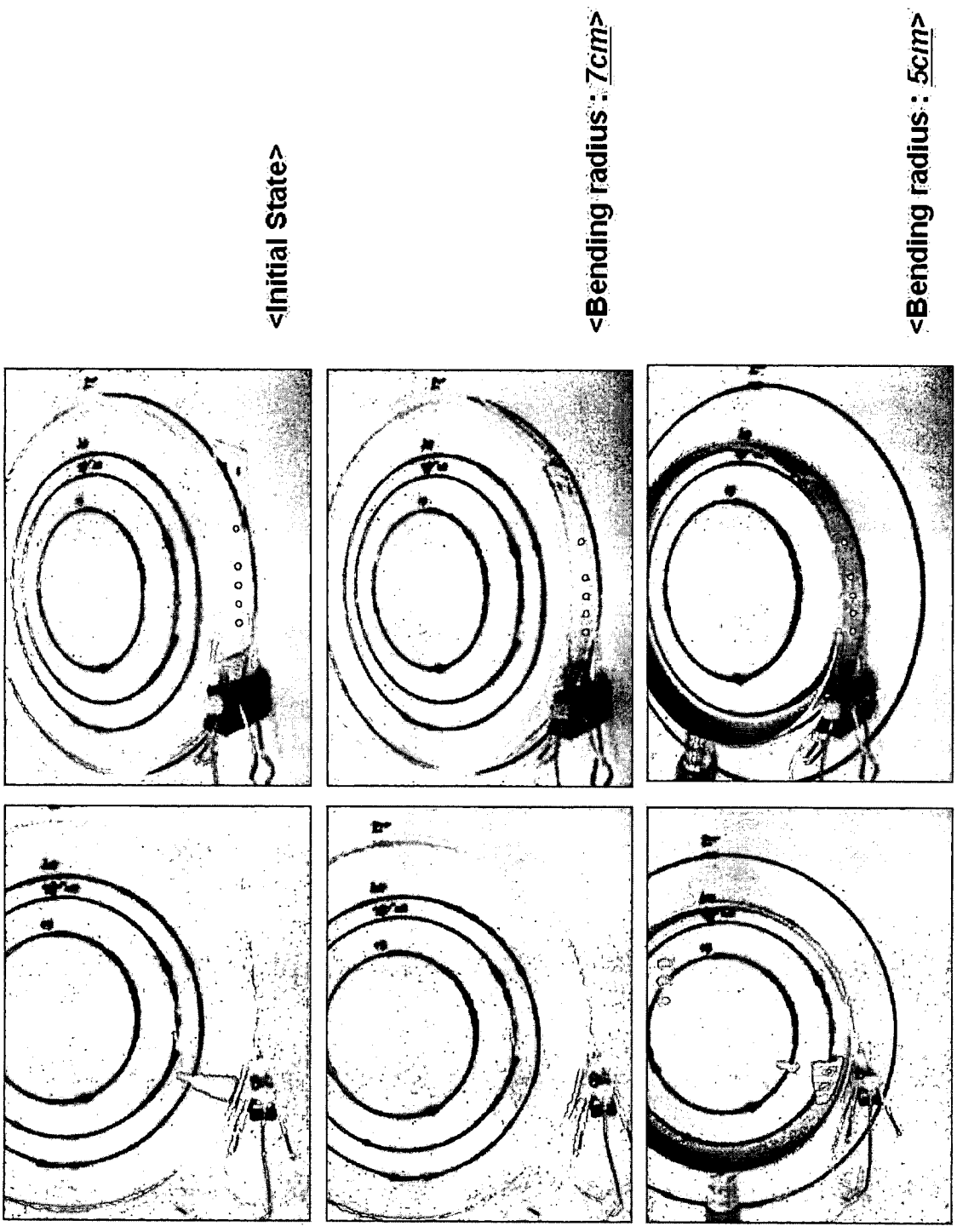


Fig. 41

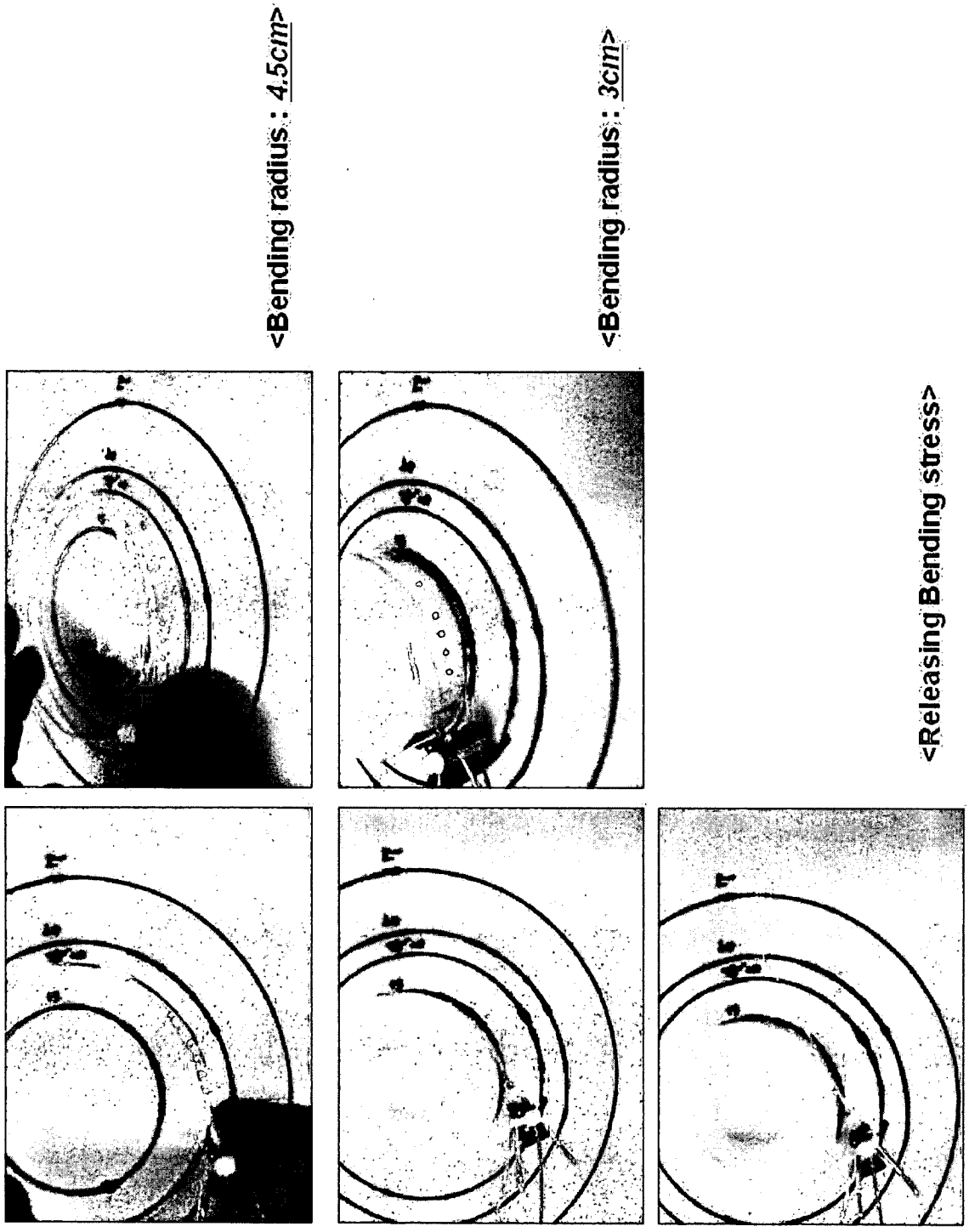

<Bending radius : 4.5cm>
<Bending radius : 3cm>
<Releasing Bending stress>

Fig. 41 (cont'd)

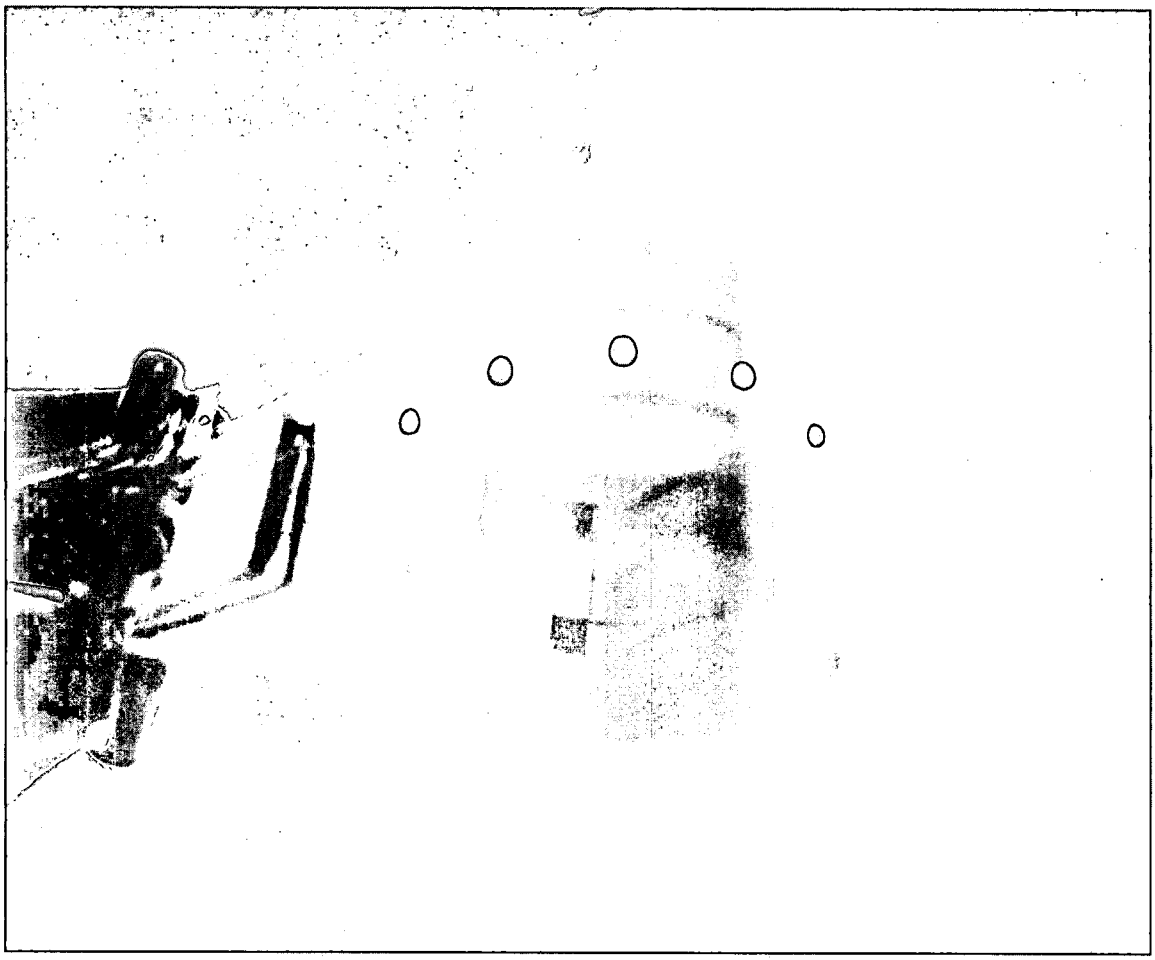


Fig. 42

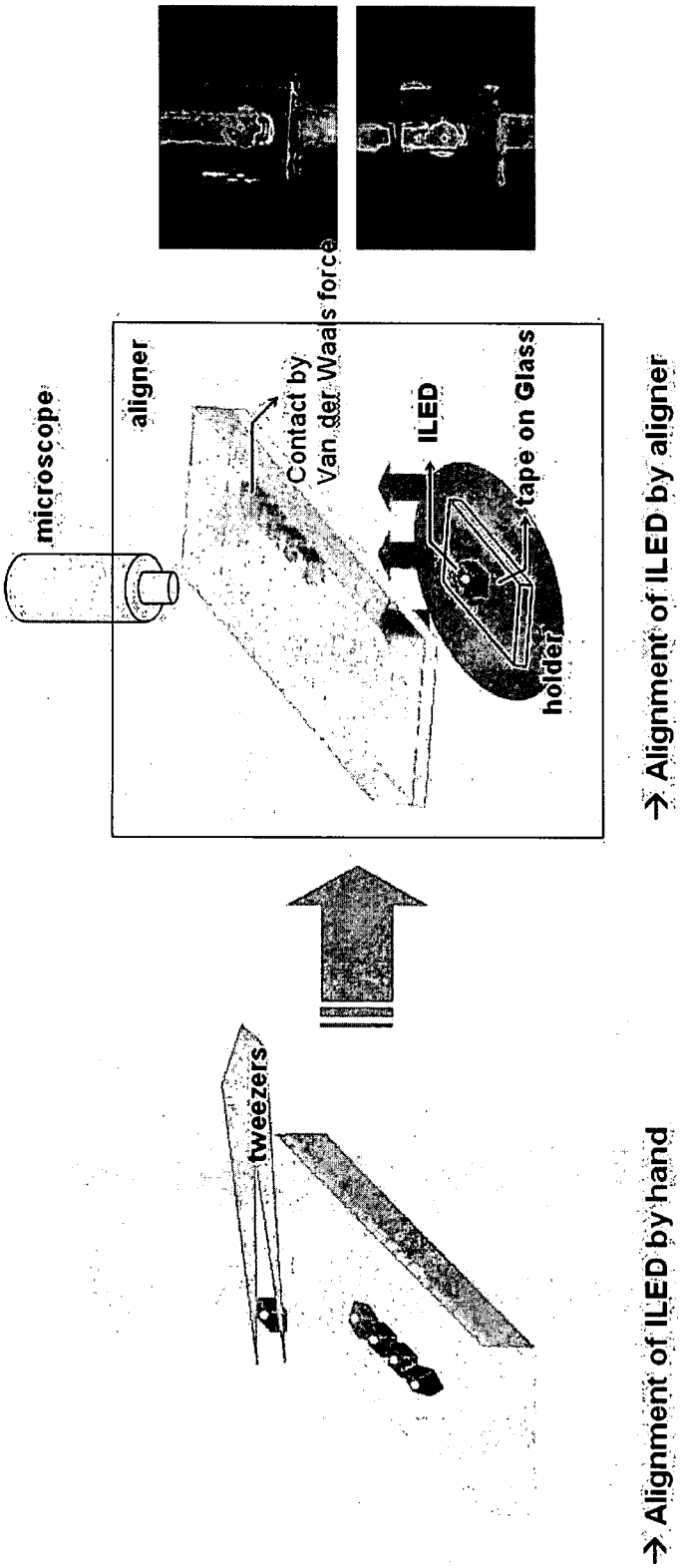

microscope
aligner
Contact by Van der Waals force
ILED
tape on Glass
holder
→ Alignment of ILED by aligner
tweezers
→ Alignment of ILED by hand

Fig. 43

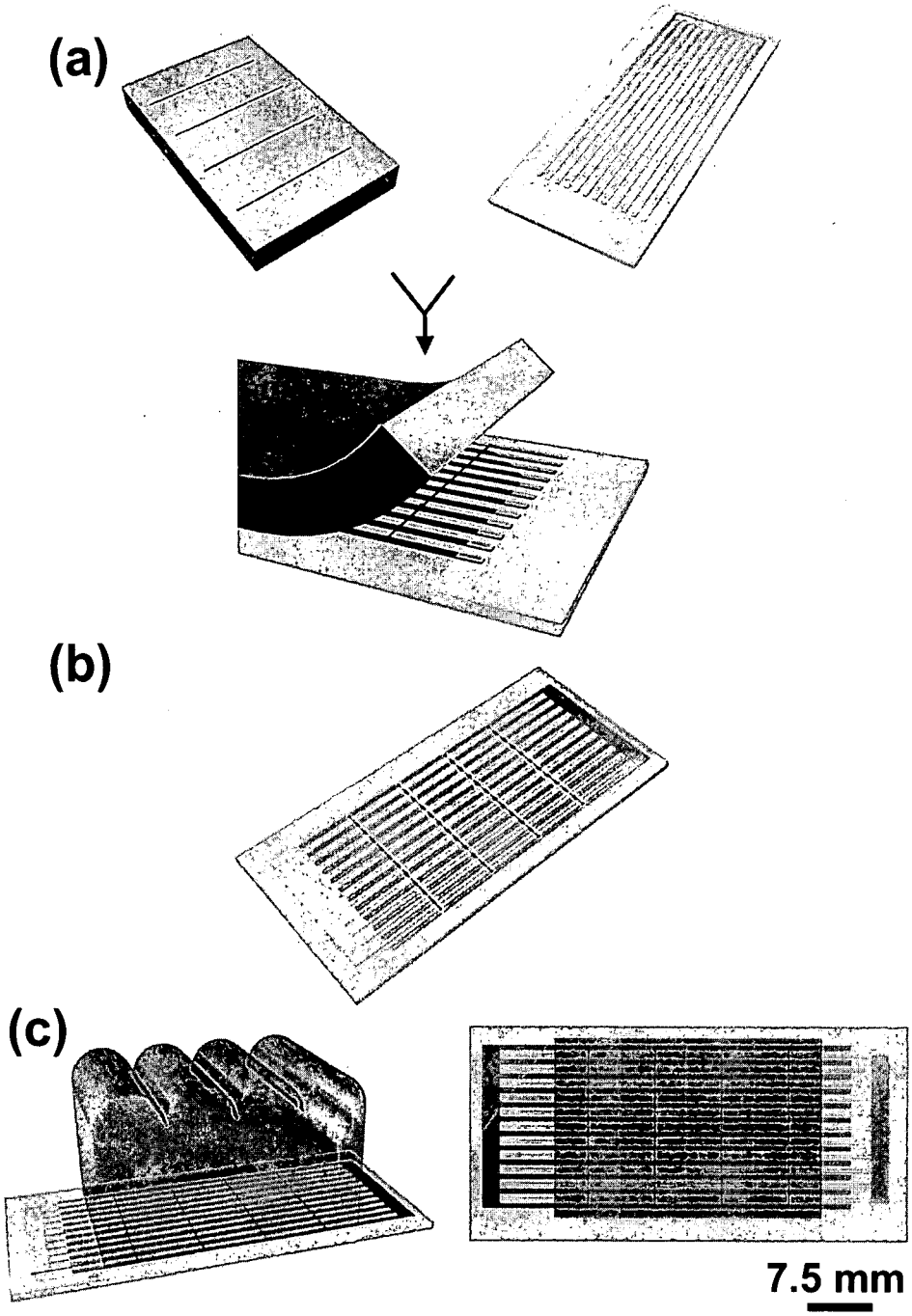
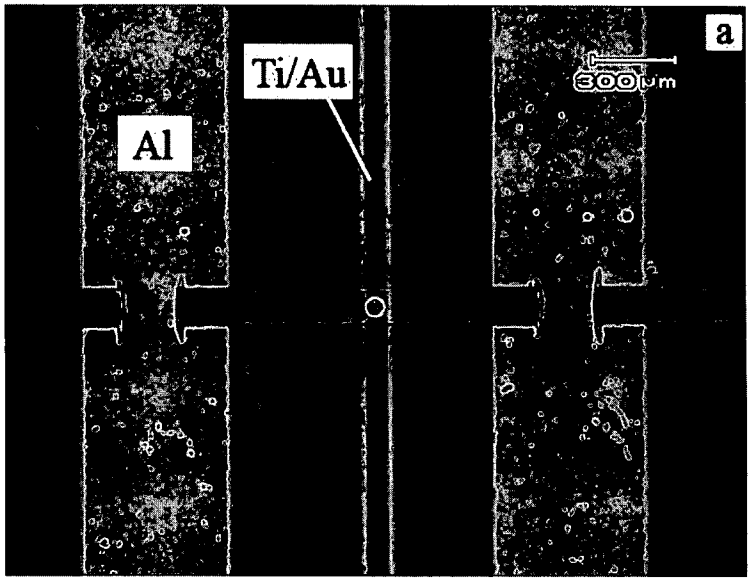
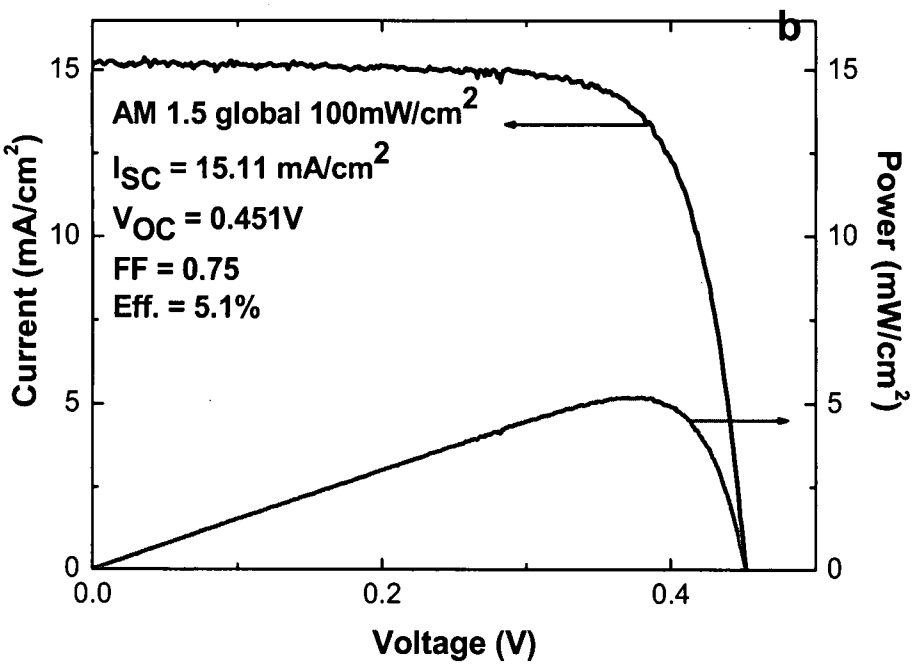


Fig. 44





I-V for 1 cell (not fully integrated device)

Fig. 45

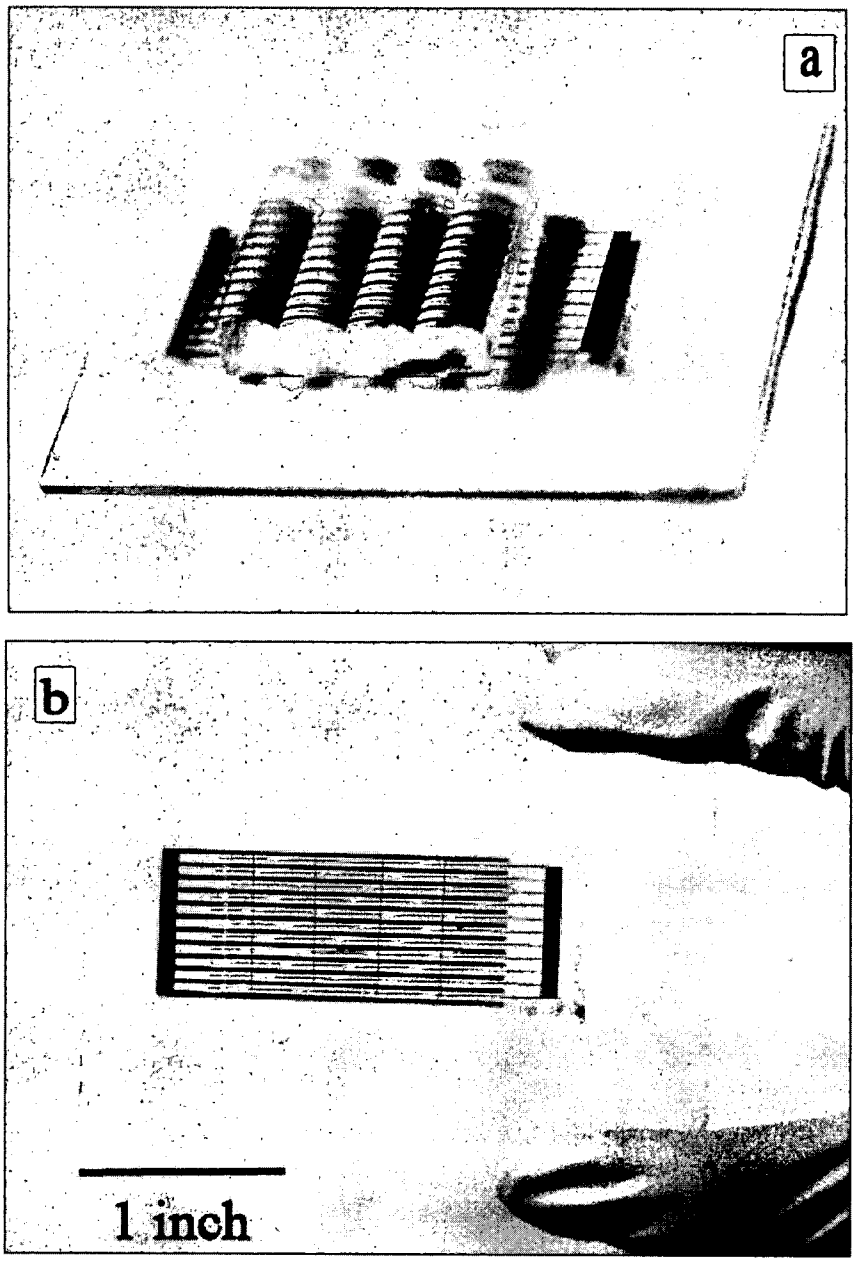
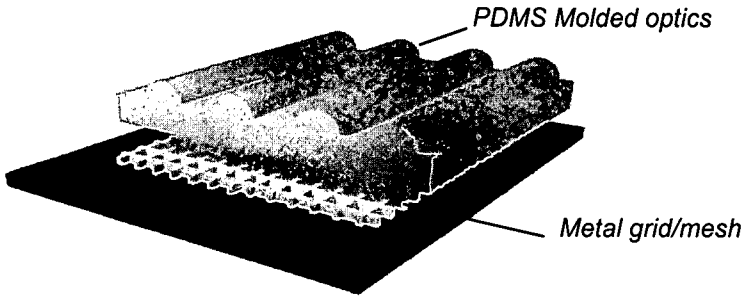
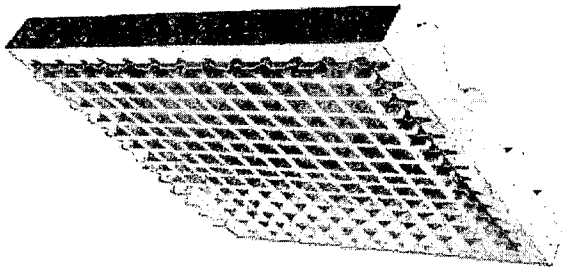


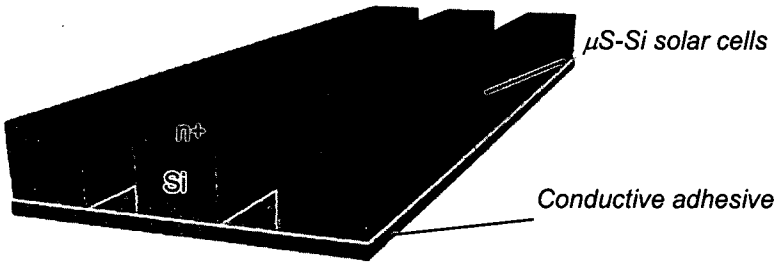
Fig. 46



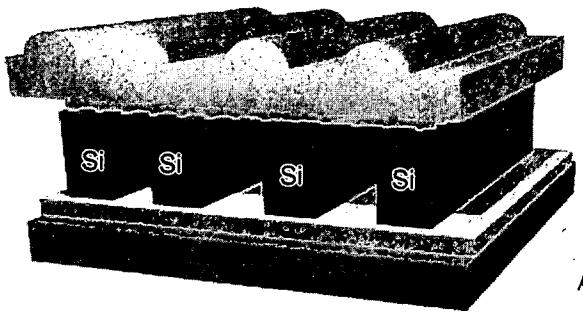
i. Retrieve metal grid or mesh from substrate with PDMS molded lens



ii. Transfer print metal grid or mesh with PDMS molded lens



iii. μS-Si solar cells with integrated contacts and optics



μS-Si solar cells final device

Fig. 47

Process for making printable μS-Si solar cells from bulk wafers

- Emitter formation: Coat phosphorus spin on dopant (SOD) onto a Silicon <111> wafer.
- Silicon Ribbon formation (i.e. cell) : Pattern length and width of the cells via photolithography
- Define the cell thickness (can vary from 5 μm- 60 μm) by deep reactive ion etching or wet anisotropic etching
- Passivate the sidewalls of the ribbons with SiN and then KOH undercut to release the ribbons from the mother substrate
- Retrieve silicon solar cells (i.e. ribbons) with PDMS Deposit back metallization
- Print onto plastic or any substrate via a conductive adhesive (e.g. silver paint)
- Cast insulating/planarization layer
- Laminate PDMS concentrating optics and metal contact grid onto top of silicon ribbons

Fig. 48

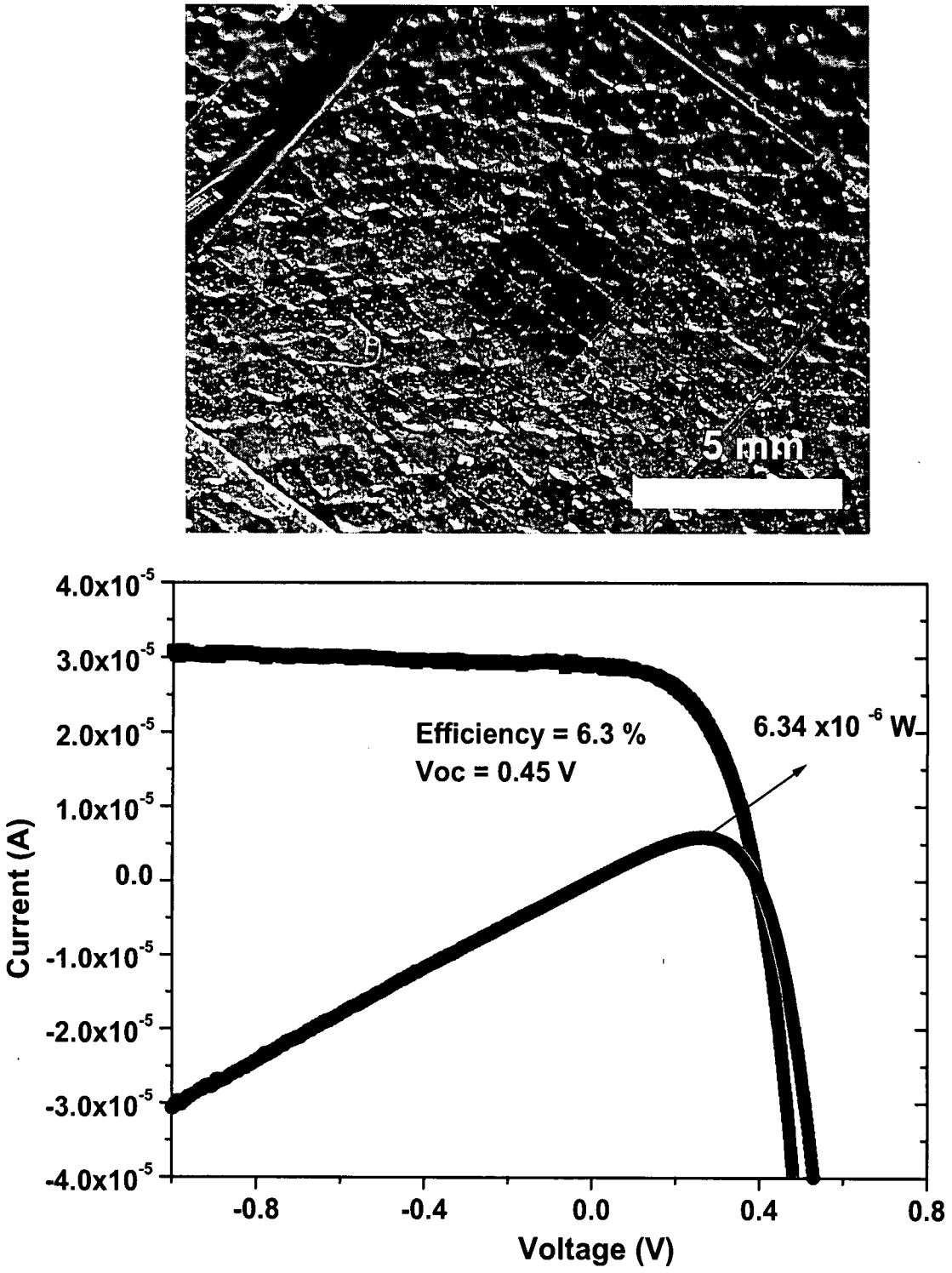

5 mm
4.0x10-5
3.0x10-5
2.0x10-5
1.0x10-5
0.0
-1.0x10-5
-2.0x10-5
-3.0x10-5
-4.0x10-5
Current (A)
Efficiency = 6.3 %
Voc = 0.45 V
6.34 x10 -6 W
-0.8
-0.4
0.0
0.4
0.8
Voltage (V)

Fig. 49

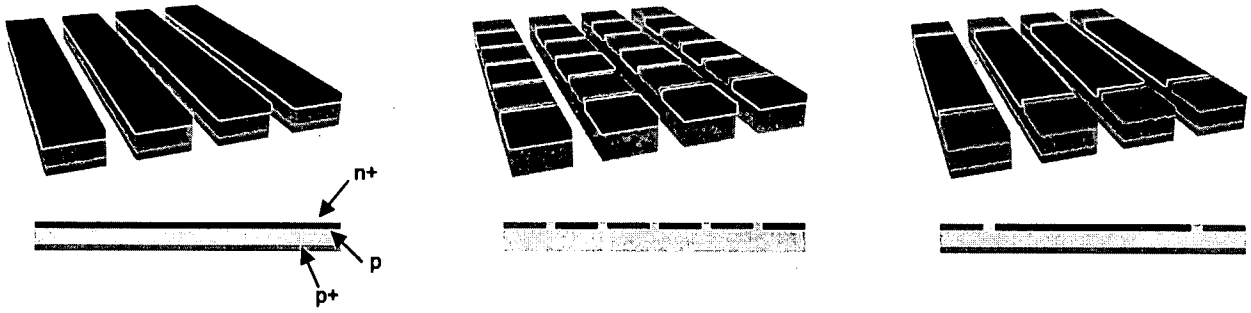


Fig. 50

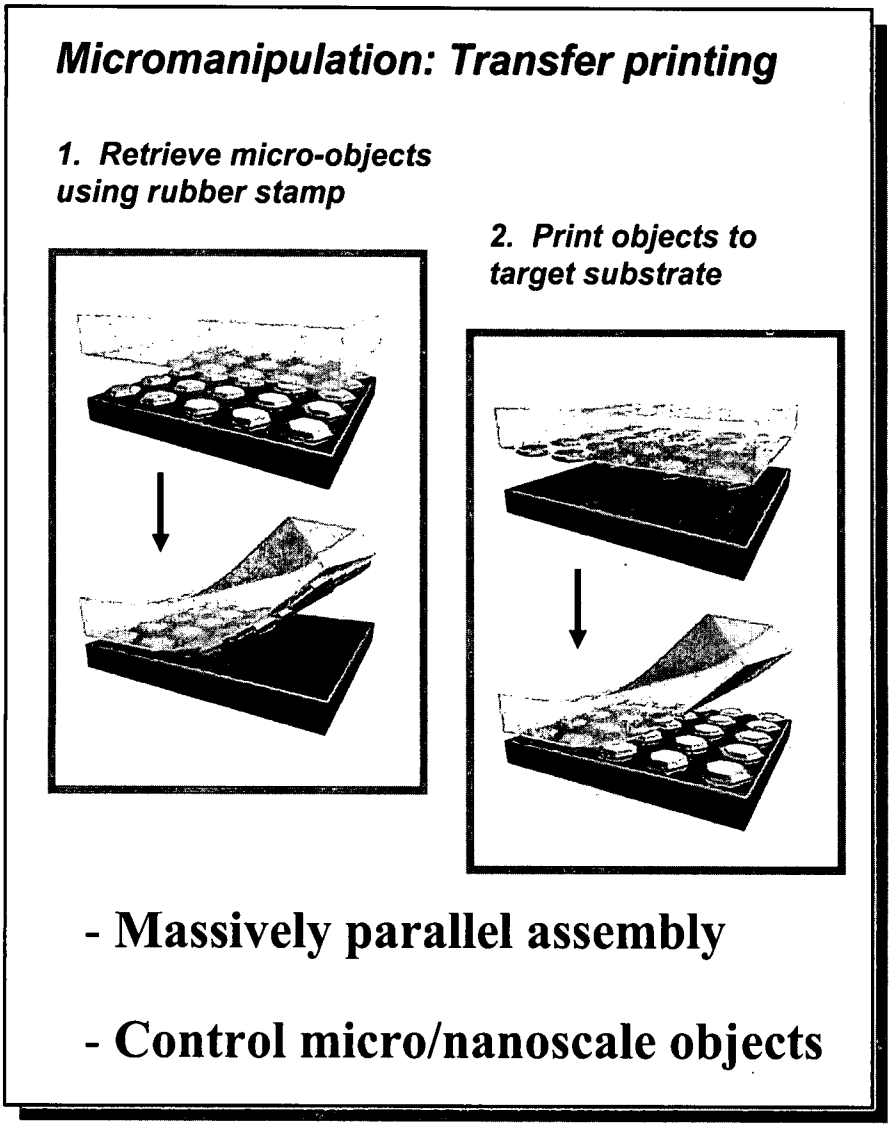
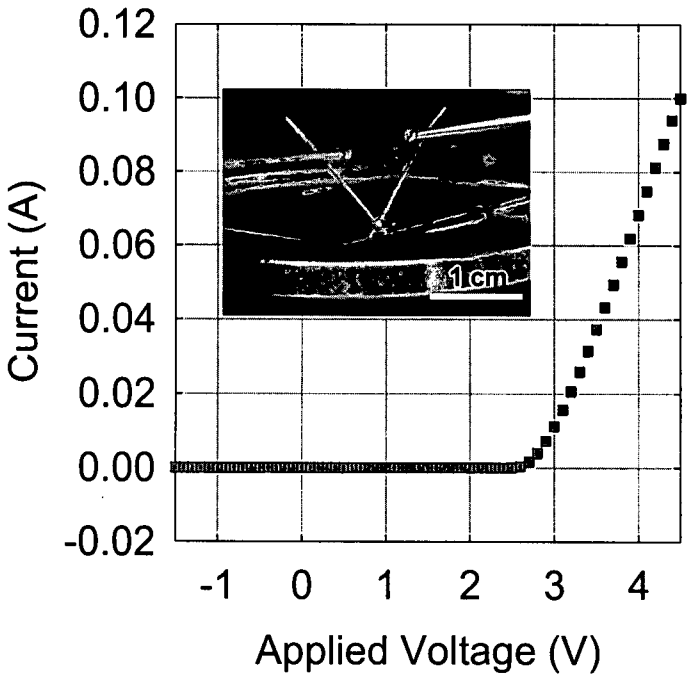

Micromanipulation: Transfer printing
1. Retrieve micro-objects using rubber stamp
2. Print objects to target substrate
- Massively parallel assembly
- Control micro/nanoscale objects

Fig. 51

Inorganic LED operation



- High efficiency & brightness

- Rugged; robust operation

Fig. 52

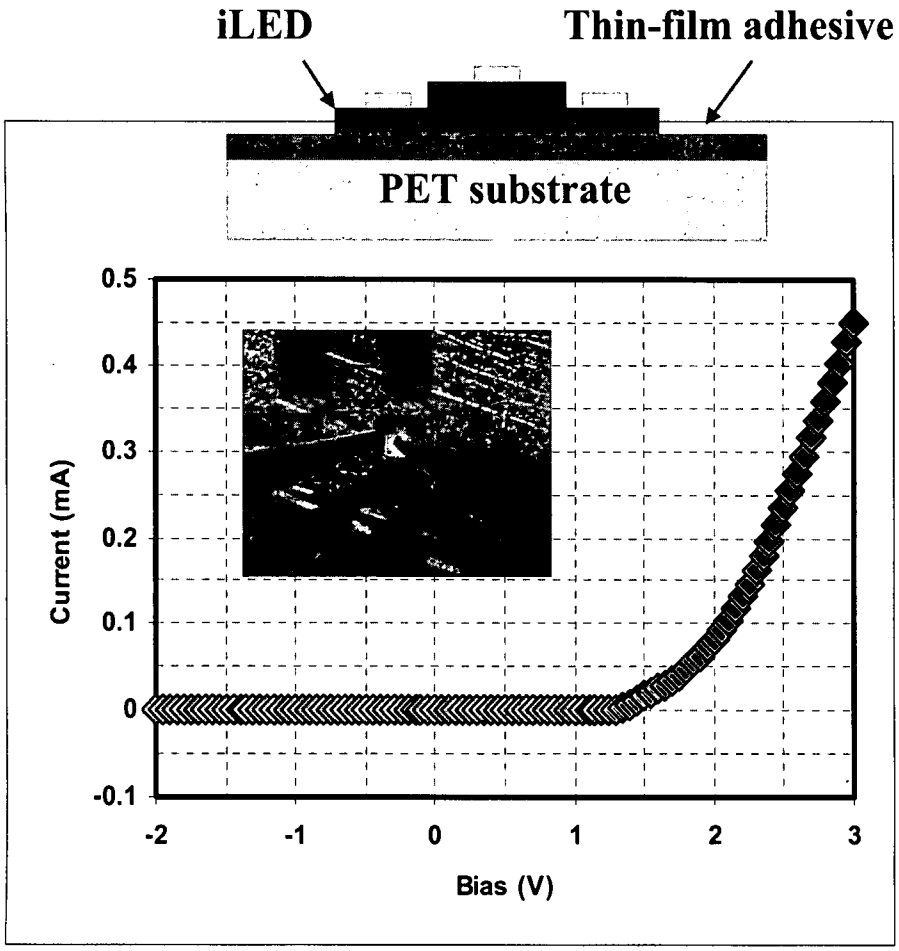


Fig. 53A

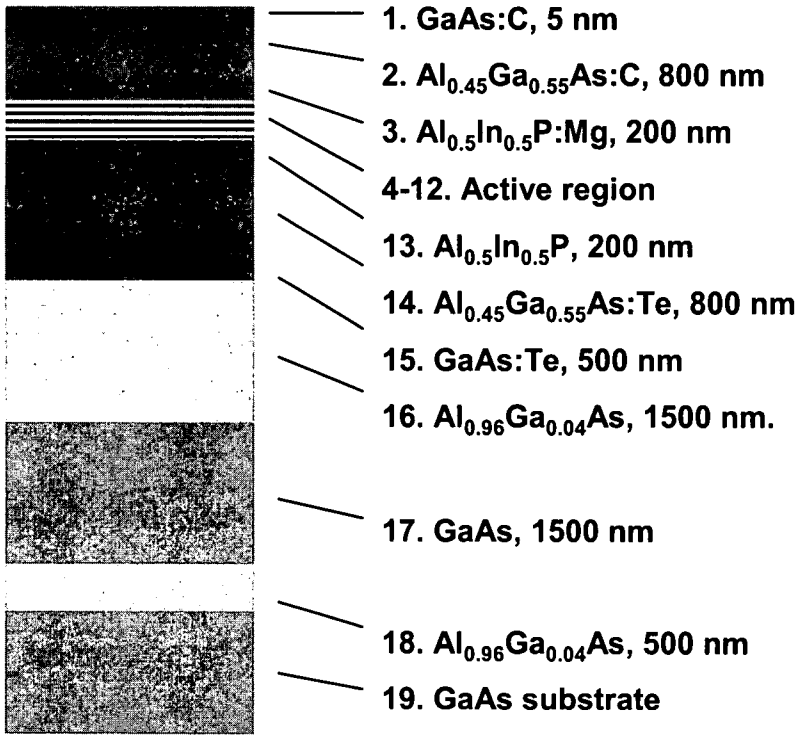


Fig. 53B

Fig. 54A

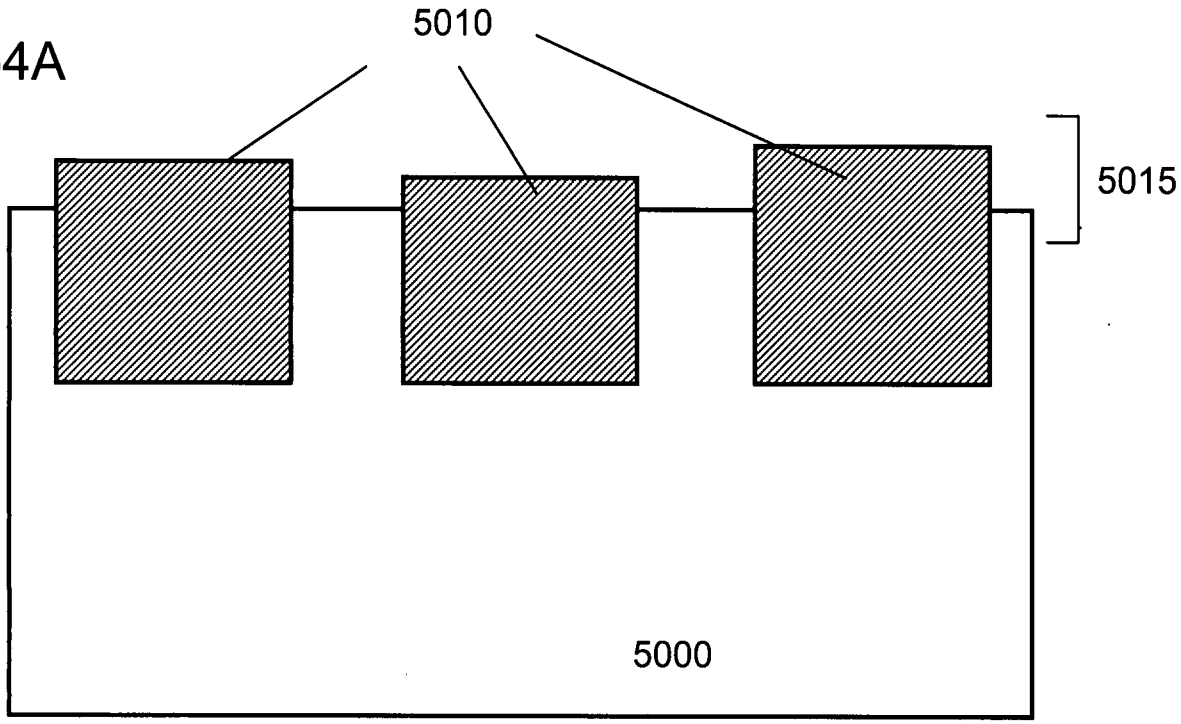
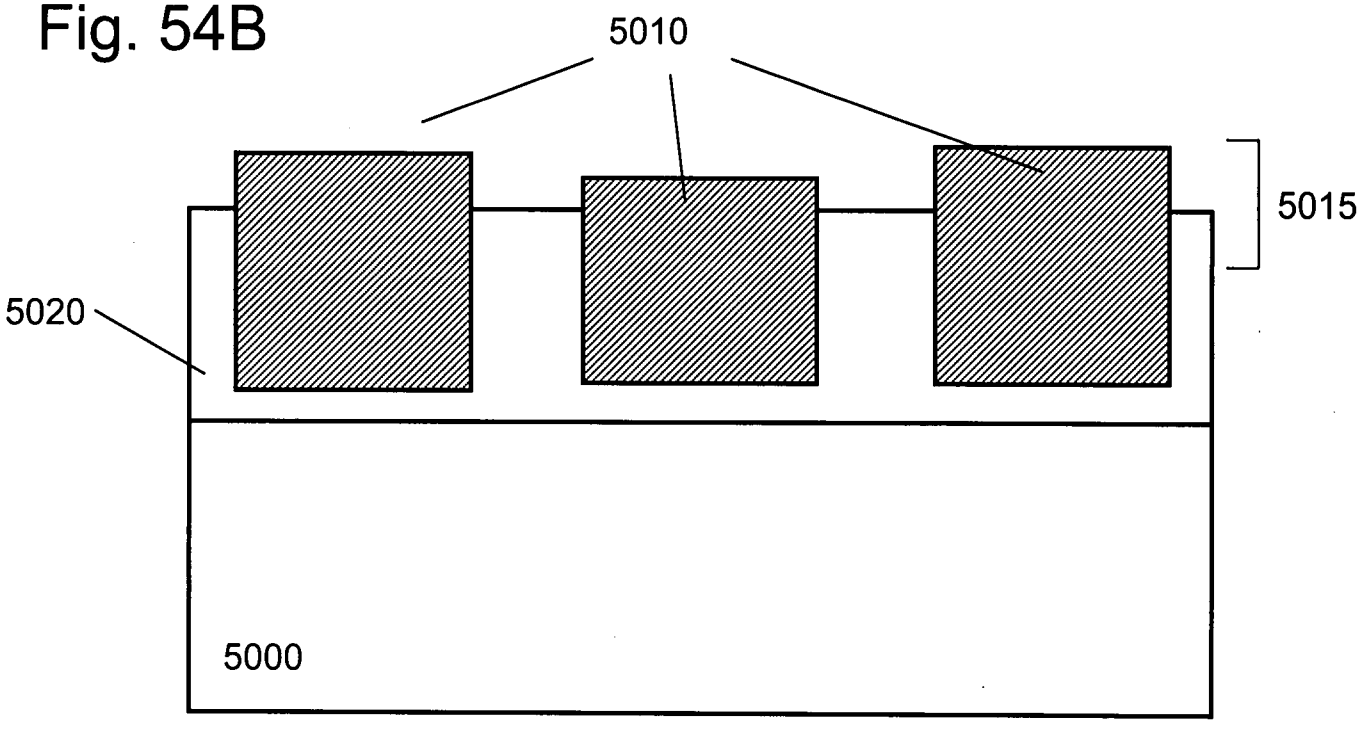


Fig. 54B



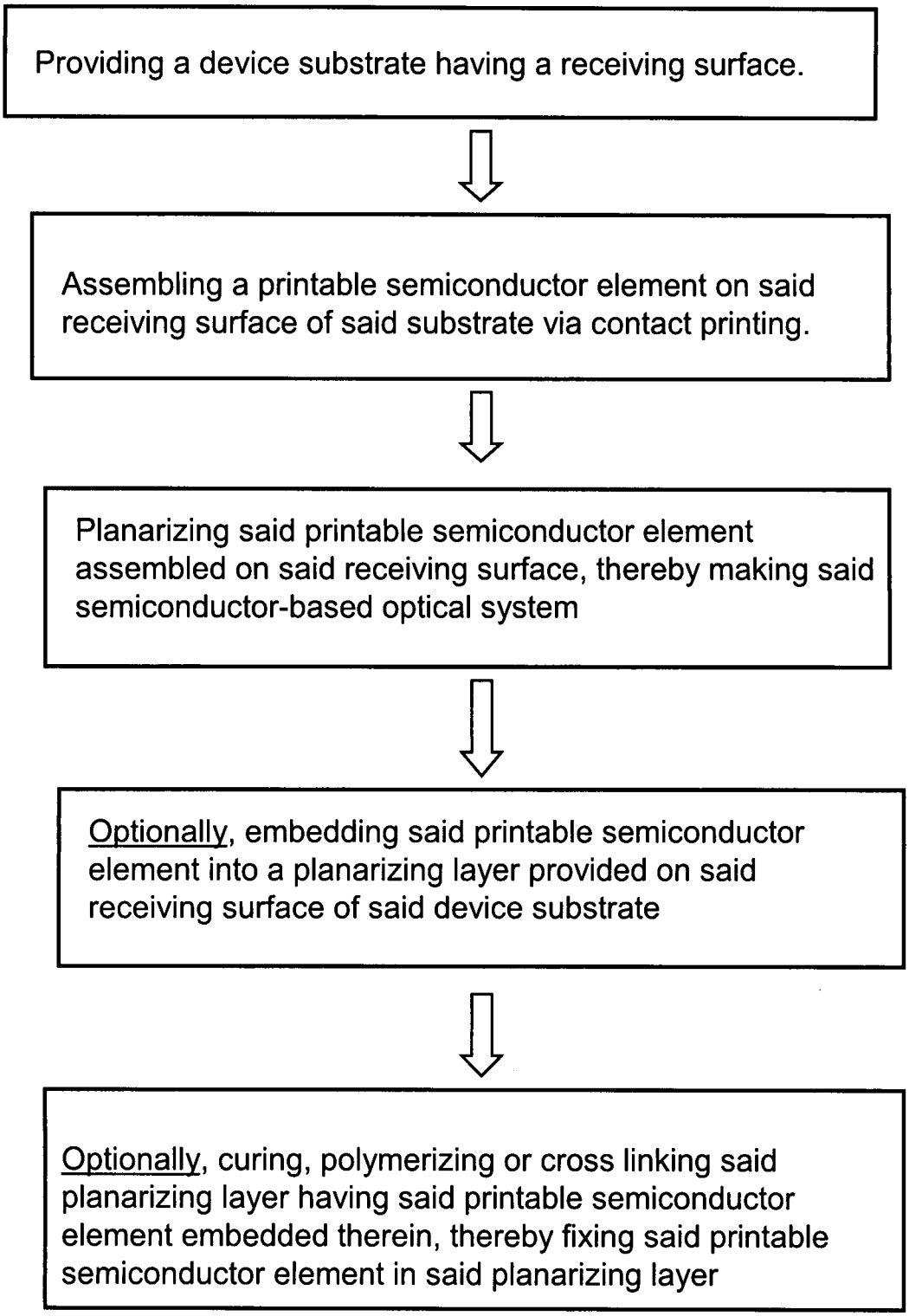

Providing a device substrate having a receiving surface.
Assembling a printable semiconductor element on said receiving surface of said substrate via contact printing.
Planarizing said printable semiconductor element assembled on said receiving surface, thereby making said semiconductor-based optical system
Optionally, embedding said printable semiconductor element into a planarizing layer provided on said receiving surface of said device substrate
Optionally, curing, polymerizing or cross linking said planarizing layer having said printable semiconductor element embedded therein, thereby fixing said printable semiconductor element in said planarizing layer

Fig. 55

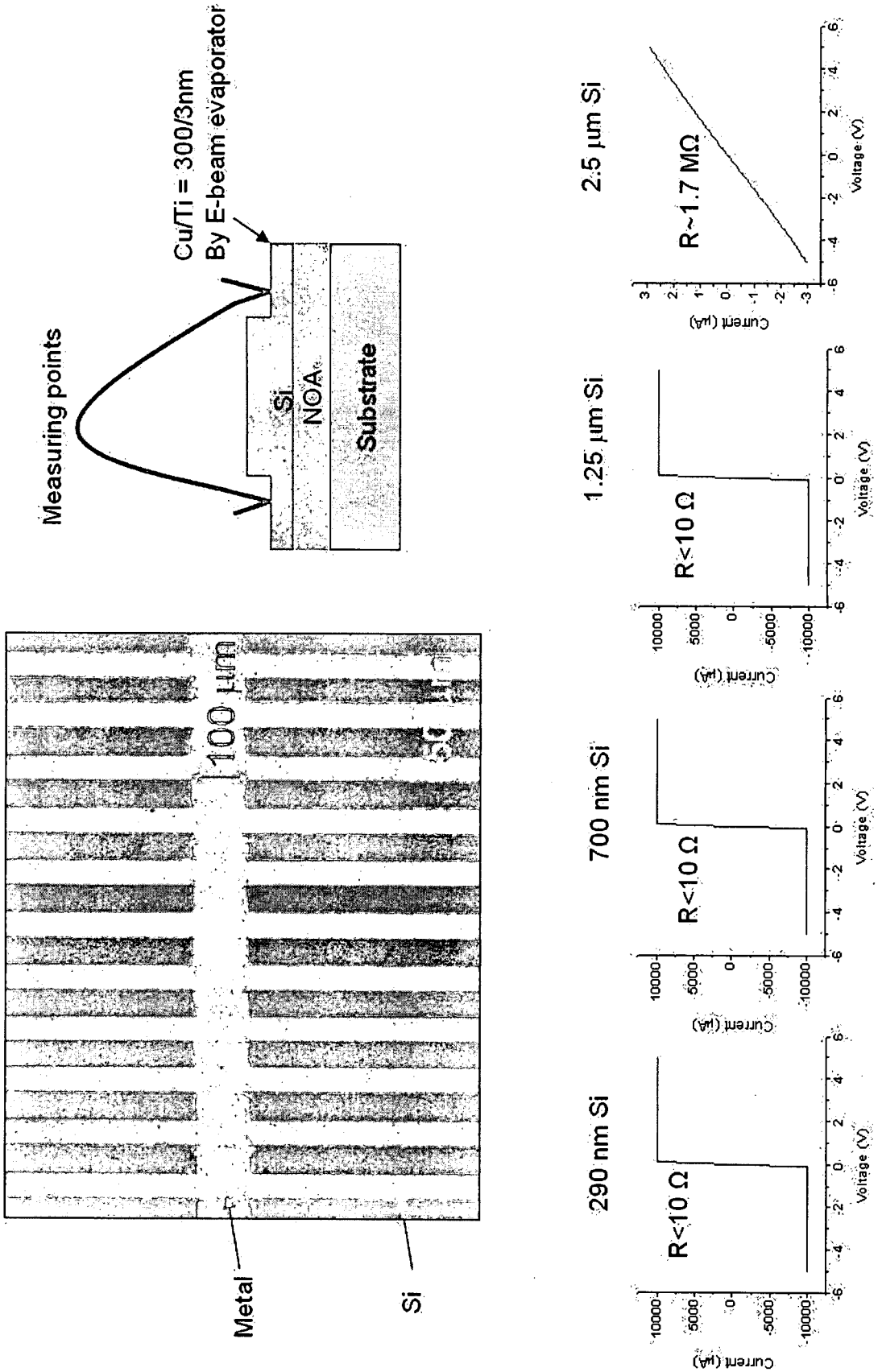

Measuring points
Cu/Ti = 300/3nm
By E-beam evaporator
Si
NOA
Substrate
100 μm
Metal
Si
290 nm Si
700 nm Si
1.25 μm Si
2.5 μm Si
R<10 Ω
R<10 Ω
R<10 Ω
R~1.7 MΩ
Current (μA)
Voltage (V)

Fig. 56

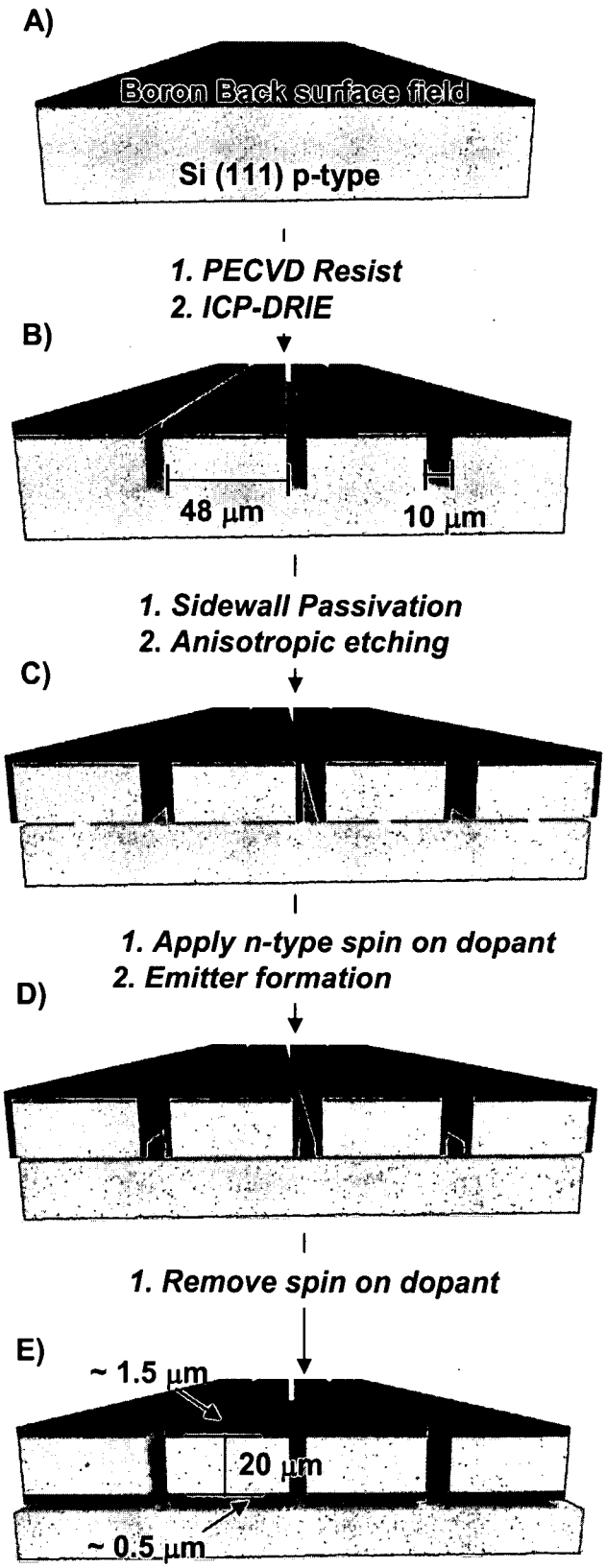

A)
Boron Back surface field
Si (111) p-type
1. PECVD Resist
2. ICP-DRIE
B)
48 μm
10 μm
1. Sidewall Passivation
2. Anisotropic etching
C)
1. Apply n-type spin on dopant
2. Emitter formation
D)
1. Remove spin on dopant
E)
~ 1.5 μm
20 μm
~ 0.5 μm

Fig. 57

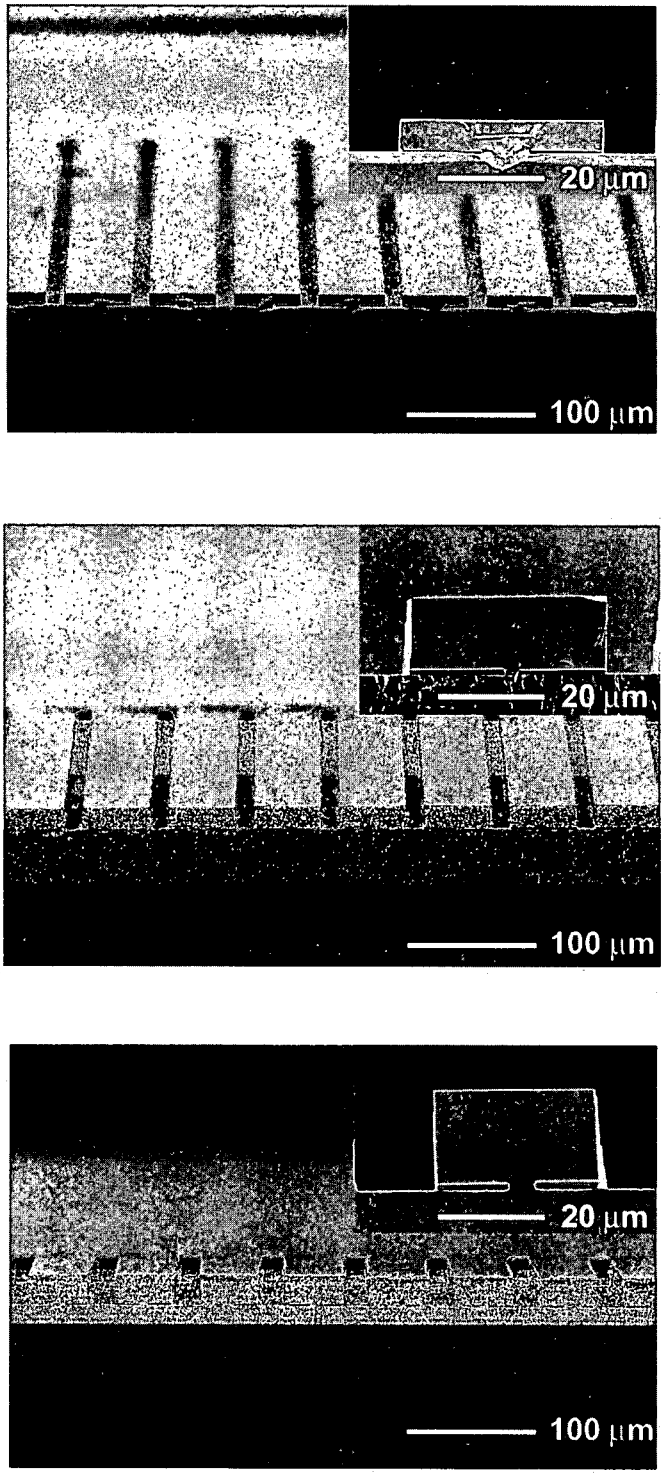


Fig. 58

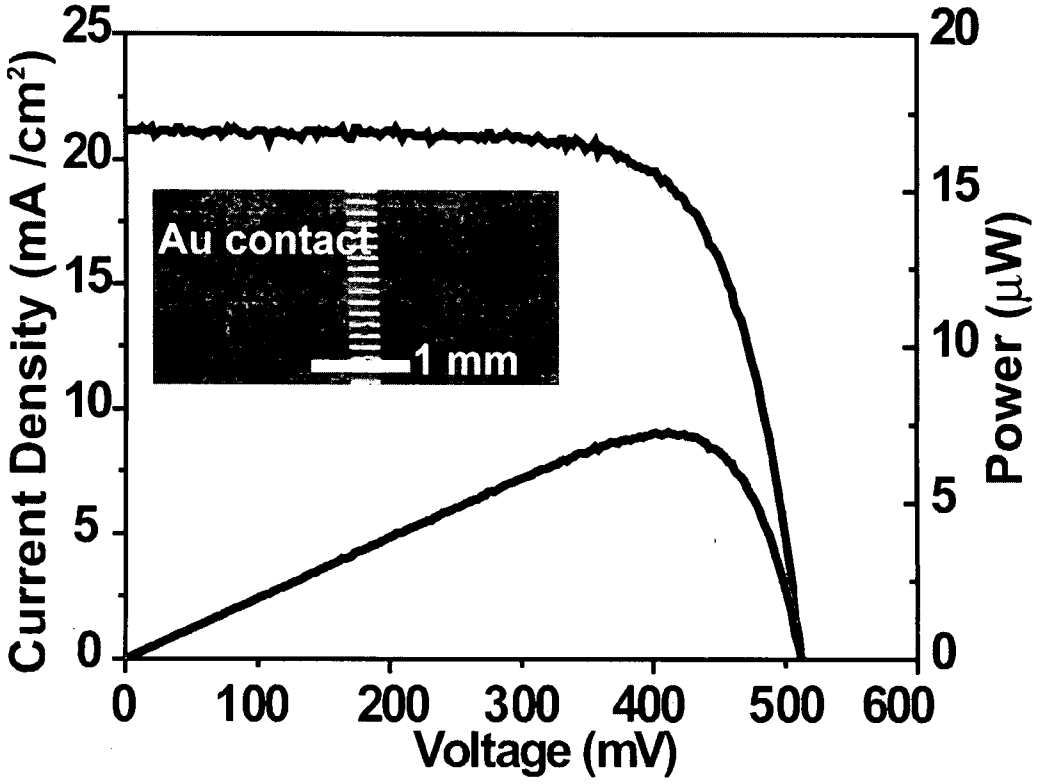

Current Density (mA /cm²)
Power (μW)
Voltage (mV)
Au contact
1 mm
0
5
10
15
20
25
0
100
200
300
400
500
600

Fig. 59

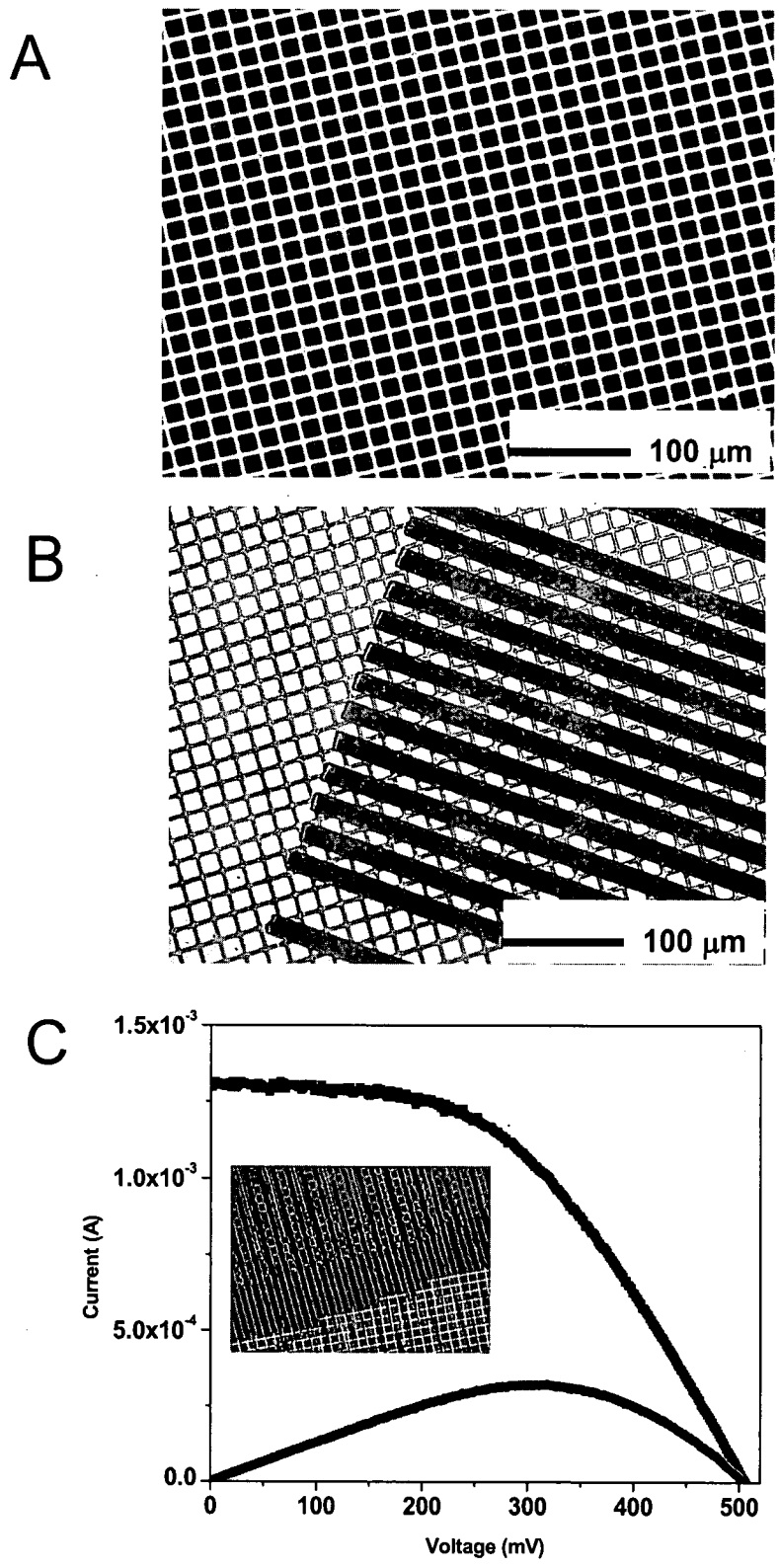

A
100 μm
B
100 μm
C
1.5x10-3
1.0x10-3
5.0x10-4
0.0
Current (A)
0
100
200
300
400
500
Voltage (mV)

Fig. 60

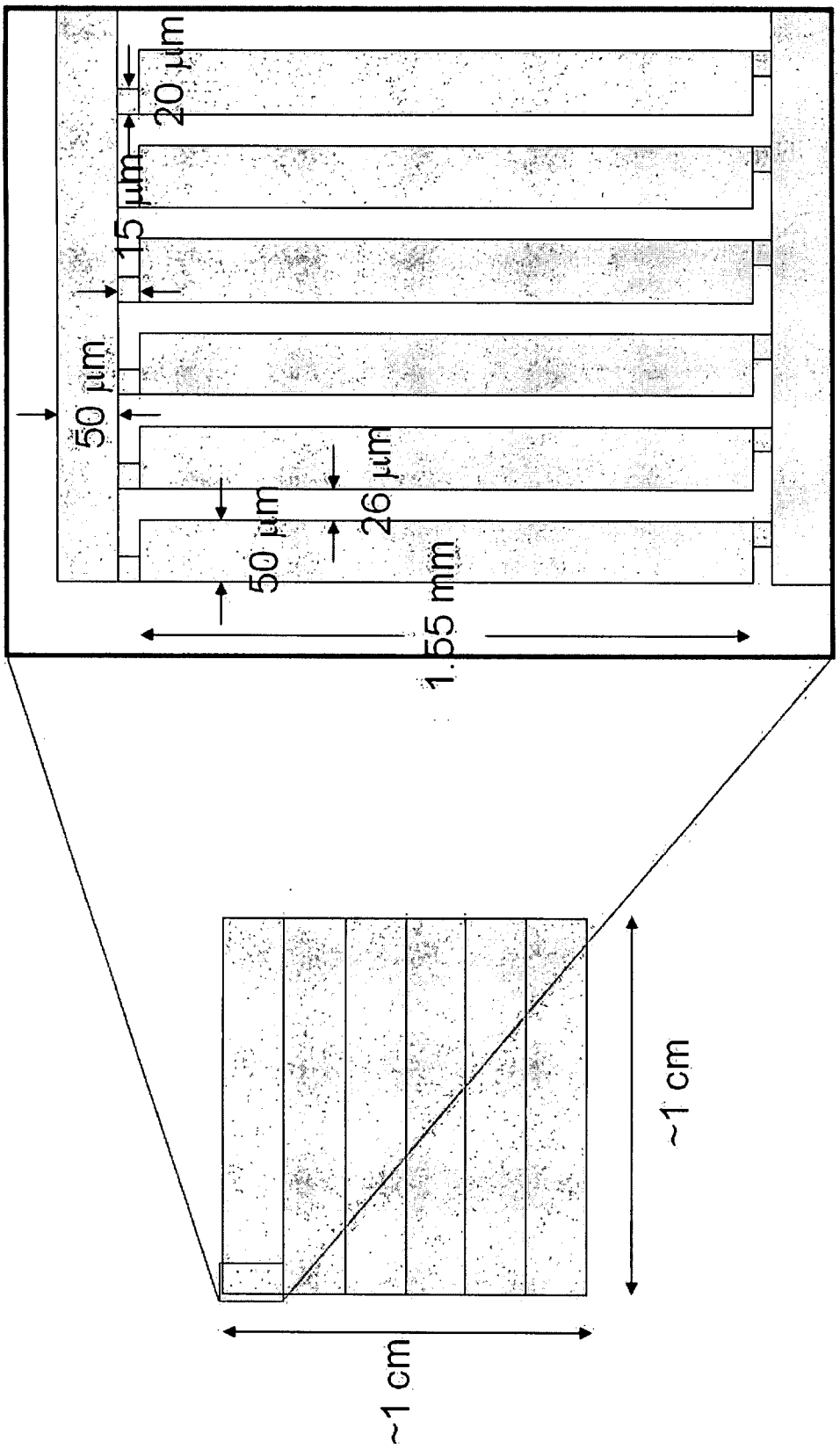


Fig. 61

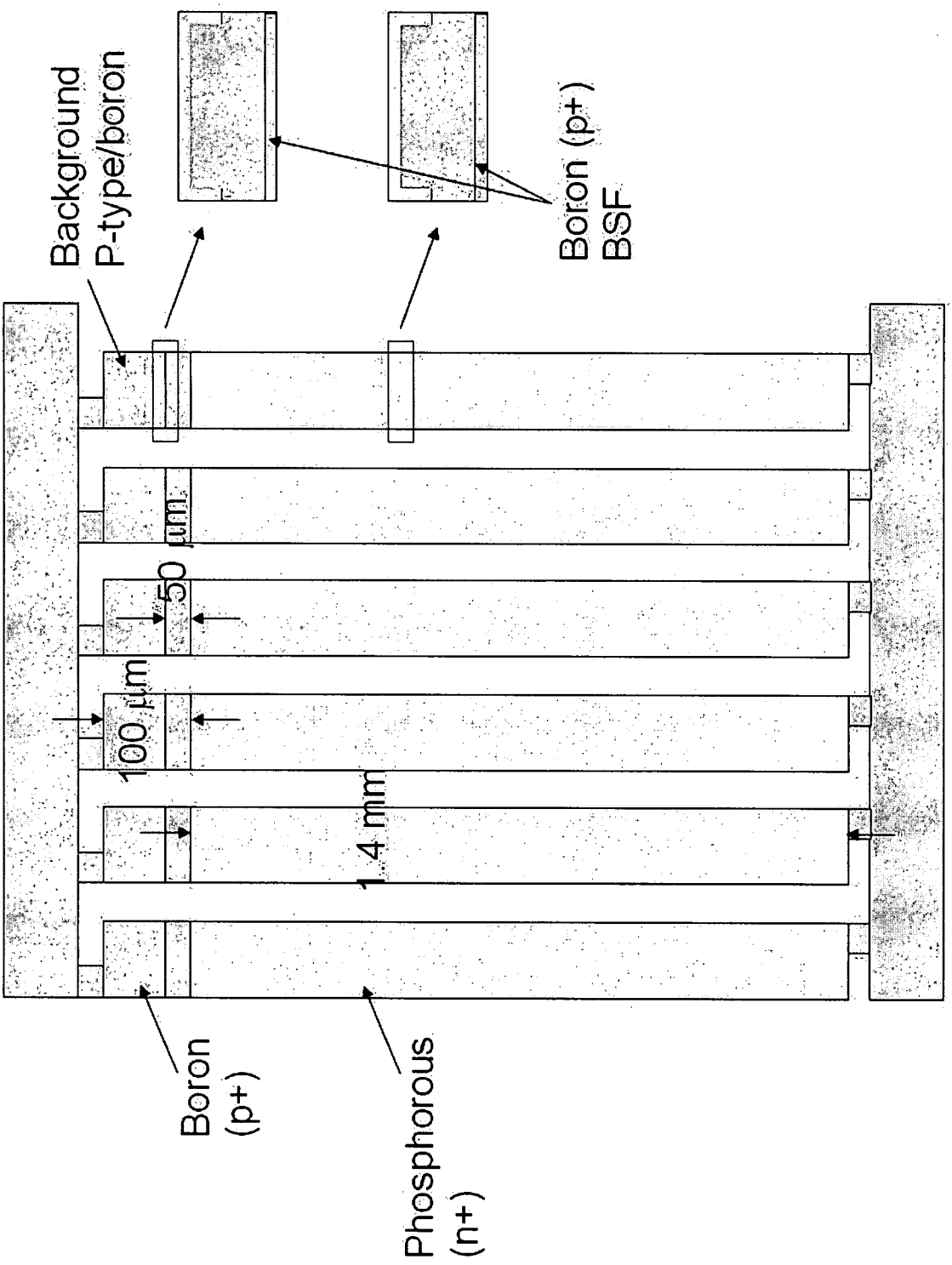

Background
P-type/boron
Boron (p+)
BSF
50 µm
100 µm
1.4 mm
Boron
(p+)
Phosphorous
(n+)

Fig. 62

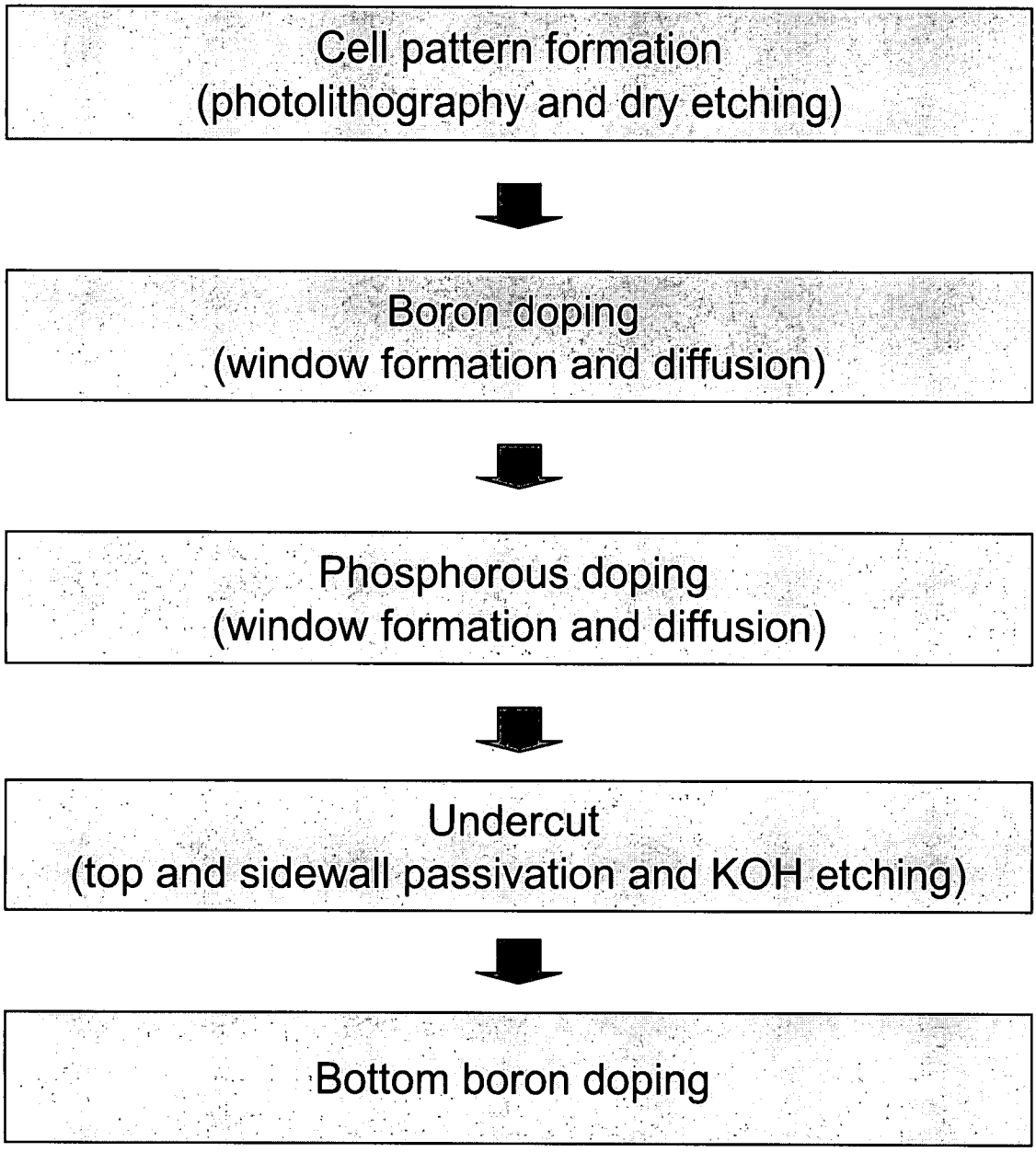

Cell pattern formation
(photolithography and dry etching)
Boron doping
(window formation and diffusion)
Phosphorous doping
(window formation and diffusion)
Undercut
(top and sidewall passivation and KOH etching)
Bottom boron doping

Fig. 63

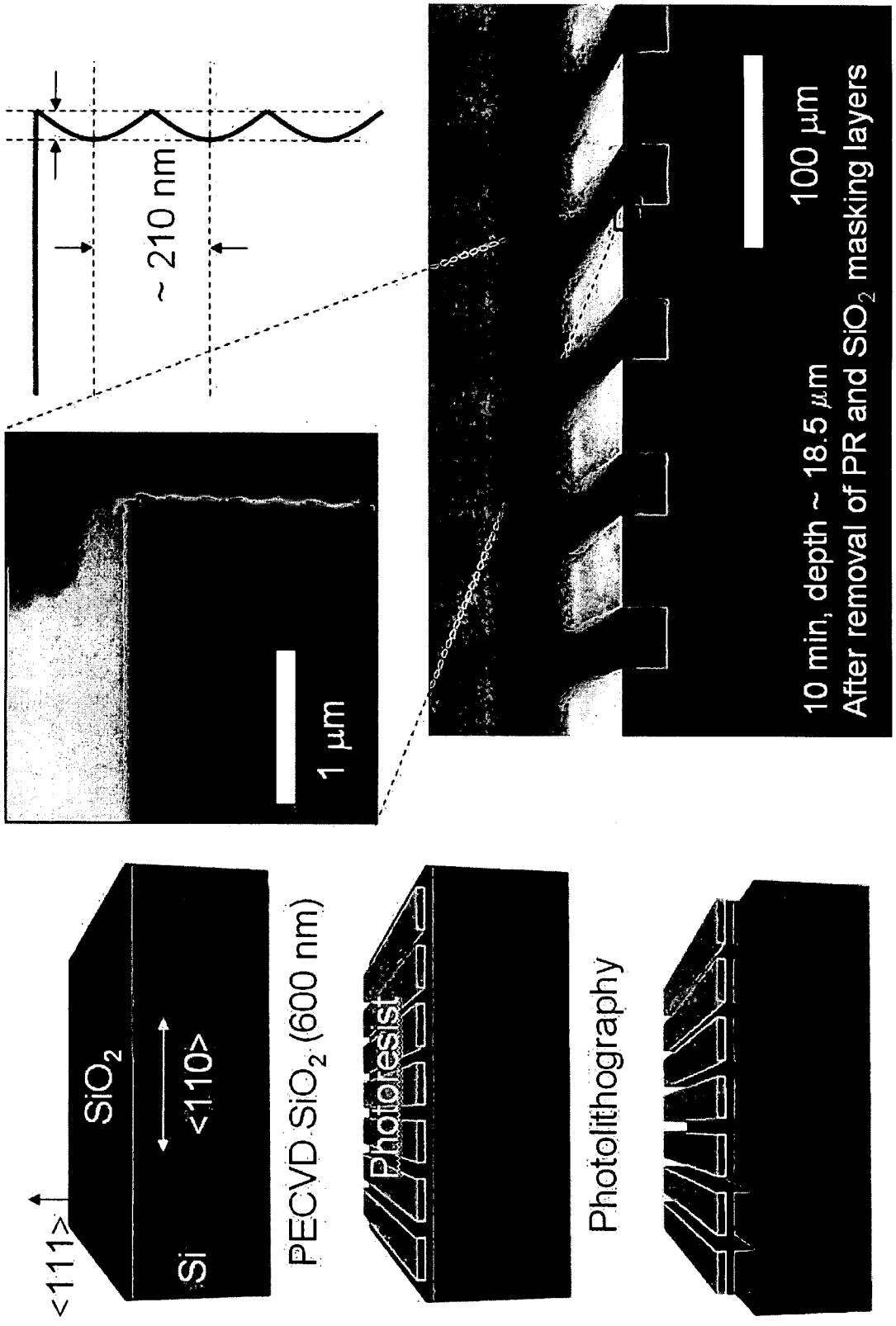

~ 210 nm
1 μm
100 μm
10 min, depth ~ 18.5 μm
After removal of PR and SiO2 masking layers
<111>
SiO2
<110>
Si
PECVD SiO2 (600 nm)
Photoresist
Photolithography

Fig. 64

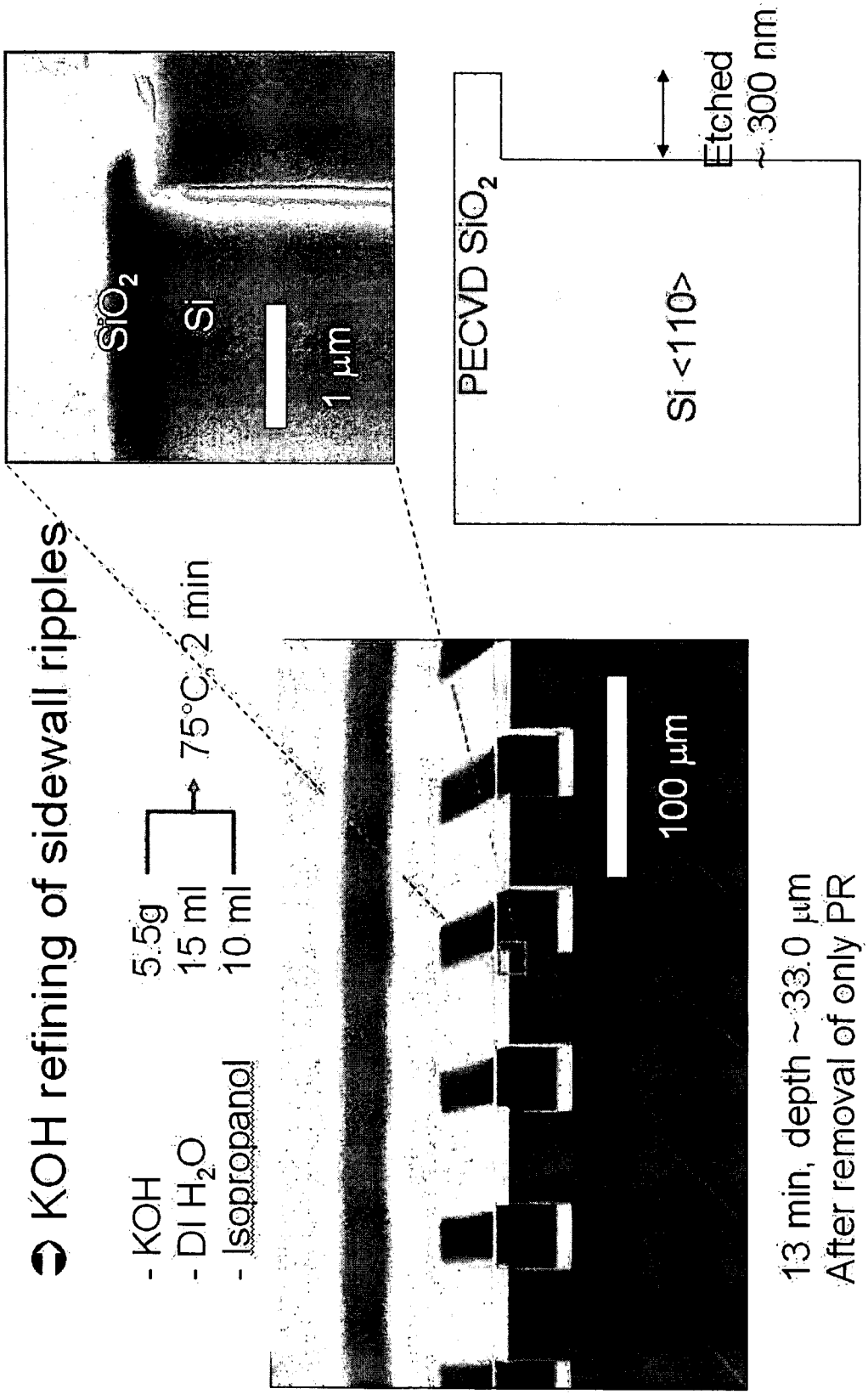
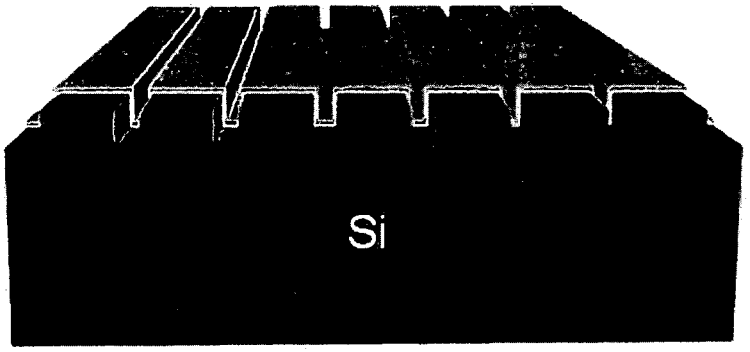
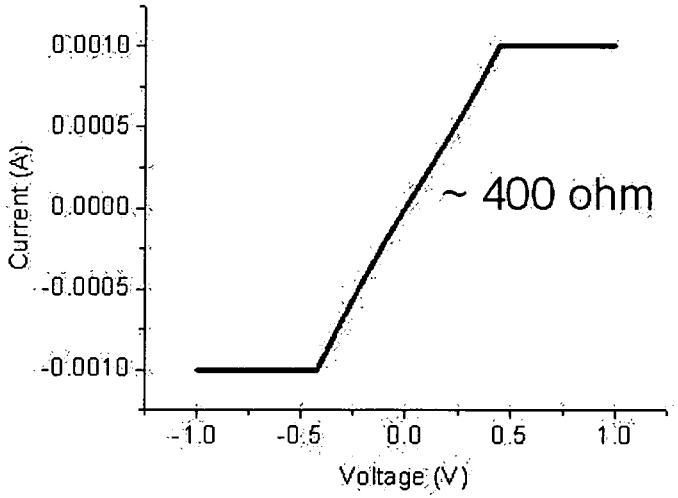

KOH refining of sidewall ripples
- KOH 5.5g
- DI H_2O 15 ml
- Isopropanol 10 ml
75°C, 2 min
SiO_2
Si
1 µm
PECVD SiO_2
Si <110>
Etched ~ 300 nm
100 µm
13 min, depth ~ 33.0 µm
After removal of only PR

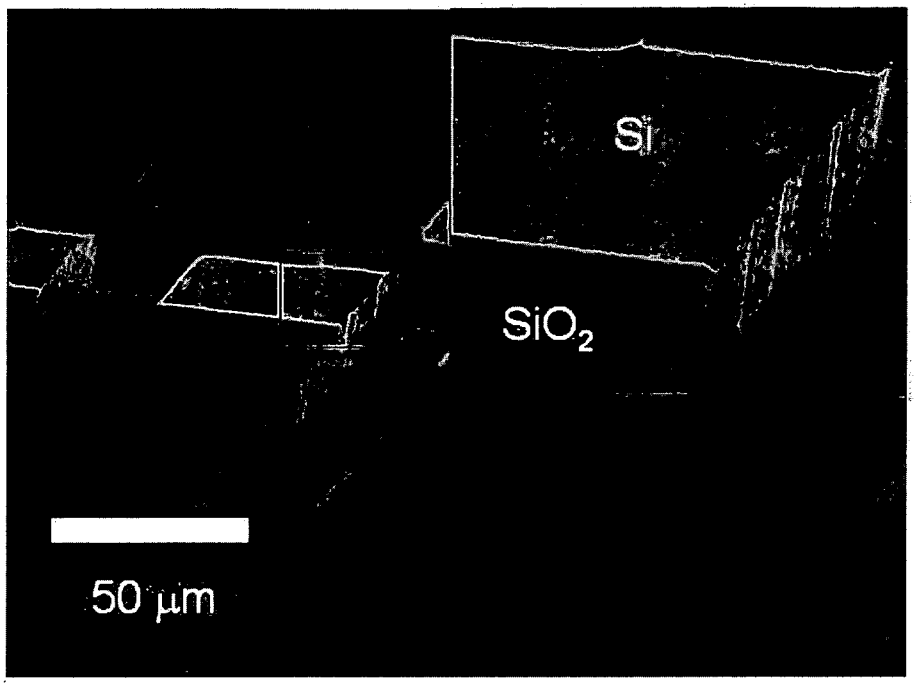
Fig. 65

➲ Doping mask
– PECVD SiO_2 (900 nm)



Boron doping window

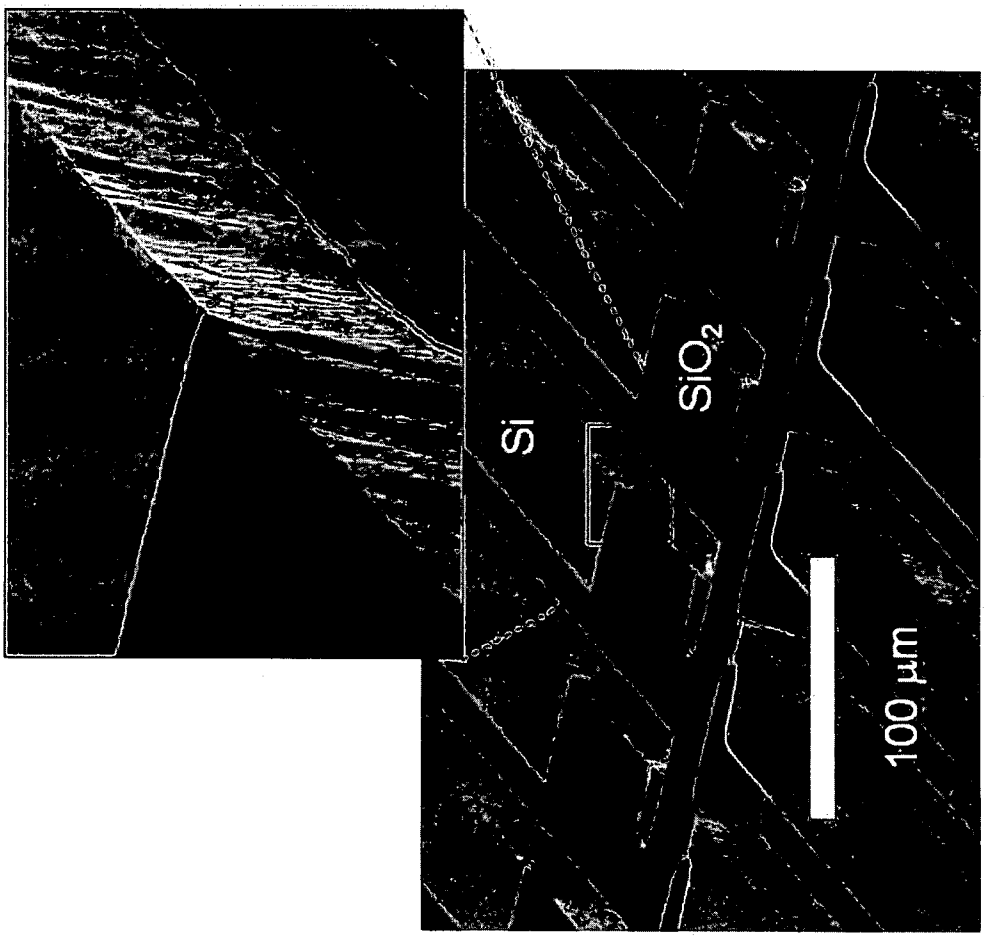




➲ Thick PR (AZ4620) for patterning doping window

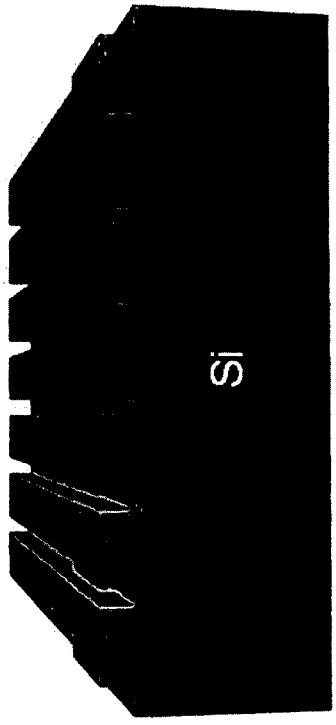
➲ Spin-on-dopant (B219)
Diffusion 1150°C 20 min N_2/O_2 75/25
or
Boron-nitride solid state source
Diffusion 1000°C 15 min N2

Fig. 66



Spin-on-dopant (P509)
Diffusion 950°C 10 min N_2/O_2 75/25

Doping mask
– PECVD SiO_2 (900 nm)



Phosphorous doping window

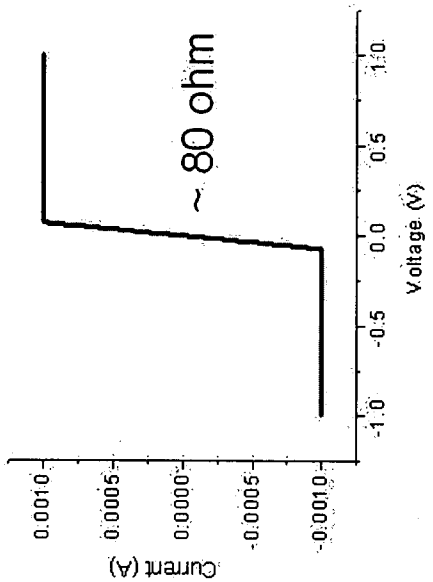
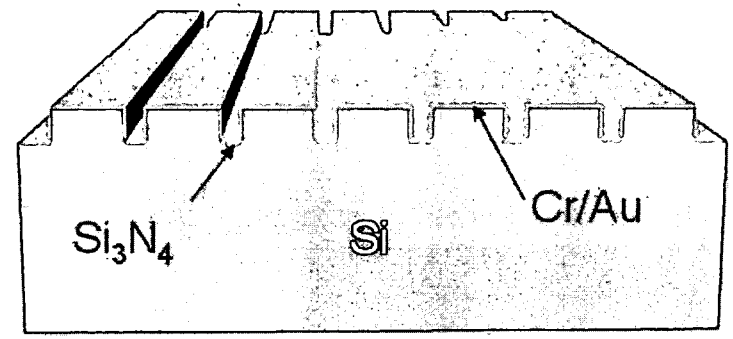
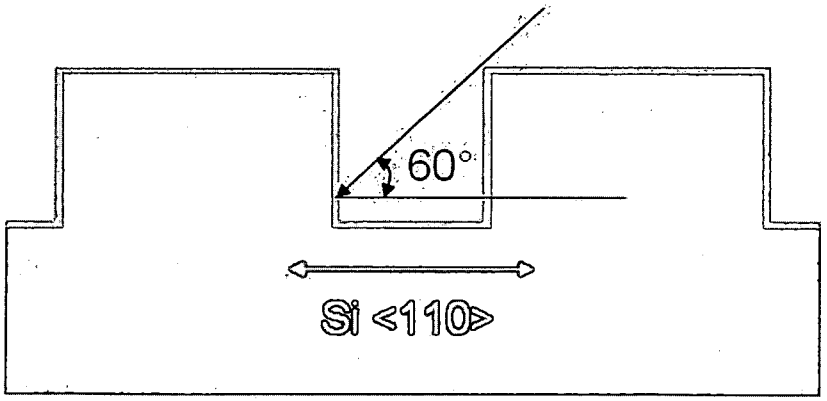


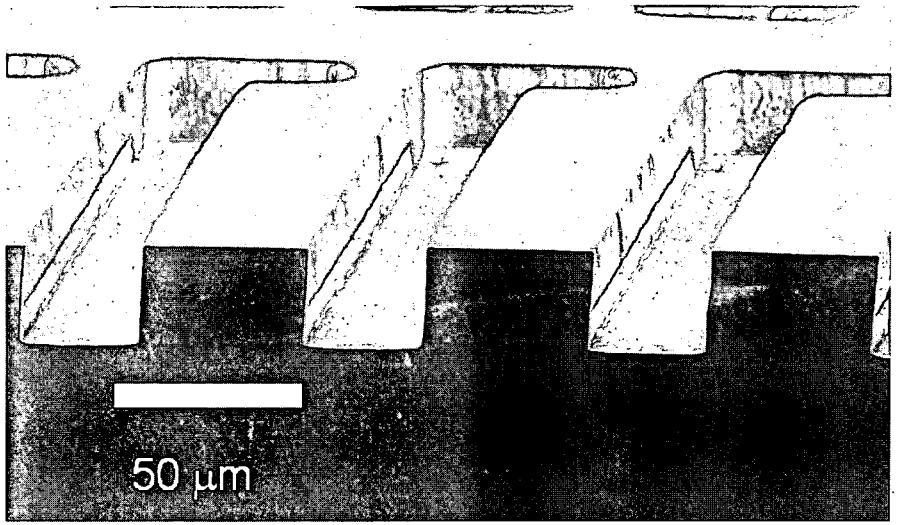
Fig. 67

➲Sidewall passivation

- PECVD: Si_3N_4 (~ 250 nm) @ 350°C
- Angle evaporation: Cr/Au (70Å/700Å), 60°







➲ Metal-covered surface (bright region) is protected from subsequent dry-etching process and thus acts as a passivation layer for KOH wet-etching.

Fig. 68

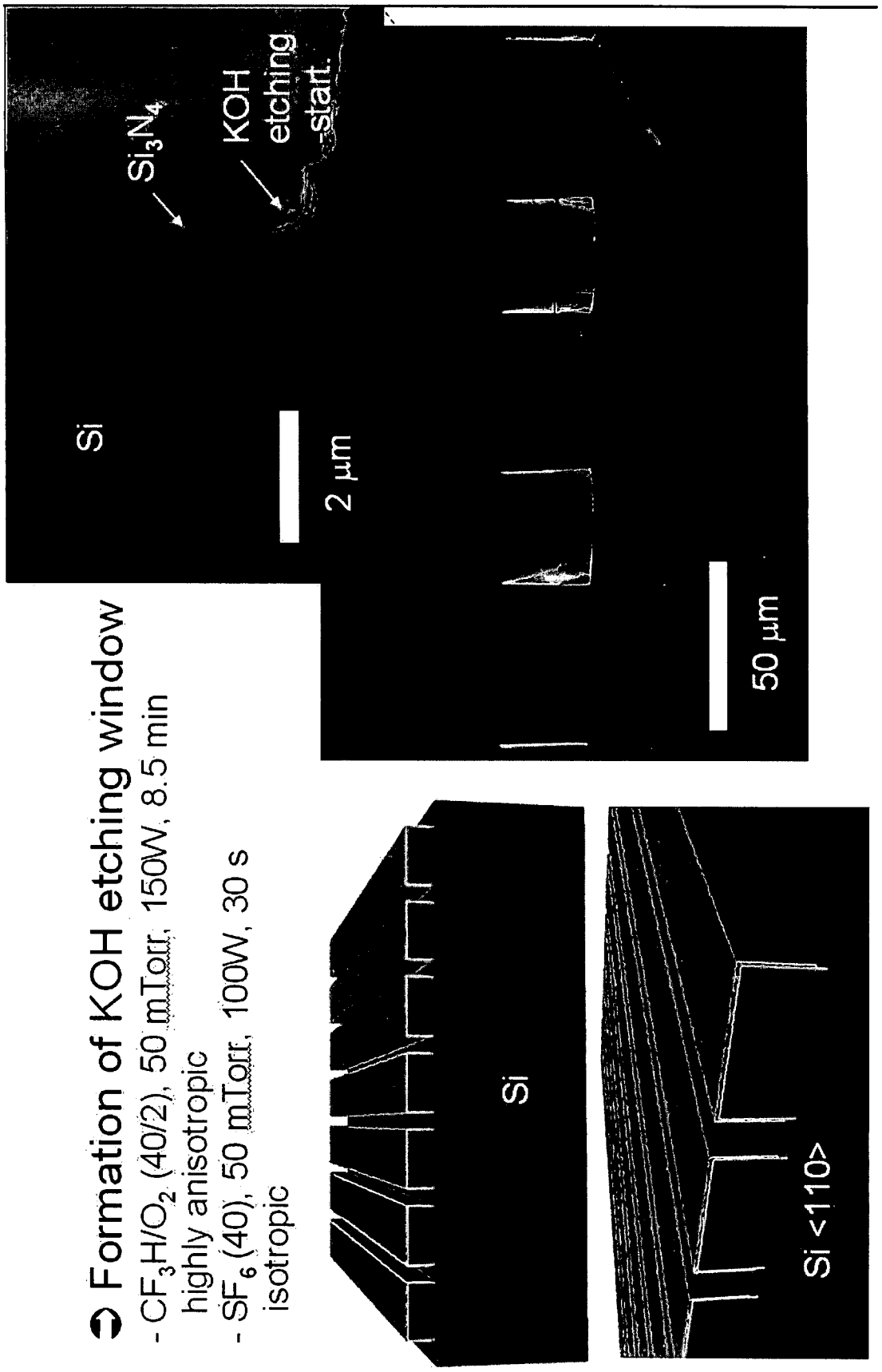

Formation of KOH etching window
- CF_3H/O_2 (40/2), 50 mTorr, 150W, 8.5 min
highly anisotropic
- SF_6 (40), 50 mTorr, 100W, 30 s
isotropic
Si
Si_3N_4
KOH etching start
2 μm
50 μm
Si
Si <110>

Fig. 69

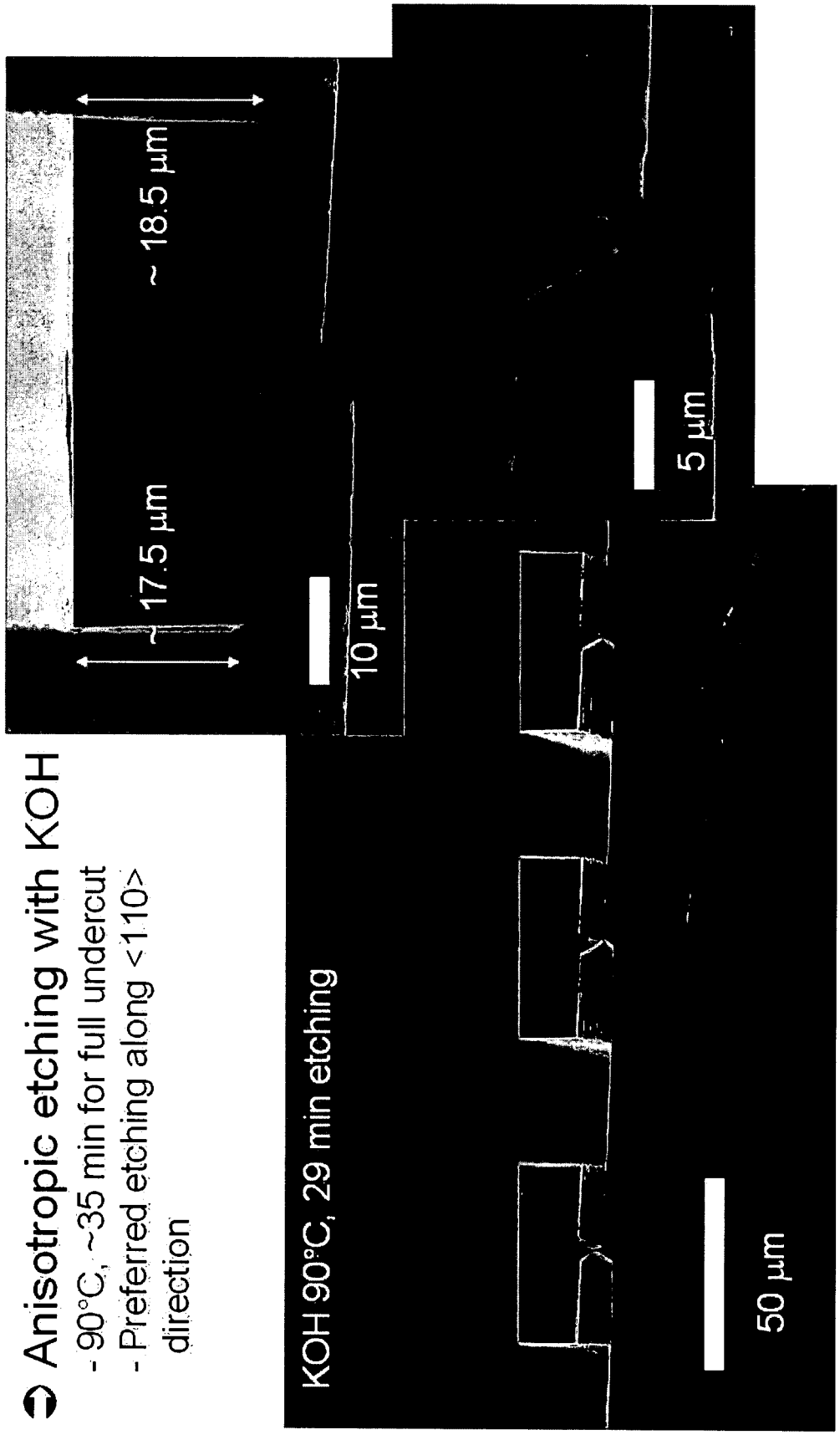

Anisotropic etching with KOH
- 90°C, ~35 min for full undercut
- Preferred etching along <110> direction
KOH 90°C, 29 min etching
~ 18.5 µm
17.5 µm
10 µm
5 µm
50 µm

Fig. 70

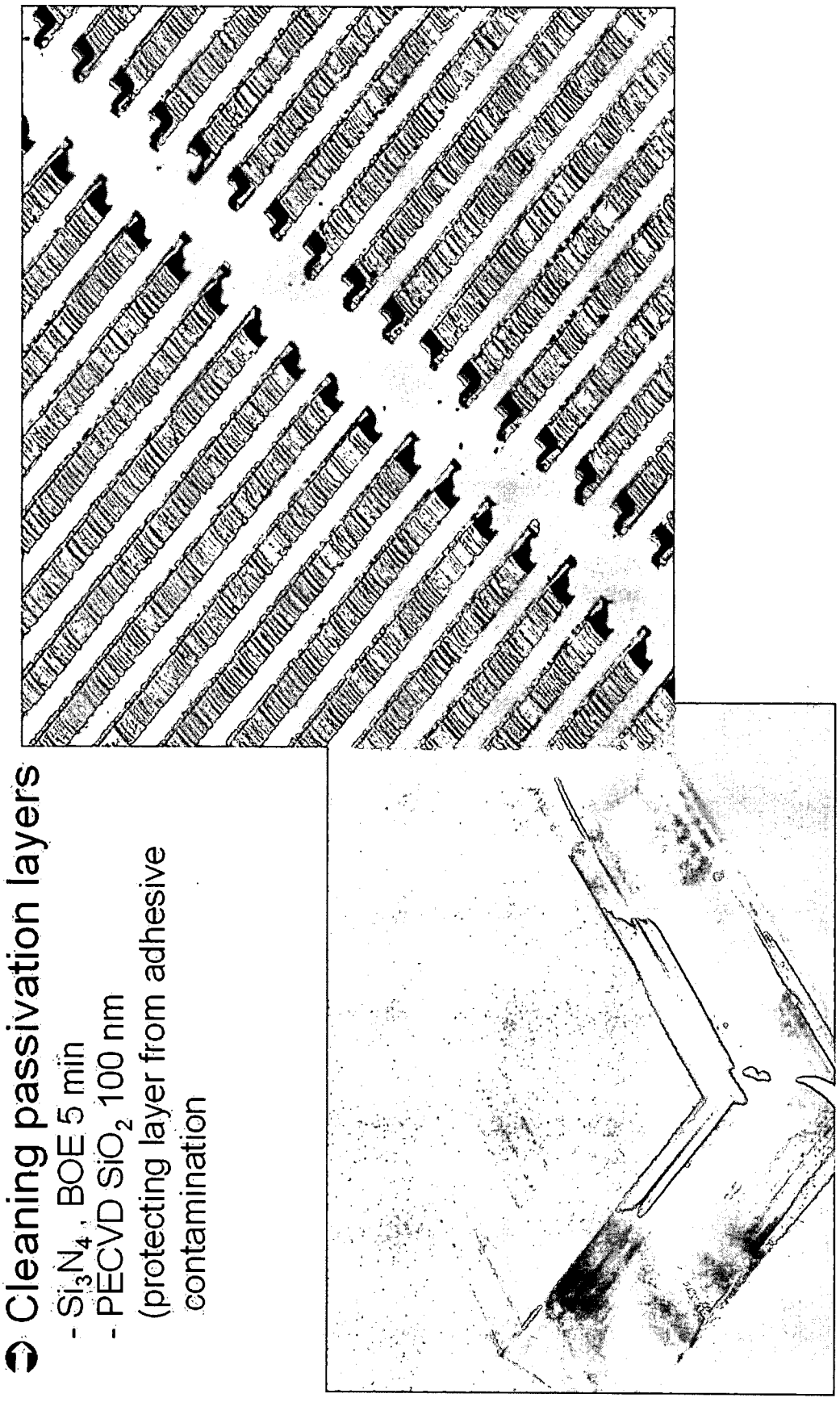

Cleaning passivation layers
- Si_3N_4 , BOE 5 min
- PECVD SiO_2 100 nm
(protecting layer from adhesive contamination

Fig. 71

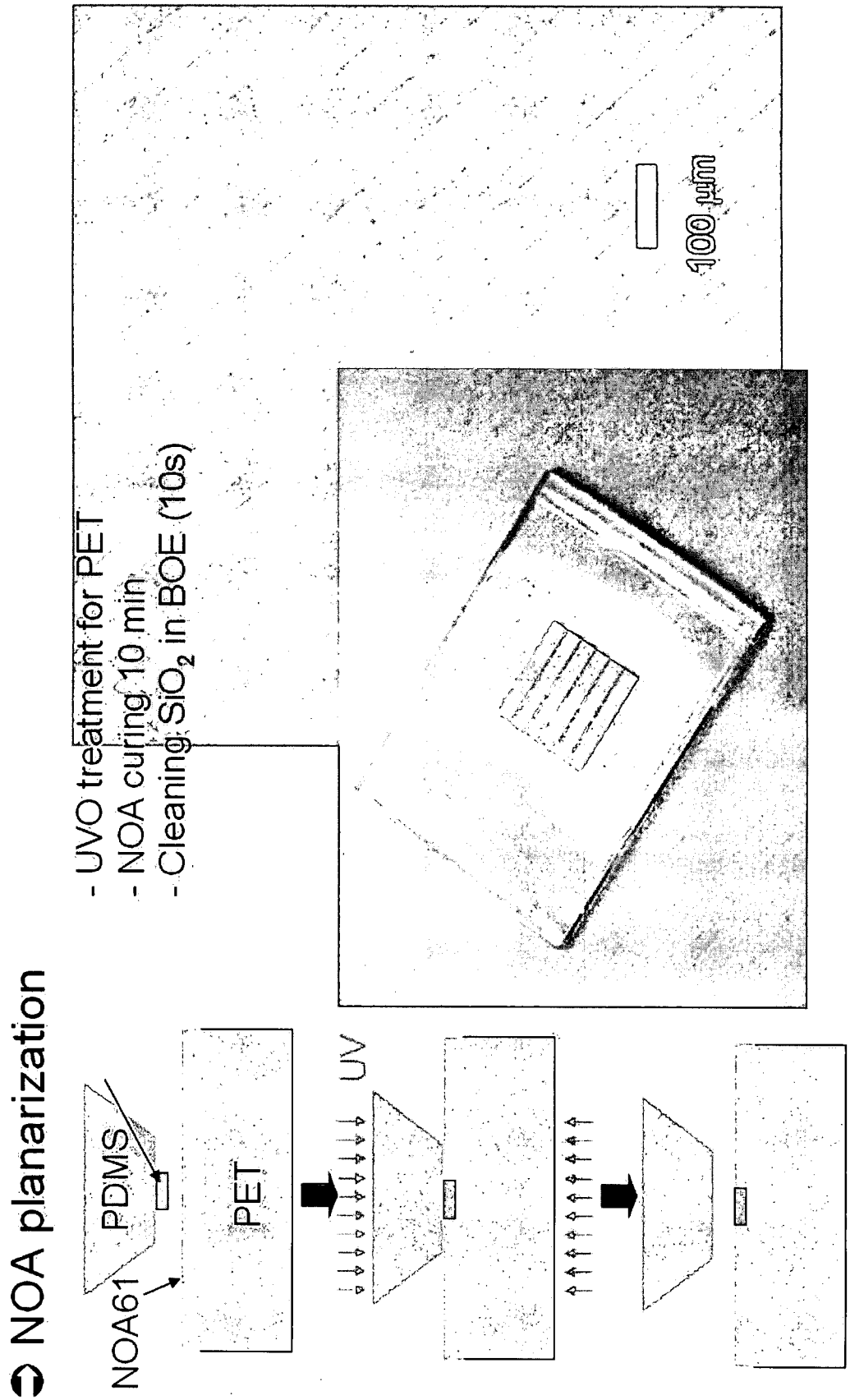

NOA planarization
NOA61
PDMS
PET
UV
- UVO treatment for PET
- NOA curing 10 min
- Cleaning SiO_2 in BOE (10s)
100 μm

Fig. 72

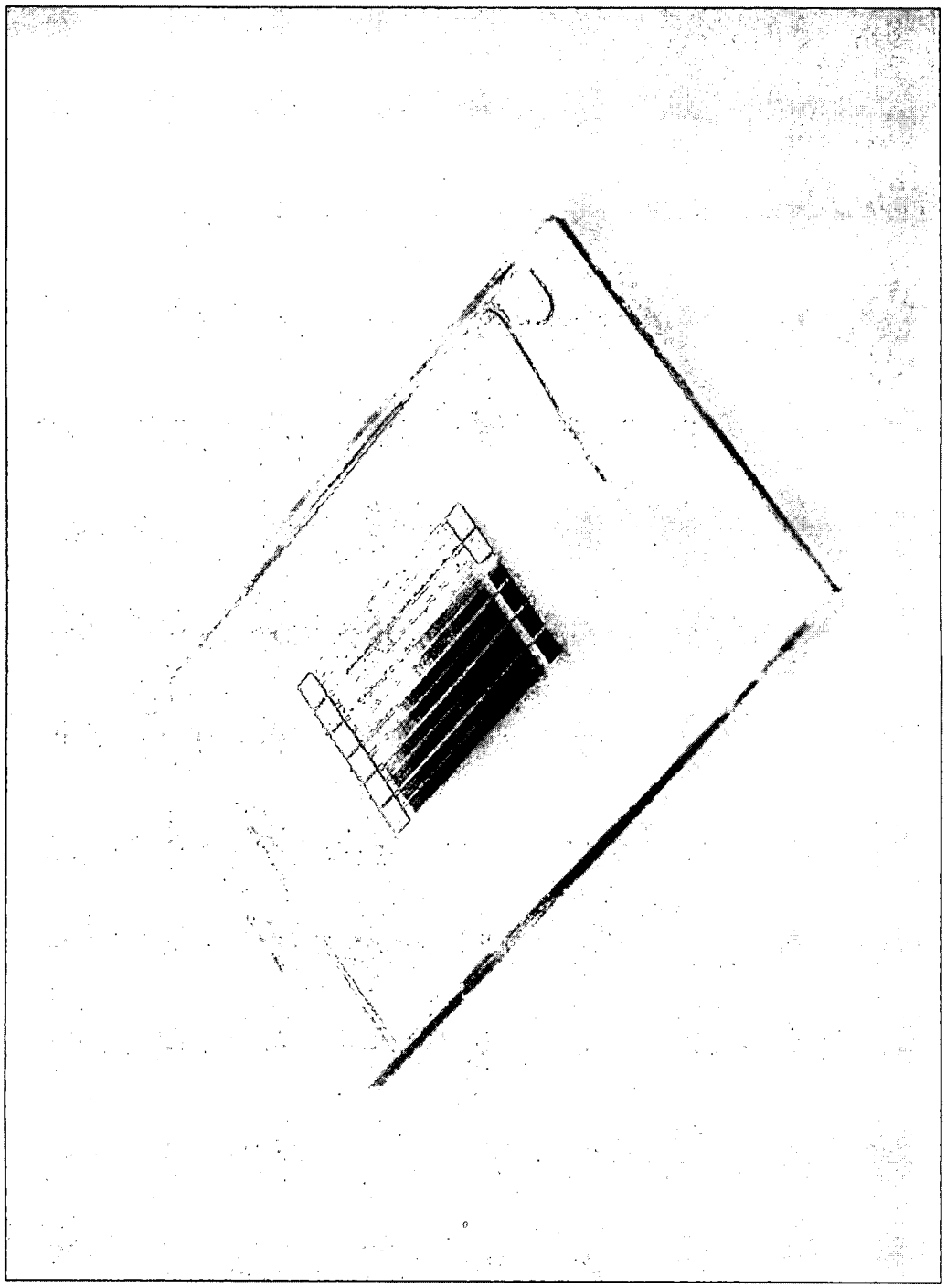


Fig. 73

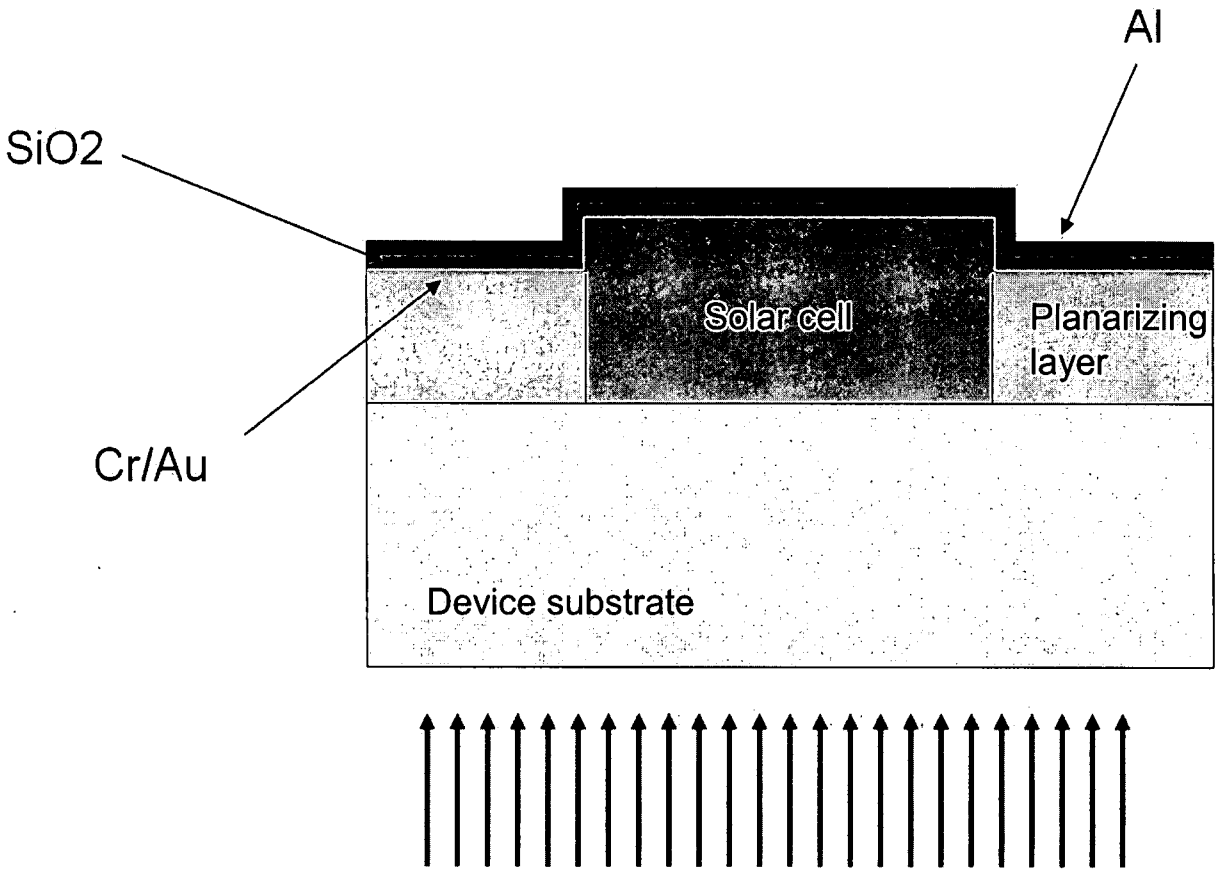

Al
SiO2
Solar cell
Planarizing layer
Cr/Au
Device substrate

Fig. 74

Fig. 75A – Top Plan View

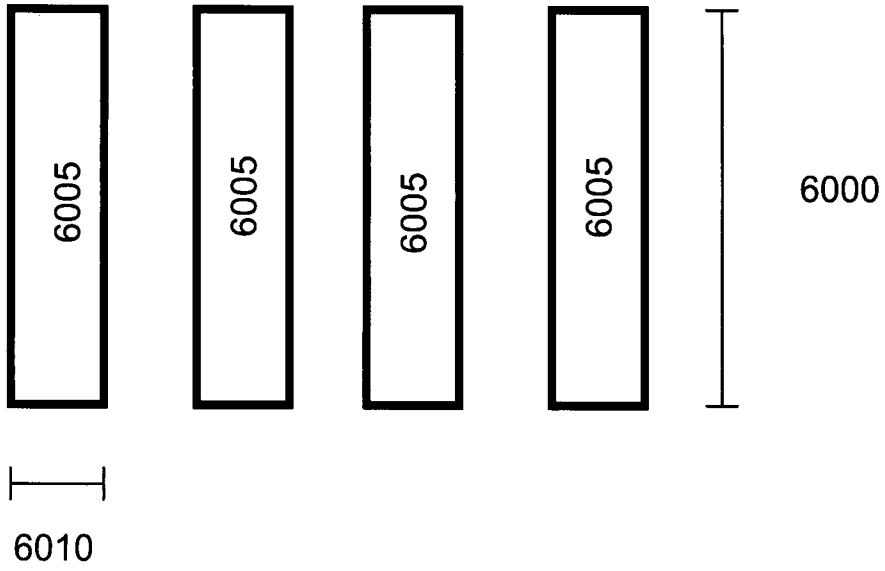
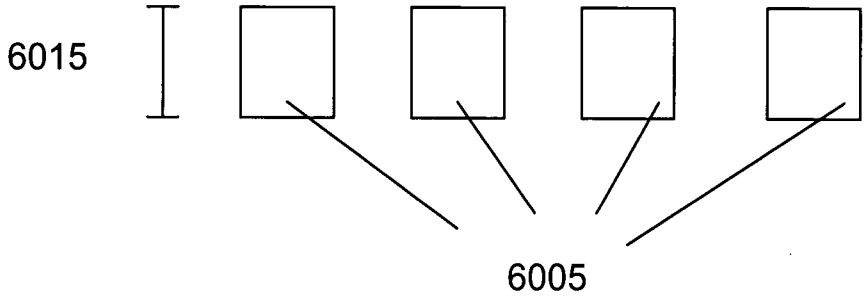
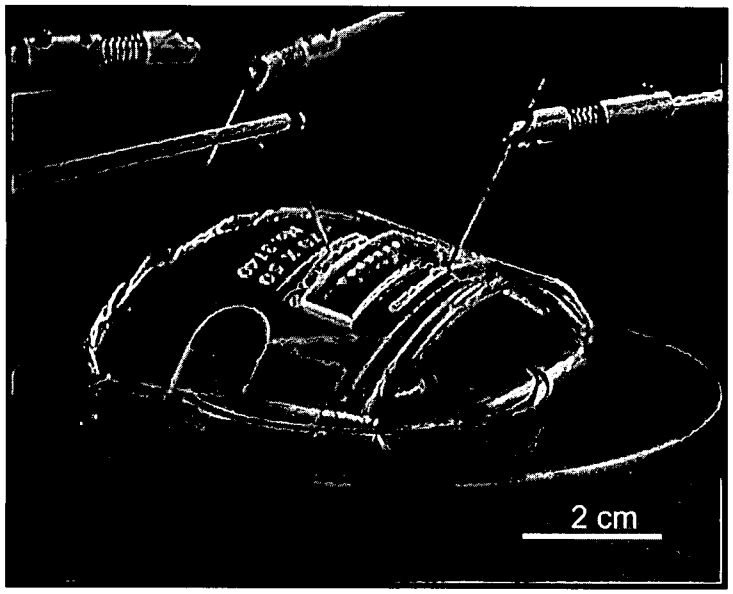
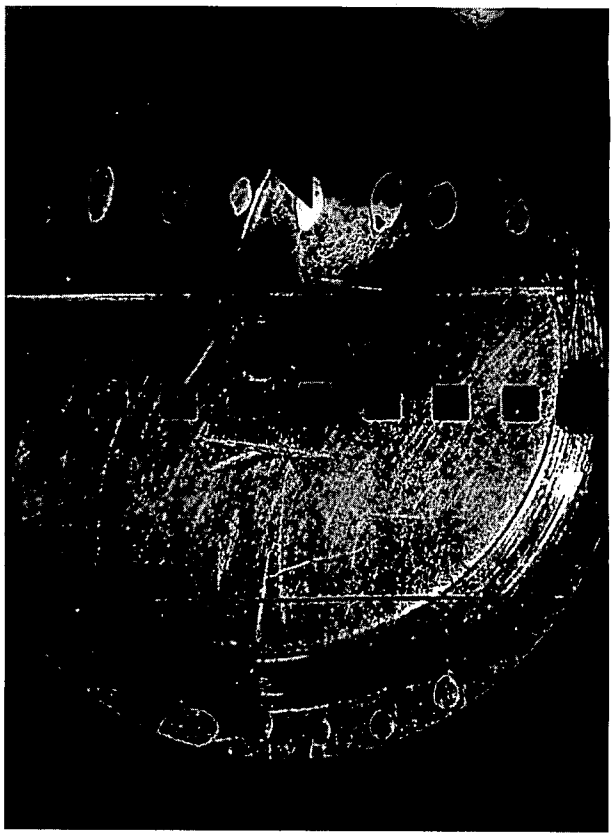


Fig. 75B – Cross Sectional View







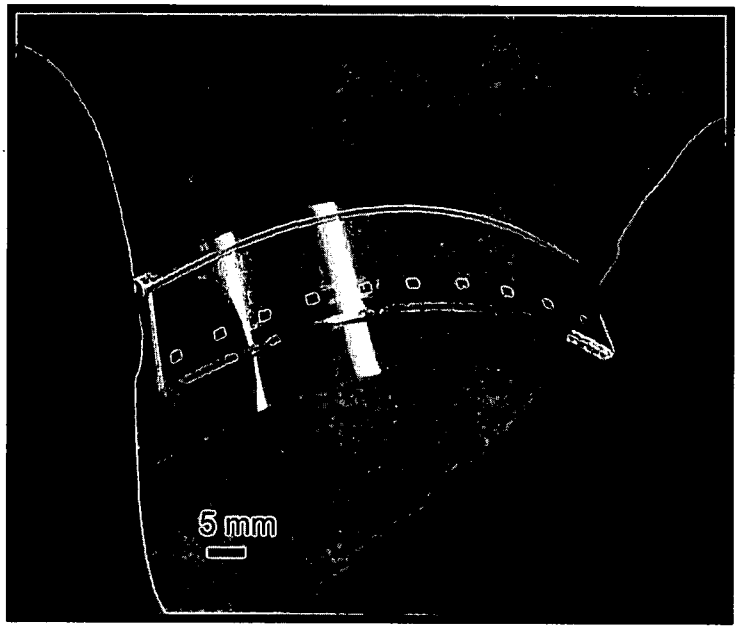


Fig. 76