

CERAMIC-ON-METAL CIRCUIT BOARD

DUPLICATE

As known in the art, multi-layered, co-fired, ceramic circuit boards are fabricated from a stack of layers of ceramic dielectric tape sold under the trademark, GREEN TAPE, by the E. I. Du Pont Company of Wilmington, Del. Each layer of the ceramic tape has a thickness of about five mils (0.13mm). The surface of each layer may have metallic conductors printed thereon that can be electrically interconnected by means of small holes (known as vias) in one or more of the layers. The holes are filled with a conductive material. Such a co-fired, ceramic circuit board is described in U.S. Patent No. 5,041,695 issued on Aug. 20, 1991 to J. A. Olenick.

Two types of co-fired, ceramic circuit boards are available. These are: (i) high temperature fire (typically below 1300°C) and (ii) low temperature fire (typically below 1000°C). The high temperature, co-fire technology is used for alumina and aluminum nitride ceramics, whereas the low temperature, co-fire technology is used for glass ceramics (ceramic filler filled vitreous glasses or devitrifying glasses). The conductor metallurgy for high temperature, co-fired boards is W or Mo-Mn, whereas low temperature, co-fired circuit boards utilize Ag, Au, AgPd or Cu conductors.

Shrinkage in volume, experienced by the ceramic bodies after firing, is a problem encountered in the fabrication of multi-layered, co-fired, ceramic circuit boards. This shrinkage, which occurs in the x and y surface dimensions as well as in the z thickness dimension of the respective layers, results from the release, during firing, of the air distributed between the particles as well as the organic binder material in the green tape. Such shrinkage is quite high, typically 10-15% for low

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Drawing(s)	☐
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☒ Description	: paged 1 to paged 15
☒ Claim(s)	: paged 4 to paged 24
☒ Drawing(s)	: paged 1/4 to paged 2/4
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1 temperature, co-fired circuit boards. While one can
attempt to compensate for such shrinkage in the x and y
surface dimensions by oversizing the area of the green
5 tape layers, it is quite difficult to control shrinkage
consistently. For example, in order that the variation
in the x and y dimensions of the multi-layered circuit
board, after firing, be maintained within 0.1%, a degree
of control that may be as large as one to two parts in one
10 hundred in the amount of shrinkage is required. Because
of this, the yield on co-fired circuit boards is low. In
addition, the low temperature, co-fired circuit boards
suffer from poor thermal conductivity and low flexure
strengths associated with the glass ceramic.

15 A single layer of ceramic fired on a metal base,
such as porcelain enamel-on-steel, is known in the art.
Because the temperature coefficient of expansion exhibited
by the steel, which comprises such a base, is relatively
large, the composition of the ceramic layer fired on the
steel base also must exhibit a relatively large
20 temperature coefficient of expansion, in order to closely
match that of the base. High barium, high-expansion
glass-ceramics have been developed which may be used to
fabricate such porcelain enamel-on-steel boards. While
other ceramic composition systems are known that exhibit a
25 relatively large temperature coefficient of expansion,
high-expansion in these systems is typically achieved by
the addition of heavy metal oxides, such as, lead, barium, or
alkali, e.g., sodium and potassium. However, this results
in higher dielectric constants and higher dielectric
30 losses, and may lead to poor chemical durability, which
makes such high-expansion systems poor candidates for use
in fabricating multi-layered, co-fired, ceramic circuit
boards that may be employed in microelectronic packaging.

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1 The present invention is directed broadly to a
multi-layered, co-fired ceramic on a metal base and, more
particularly, to a system of low temperature, co-fired,
5 high-expansion glass ceramics that, when fine-tuned with
certain fillers, exhibit dielectric constants and
dielectric losses that are sufficiently low to make them
suitable for use in the fabrication of multi-layered,
co-fired ceramic-on-metal circuit boards suitable for
10 microelectronic packaging. The invention is further
directed to a method of fabricating such circuit board
utilizing a glass bonding layer to securely attach the
ceramic to the metal base.

In the drawings:

15 Fig. 1 diagrammatically illustrates an example of a
microelectronics package fabricated in accordance with the
present invention.

Fig. 2 is a flow chart of the process steps
involved in the present invention.

20 BRIEF DESCRIPTION OF THE PREFERRED EMBODIMENTS

The fabrication process, embodied in Fig. 1, generally
comprises forming a metal base 12 having two oppositely
disposed major surfaces 14 and 16, for example, by stamping
25 a metal core (not shown) and then annealing the core at a
temperature of about 500 to 900°C to provide dimensional
stability. The surfaces of the core are cleaned to remove
dirt and oxide. Preferably, at least one of the major
surfaces 14 and 16 is plated with a suitable material,
30 such as Cu, to a thickness of about 0.5 to 25.0 microns.
Suitable materials for the base 12 include Cu, Al, Ni,
stainless steel, low carbon steel, Cu/Invar/Cu, Cu/Mo/Cu
or Cu/stainless steel/Cu, the latter being preferred.

35 A bonding layer 18, of a glass having a
coefficient of thermal expansion less than that of the
base 12, is applied, as a slurry, to one major surface,
for example, surface 14, of the base 12. The slurry can be



1 applied by screen printing, spraying, spin coating,
curtain coating, fluidized-bed coating, electrophoretic
deposition or other equivalent methods. Circuit boards
made according to the present invention utilized screen
5 printing and spraying methods. A multi-layered ceramic 20
is provided on the glass bonding layer 18.

The multi-layered ceramic 20 may be formed by
applying multiple layers of green tape to the glass
bonding layer, or the laminated ceramic structure may be
10 bisque fired prior to being placed on the glass bonding
layer 18. For a Cu/stainless steel/Cu base, the resultant
structure is co-fired in nitrogen (about 10,000 ppm O₂)
at a peak temperature of about 900-930°C for about 2 to
20 minutes to bond the ceramic 20 to the surface 14 of the
base 12. The intermediate glass bonding layer 18 serves
15 two functions; it provides a means of attaching the
multi-layered ceramic 20 to the base 12, and it minimizes
the shrinkage of the ceramic 20 in the x and y dimensions
during the firing. The glass bonding layer 18, in
20 addition to having a coefficient of expansion less than
that of the metal base 12, must be sufficiently reactive
with the copper plating and the copper oxides on the
surface 14 of the base 12 to promote and maintain adhesion
between the ceramic 20 and the base during the co-firing
25 operation. The glass of the bonding layer 18 must have a
relatively low softening point (<600°C) so that it can
flow and bond to the surface 14 of the metal base 12, and
possess appropriate surface tension characteristics at
temperatures below the softening point of the glass in the
30 ceramic layer 20 to minimize the lateral (x and y)
shrinkage of the ceramic. Additionally, the glass of the
bonding layer 18 also must possess good chemical
durability and dielectric properties.

The composition of the glass bonding layer 18 is
35 influenced by the composition of the metal core and its
thermal characteristics, as well as the composition of the



ceramic laminate, the sintering characteristics and the process employed for fabricating the co-fired, ceramic-on-metal circuit board. Each layer of the multi-layered ceramic 20 comprises a glass-ceramic/filler composition having a coefficient of thermal expansion that closely matches that of the base 12 and the glass bonding layer 18, over the temperature range from room temperature to about 600°C. A number of glass compositions from the multi-component system $\text{PbO-ZnO-BaO-B}_2\text{O}_3\text{-SiO}_2$ are suitable for the glass bonding layer 18. These glass compositions may also contain small amounts of ZrO_2 and Al_2O_3 . Some of the generalized compositions and their typical properties are listed in Table I.

TABLE I

Glass System	Thermal Coefficient of Exp. (10^{-7})/°C	Softening Point (°C)
Pb-borate	75-120	280-430
Pb-Zn-borate	70-110	320-450
Pb-borosilicate	40-120	370-700
Pb-Zn-borosilicate	75-80	370-700
Pb-Zn-Ba-borosilicate	75-100	380-400
Pb-alumino silicate	60-85	440-485
Pb-alumino borosilicate	80-90	390-440

Ceramic-on-metal circuit boards have been made according to the present invention using glasses selected from the Pb-Zn-borosilicate and Pb-Zn-Ba-borosilicate glass systems listed in TABLE I. The preferred glass, from the Pb-Zn-Ba-borosilicate system, is a commercially available glass identified as SCC-11, available from SEM-CON Co. (Toledo, OH). Another suitable glass from this same system is commercially available as CV-808 from Owens Illinois (Toledo, OH). This latter glass contains a small amount of ZrO_2 . A suitable glass from the Pb-Zn-borosilicate system is CV-101, also commercially available from Owens Illinois.

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1 These bonding glasses have been successful in
providing good adhesion of the laminated ceramic to a
Cu/stainless steel/Cu base 12. Furthermore, the x-y
shrinkage of the laminated ceramic layer 20 is
5 decreased by more than an order of magnitude, to, about
0.8%, by using these glasses. The x-y shrinkage of the
ceramic laminate is typically 12-15% in the absence of
the glass bonding layer 18. In addition, the metal
base 12 exhibits good thermal conductivity and high
10 flexure strength, thereby overcoming the problems of
poor thermal conductivity and low flexure strength
suffered by prior-art circuit boards comprising only
multi-layers of low temperature, co-fired, glass
ceramic.

15 The conductor metallurgy can be Ag, Au, AuPt,
AgPd, Ni, or Cu. Nitrogen or any other inert
atmosphere may also be required to fire precious metal
conductor co-fired circuit boards to prevent oxidation
of the metal base. Appropriate slots can be provided
20 in the laminated tape for integrated-circuit chips to
be placed directly on the metal base using adhesive,
solder attachment, or other direct bonding method to
provide very efficient heat spreading. High density
circuitry can be produced on the co-fired ceramic
25 using photolithography for top layer conductors. It
is also possible to spin-on additional polymer layers
on the co-fired ceramic and then use thin film-plating
techniques to form very high density circuitry.

30 The co-fired circuit board on metal base
technology disclosed herein, in addition to producing
high density circuit boards with excellent thermal
dissipation and shrinkage control characteristics,
helps to obtain a mechanically rugged base. Also, the
integrated circuit chips and other components can be
35 attached directly on the metal by providing slots
either in the green tape, as shown in Fig.1 and discussed
below, or on the opposite surface of the metal base
from the multi-layered ceramic. Components can be



1 attached by soldering, wire bonding, TAB, flip-chip or
 adhesive attach. The packages can be hermetic
 (glass-sealing on metal) or non-hermetic with appropriate
 encapsulation for component protection.

5 While it is not intended to limit the multi-layered,
 co-fired ceramic-on-metal technology of the present
 invention to any particular application, its suitability
 for microelectronic packaging depends on the fired
 multi-layered ceramic exhibiting appropriate electrical
 10 properties, in addition to having other appropriate
 properties for this purpose. In this regard, reference is
 made to the following Table II, which is an example of
 electrical and other property value constraints required
 of the fired multi-layered ceramic in one practical case
 15 of microelectronic packaging.

TABLE II

Property	Desired Value
Coef. of Thermal Expansion (25-250°C)	90-130x10 ⁻⁷ /°C
20 Dielectric Constant (1 MHz)	<6.6
Dissipation Factor (1 MHz)	<0.0035
Breakdown Voltage	>2 kV/mm
Specific (Volume) Resistivity	>10 ¹² Ω cm
Resistivity of buried conductor	<10 mΩ/square
25 Resistivity of via conductor	<50 mΩ/square
Resistivity of surface conductor	<50 mΩ/square
Camber	<0.005"/inch
Long term reliability (HHBT conditions)	no shorts

30 In Table II, HHBT conditions, with respect to long
 term reliability, refers to an accelerated aging test, in
 which a microelectronic packaging sample, under high
 humidity and high temperature conditions, withstands a
 given voltage stress for a given time without electrical
 breakdown.

35 The application of the multi-layered, co-fired,
 ceramic-on-metal technology of the present invention to
 microelectronic packaging required the development of
 glass-ceramic (GC) compositions capable of being used in



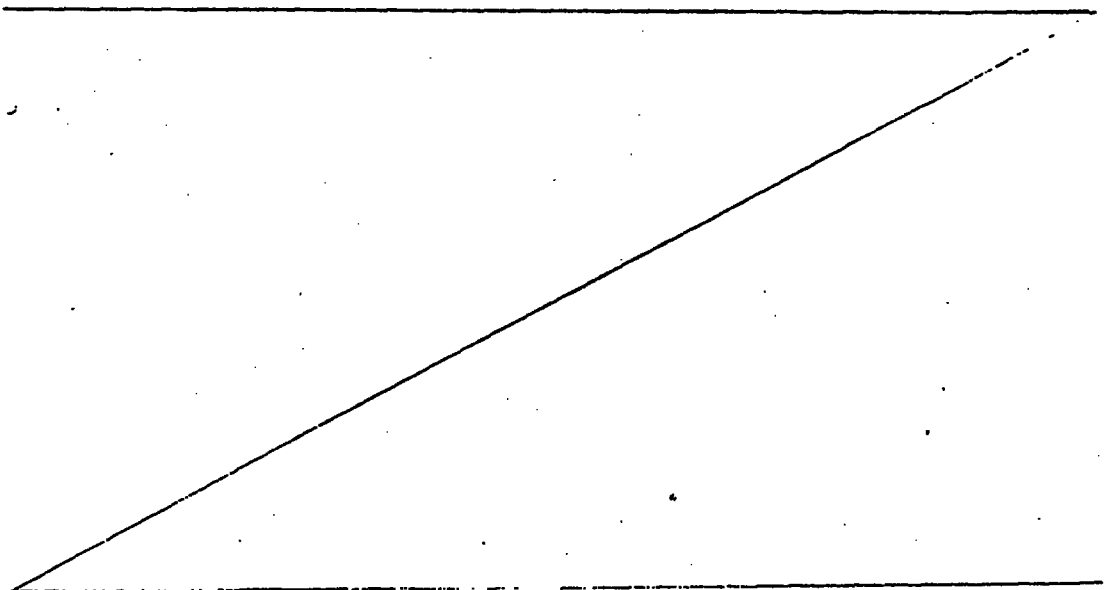
1 glass-ceramic+filler (GC/F) compositions that meet the
constraints set forth above in Table II.

5 In the past, glass, glass-ceramic, and glass+filler
systems have been developed and successfully employed in
microelectronics packaging for high density packaging
applications. The major advantage of these materials over
the conventional ceramics such as alumina is the lower
firing temperature, which enables the use of higher
electrically conductive Ag, Cu, Au, and Ag-Pd as
10 compatible metallizations. There was a proliferation of
glass-ceramic and glass+filler systems during these
developments; however, emphasis was laid on matching
thermal expansion to silicon and in some cases to Ga-As.
Thermal expansion coefficients typically ranged from
15 $30-70 \times 10^{-7}/^{\circ}\text{C}$. The issues related to controlling
dielectric constant, dielectric loss, strength, bulk and
surface resistivities, electrical breakdown strength,
chemical durability, shrinkage during firing, and
compatibility with metallization were addressed in a broad
20 range of borate, boro-silicate, and silicate glass and
glass-ceramic systems containing low or intermediate
expansion fillers such as alumina, cordierite, forsterite,
eucryptite, etc. However, none of these glass,
glass-ceramic, and glass+filler systems substantially
25 exhibits the property-value constraints set forth in Table
II. In particular, the expansion coefficient of these
prior-art composition systems is too low to be
successfully employed in the fabrication of multi-layered,
co-fired, ceramic-on-metal, high density circuit boards.

30 It is one of the objects of the present invention
to (1) identify a glass-ceramic system, and specific
glass-ceramic compositions within this system, with
suitable thermal, electrical, chemical, and mechanical
properties that make them likely candidates for use in
35 fabricating a multi-layered, co-fired, ceramic-on-metal,
high density circuit board, and (2) then incorporate
appropriate fillers in such likely GC candidates to
fine-tune the composite GC/F to substantially meet the
property value constraints set forth in Table II.



1 In this regard, Table III, set forth below, is
directed to an $\text{MgO-B}_2\text{O}_3\text{-SiO}_2$ system, containing CaO ,
5 ZnO , and SnO_2 as additives, that was chosen for the
development of likely glass-ceramic (GC) candidates for
use in fabricating a multi-layered, co-fired,
ceramic-on-metal, high density circuit board. No alkaline
oxides are deliberately added to the glasses, but they may be
present as impurities in the raw materials. ZrO_2 was
10 incorporated in all compositions as a nucleating agent for
controlled crystallization. The compositions of the
different glasses that were prepared and evaluated are
shown in Table III. Glass-ceramics were produced by
heat-treating the glasses at $850\text{-}950^\circ\text{C}$ for 10-30
15 minutes. The thermal expansion coefficient of the
resultant glass-ceramics ranged from 85 to $105 \times 10^{-7}/^\circ\text{C}$
over a temperature range from room temperature (RmT) to
about 600°C (as specifically exemplified below in Table
20 III by the thermal expansion coefficient of each of
glass-ceramics GC-1 to GC-7), which is appropriate for
further tailoring by incorporation of fillers.
Sensitivity to moisture was evaluated by exposing the
glass-ceramics to steam at 15 psi for twelve hours. All
the compositions showed no clear evidence of deterioration
in moisture.



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TABLE III

Candidate Glass-Ceramic Compositions in the MgO-B₂O₃-SiO₂ System $\alpha \times 10^{-7}/^{\circ}\text{C}$

(Weight %)

Id.	SiO ₂	B ₂ O ₃	MgO	ZnO	CaO	SnO ₂	BaO	ZrO ₂	Cr ₂ O ₃	RmT-600°C
GC-1	17	28	45	8.5	-	-	-	1.5	-	92
GC-2	17.8	31.0	48.6	-	-	-	-	2.6	-	97
GC-3	16.4	28.5	43.2	9.5	-	-	-	2.4	-	105
GC-4	17.5	29.5	43	-	4	-	-	2.0	-	86
GC-5	14.5	25.2	34.7	5.6	4.8	13.0	-	2.1	-	84
GC-6	14.3	24.8	34.2	-	6.7	17.9	-	2.1	-	86
GC-7	16.9	30.0	39.1	9.1	3.7	-	-	1.2	-	85
GC-8	15.9	28.3	41.2	9.23	4.2	-	-	1.2	-	-
GC-9	17.5	31.8	43.0	-	6.53	-	-	1.2	-	-
GC-10	16.7	30.4	29.9	-	21.9	-	-	1.1	-	-
GC-11	16.1	28.5	25.1	8.7	20.5	-	-	1.1	-	-
GC-12	16.8	29.8	38.8	9.1	3.6	-	-	0.9	1.0	-
GC-13	15.8	28.0	34.4	8.5	3.4	-	8.0	0.4	1.5	-
GC-14	16.6	30.0	31.8	8.4	3.4	-	7.9	0.4	1.5	-

Based on the compositions of the glass ceramics GC-1 through GC-14, the following composition ranges (by weight percent) are identified to be suitable for expansion matched glass-ceramics co-fired on CU/stainless steel/Cu metal cores:

SiO ₂	10-20%
B ₂ O ₃	20-35%
MgO	25-50%
ZnO	0-10%
CaO	0-22%
SnO ₂	0-18%
BaO	0-10%

It may be possible to incorporate other oxides, including alkali and heavy metal oxides, in small quantities with minor effect on dielectric constant and dielectric loss. Other nucleating agents such as TiO₂ and P₂O₅ also may be used instead of ZrO₂. For example, up to 5% by weight (individual or combined) of these nucleating agents can be included. For obtaining suitable color, up to 3% by weight (individual or combined) of Cr₂O₃, CoO, Fe₂O₃, CuO, CeO₂, and/or Pr₂O₃ may be incorporated. Further, the glass-ceramic may include, as other additives, up to 10% by weight (individual or combined), Li₂O, Na₂O, K₂O, Al₂O₃, PbO, Bi₂O₃, and/or SrO.

Three fillers were chosen as candidates for tailoring the glass-ceramic properties. They are Fluorspar (CaF₂), Quartz (SiO₂), and Cristobalite (SiO₂). The thermal expansion coefficients of Fluorspar, Quartz, and Cristobalite in the range of 20 to 600°C are 225, 237, and 271x10⁻⁷/°C respectively. Several glass-ceramic/filler (GC/F) combinations were processed by standard tape casting procedures. One or more of these fillers, up to 50% by volume, were considered for altering the expansion and dielectric constant of the base glass-ceramics (GC). By varying the



amount of filler in the glass-ceramic/filler system, the expansion coefficient of the glass-ceramic/filler (GC/F) systems can be increased up to $130 \times 10^{-7}/^{\circ}\text{C}$.

Five novel glass-ceramic/filler materials (GC/F-1 to GC/F-5) having properties suitable for use in fabricating multi-layered, co-fired, ceramic circuit boards are shown below in Table IV. Of these five glass-ceramic/filler materials, GC/F-4 and GC/F-5 were found to have the best overall properties for this purpose.

TABLE IV

	Composition (Weight %)	GC/F-1	GC/F-2	GC/F-3
		70 GC-7 + 15 Fluorspar + 15 Quartz	75 GC-8 + 25 Fluorspar	70 GC-9 + 15 Quartz + 15 Fluorspar
Expansion Coefficient ($10^{-7}/^{\circ}\text{C}$) (Rm.T.-600 $^{\circ}\text{C}$)		116	106	110
Dielectric Constant (@ 10 KHz)		6.4	5.6	6.5
Dissipation Factor (@ 10 KHz)		0.2%	0.2%	0.2%
	Composition (Weight %)	GC/F-4	GC/F-5	
		70 GC-12 + 15 Fluorspar + 15 Quartz	70 GC-13 + 15 Fluorspar + 15 Quartz	
Expansion Coefficient ($10^{-7}/^{\circ}\text{C}$) (Rm.T.-600 $^{\circ}\text{C}$)		115-120	120-125	



1	Dielectric Constant (@ 1 MHz)	6.2-6.6	6.3-6.9
5	Dissipation Factor (@ 10 KHz) (@ 1 MHz)	0.1% 0.3%	0.3% 0.5%
10	Peak Firing Temp. (°C)	930-935	910-920
	Moisture Resistance	Good	Good
15	HHBT (60°C, 90RH, 48V)	Pass	Pass
20	Volume Resistivity	>10 ¹² Ωcm	>10 ¹² Ωcm

A combined weight of up to 50% of the fillers Quartz, Fluorspar and/or Cristobalite can be incorporated for further elevation of the thermal expansion coefficient and improvement of the shrinkage behavior.

An example of microelectronic packaging of a multichip module is shown in Fig. 1. The co-fired ceramic-on-metal structure 10 comprises the metal base 12 having first and second major surfaces 14 and 16 with the co-fired, multi-layered ceramic 20 bonded to the first major surface 14 by the glass bonding layer 18. Each layer of the laminated glass-ceramic/filler tape, prior to firing, may be provided with suitable holes or vias, which, after firing, provide slots 22 in the co-fired, multi-layered, ceramic 20, thereby permitting integrated-circuit chips 24 (or other components) to be



1 attached directly to the metal base 12. An encapsulant
26, covering each of the chips 24, may then be
hermetically sealed to the metal base 12. The chips 24
are electrically attached, e.g., by wire bonding 28 or
5 similar means, as is known in the art. Alternatively,
each of the chips 24 may be protected by a non-hermetic
sealed encapsulant 26.

A heat sink 30 is attached to the opposite major
surface 16 of the base 12 by an adhesive 32. Further,
10 the microelectronic packaging includes support structure
34 for mounting the multichip module in a device (not
shown).

Although not shown in Fig. 1, co-fired,
multi-layered ceramic 20 incorporates metallic
15 conductors which currently comprise Ag and Ag/Pd.
However, metallic conductors comprising Cu or Au should
also be compatible with co-fired, multi-layered,
ceramic-on-metal boards of the type disclosed herein.

While the new glass-ceramic (GC) materials shown
20 in Table III and, particularly, the glass-ceramic/filler
materials shown in Table IV were developed for use in
the microelectronic packaging of a ceramic-on-metal
multichip module of the type shown in Fig. 1, these new
materials also should be useful for other standard
25 multi-layer ceramic packages, with or without the
incorporation of a metal-base.

The novel process, shown in Fig. 2, involves
applying the glass bonding layer 18 by, for example,
spray coating, to one major surface, for example, surface
30 14, of the base 12. A layer of SCC-11 glass that had
been made into a slurry, by mixing it with about 60 to
90 volume % of a suitable solvent, such as 2-propanol,
acetone, ethanol or terpinol, 2-propanol being
preferred, is used. The laminated ceramic layer 20 may
35 be formed separately by stacking multi-layers of
selectively metalized glass-ceramic/filler tape having
vias formed therein, and bisque firing the laminated
structure to remove the organics therefrom to form a



1 monolithic ceramic. Alternatively, the ceramic layer 20
may be formed by applying multiple layers of metalized
and via punched glass-ceramic/filler tape to the glass
bonding layer 18. In the preferred method, the glass
5 bonding layer 18 is heated to a temperature of about
450°C to pre-flow the glass of the bonding layer to
form a thin glass cover having a thickness of about
0.025mm (0.001 inch) on the surface 14. Then, the
10 previously formed ceramic layer 20 is positioned on the
glass bonding layer 18, and the entire structure is
co-fired in nitrogen (about 10,000 ppm O₂) at a
temperature of 900-930°C for about 2 to 20 minutes.
The peak firing temperatures selected for co-firing
15 depend upon the metal of the base 12 and the composition
of the ceramic layer 20. The adhesion of the ceramic
layer 20 to the base 12, resulting from the utilization
of the glass bonding layer 18, significantly minimizes
the x-y shrinkage of the ceramic layer during co-firing,
and the shrinkage in volume of the ceramic is mostly
20 confined to the z thickness dimension.



CLAIMS

1. A co-fired, multi-layered, ceramic-on-metal circuit board comprising a structure having a metal base, a bonding layer of glass on said base, and a ceramic formed from multiple layers of a ceramic tape on said bonding layer, each layer of said multiple layers of ceramic tape comprising a glass-ceramic/filler composition.
2. The circuit board defined in Claim 1, wherein:
- each of said metal and said glass-ceramic/filler composition exhibits a temperature coefficient of expansion that closely matches one another over a temperature range from room temperature to about 600°C.
3. The circuit board defined in Claim 1 or Claim 2 wherein said glass-ceramic/filler composition exhibits:
- a temperature coefficient of expansion in the range of $90-130 \times 10^{-7}/^{\circ}\text{C}$;
- a dielectric constant of less than 6.9 at 1 MHz; and
- a dissipation factor of not greater than 0.5% at 1 MHz.
4. The circuit board defined in any preceding claim, wherein:
- said glass-ceramic of said glass-ceramic/filler composition consists of a selected glass-ceramic of a $\text{MgO-B}_2\text{O}_3\text{-SiO}_2$ system of glass-ceramics.

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5. The circuit board defined in any preceding claim,
wherein:

5 said glass-ceramic/filler composition, by weight, consists of at least 50% glass-ceramic composition and a filler composition of no greater than 50%, and said filler composition comprises at least one of Quartz, Fluorspar or Cristobalite.

10 6. The circuit board defined in Claim 5,
wherein:

15 said glass-ceramic/filler composition, by weight, consists of substantially 70% of a given glass-ceramic composition and substantially 30% of a given filler composition;

said given glass-ceramic composition, by weight, consists of substantially 16.9% SiO_2 , 30.0% B_2O_3 , 39.2% MgO , 9.1% ZnO , 3.7% CaO , and 1.2% ZrO_2 ; and

20 said given filler composition, by weight, consists of substantially 50% Fluorspar and 50% Quartz.

25 7. The circuit board defined in Claim 5,
wherein:

30 said glass-ceramic/filler composition, by weight, consists of substantially 75% of a given glass-ceramic composition and substantially 25% of a given filler composition;

said given glass-ceramic composition, by weight, consists of substantially 15.9% SiO_2 , 28.3% B_2O_3 , 41.2% MgO , 9.23% ZnO , 4.2% CaO , and 1.2% ZrO_2 ; and

35 said given filler composition, by weight, consists of substantially 100% Fluorspar.





8. The circuit board defined in Claim 5,
wherein:

5 said glass-ceramic/filler composition, by weight, consists of substantially 70% of a given glass-ceramic composition and substantially 30% of a given filler composition;

said given glass-ceramic composition, by weight, consists of substantially 17.5% SiO_2 , 31.8% B_2O_3 , 43.0% MgO , 6.53% CaO , and 1.2% ZrO_2 ; and

10 said given filler composition, by weight, consists of substantially 50% Fluorspar and 50% Quartz.

9. The circuit board defined in Claim 5,
15 wherein:

said glass-ceramic/filler composition, by weight, consists of substantially 70% of a given glass-ceramic composition and substantially 30% of a given filler composition;

20 said given glass-ceramic composition, by weight, consists of substantially 16.8% SiO_2 , 29.8% B_2O_3 , 38.8% MgO , 9.1% ZnO , 3.6% CaO , 0.9% ZrO_2 , and 1.0% Cr_2O_3 ; and

25 said given filler composition, by weight, consists of substantially 50% Fluorspar and 50% Quartz.

10. The circuit board defined in Claim 5,
30 wherein:

said glass-ceramic/filler composition, by weight, consists of substantially 70% of a given glass-ceramic composition and substantially 30% of a given filler composition;

35 said glass-ceramic composition, by weight, consists of substantially 15.8% SiO_2 , 28.0% B_2O_3 , 34.4% MgO , 8.5% ZnO , 3.4% CaO , 8.0% BaO , 0.4% ZrO_2 , and 1.5% Cr_2O_3 ; and

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said given filler composition, by weight,
consists of substantially 50% Fluorspar and 50%
Quartz.

5 11. The circuit board defined in any preceding
claims, wherein:

said metal consists of one of Cu, Al,
stainless steel, Ni, low carbon steel, Cu/Invar/Cu,
Cu/Mo/Cu, and Cu/stainless steel/Cu.

10

12. The circuit board defined in any preceding
claim, wherein :

15 at least one of the layers of said co-
fired, multi-layered ceramic includes printed
conductors thereon comprising at least one of Ag, Au,
AuPt, Ag/Pd, Ni, and Cu.

20 13. The circuit board defined in any preceding
claims, wherein:

said multi-layered ceramic incorporates at
least one slot extending therethrough to the metal
underlying said slot.

25

14. The circuit board defined in Claim 13,
further comprising:

30 a microelectronic component extending into
said slot and attached directly to said underlying
metal.

35 15. The circuit board defined in Claim 14,
wherein:

said microelectronic component comprises an
integrated-circuit chip.

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16. The circuit board defined in Claim 14,
further comprising:

5 an encapsulant covering said
microelectronic component and said slot, said
encapsulant being attached to said multilayered
ceramic.

17. The circuit board defined in Claim 16,
10 wherein:

said microelectronic component is
hermetically sealed by said covering encapsulant.

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15 18. A composition comprising a selected
glass-ceramic of a $\text{MgO-B}_2\text{O}_3\text{-SiO}_2$ system of glass-
ceramics suitable for use in the fabrication of a co-
fired, multi-layered, ceramic circuit board; wherein:
said selected glass-ceramic by itself
20 exhibits a temperature coefficient of expansion in the
range of $85\text{-}105 \times 10^{-7}/^\circ\text{C}$ over a temperature range from
room temperature to about 600°C .

19. The composition defined in Claim 18,
25 wherein:

said selected glass-ceramic of said MgO-
 $\text{B}_2\text{O}_3\text{-SiO}_2$ system comprises at least one of ZnO , CaO ,
 BaO and SnO_2 as an additive.

30 20. The composition defined in Claim 18 or
Claim 19, wherein:

said selected glass-ceramic of said MgO-
 $\text{B}_2\text{O}_3\text{-SiO}_2$ system comprises, by weight, 10-20% SiO_2 ,
20-35% B_2O_3 , 25-50% MgO , 0-10% ZnO , 0-22% CaO , 0-18%
35 SnO_2 , and 0-10% BaO .

21. The composition defined in Claim 20,
wherein:



the composition of said selected glass-ceramic of said $\text{MgO-B}_2\text{O}_3\text{-SiO}_2$ system includes a nucleating agent for controlled crystallization of said composition, said nucleating agent comprising up to 5%, by weight, of ZrO_2 , TiO_2 or P_2O_5 , alone or in any combination thereof.

22. The composition defined in Claim 20, wherein:

10 the composition of said selected glass-ceramic of said $\text{MgO-B}_2\text{O}_3\text{-SiO}_2$ system includes up to 3%, by weight, of Cr_2O_3 , CoO , Fe_2O_3 , CuO , CeO_2 or Pr_2O_3 , alone or in any combination thereof for obtaining a suitable color for said composition.

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15 23. The composition defined in Claim 20, wherein:

20 the composition of said selected glass-ceramic of said $\text{MgO-B}_2\text{O}_3\text{-SiO}_2$ system includes as an additive up to 10%, by weight, of Li_2O , Na_2O , K_2O , or Al_2O_3 , PhO , Bi_2O_3 , or SrO alone or in any combination thereof.

24. The composition defined in any one of 25 Claims 18 to 23, wherein:

30 said composition further comprises a filler having a temperature coefficient of expansion sufficiently high to increase the temperature coefficient of expansion of said composition from said value in the range of $85\text{-}105 \times 10^{-7}/^\circ\text{C}$ of said selected glass-ceramic by itself to a value in the range of $90\text{-}130 \times 10^{-7}/^\circ\text{C}$ over a temperature range from room temperature to about 600°C .

35 25. The composition defined in Claim 24, wherein said composition exhibits:

a dielectric constant of less than 6.9 at 1 MHz; and



a dissipation factor of not greater than
0.5% at 1 MHz.

26. The composition defined in Claim 24 or
5 Claim 25, wherein:

said composition comprises up to 50%, by
weight, of said filler; and

said filler comprises at least one of
10 Quartz, Fluorspar or Cristobalite.

27. A method of making a co-fired,
ceramic-on-metal circuit board comprising a multi-
layered ceramic on a metal base, said metal base
15 having oppositely disposed major surfaces, said method
including the steps of

depositing a glass bonding layer on one of
said major surfaces of said metal base, said glass
bonding layer having a coefficient of thermal
20 expansion not greater than that of said base,

providing said multi-layered ceramic on
said glass bonding layer, and

heating said base, said glass bonding layer
and said multi-layered ceramic to a temperature
25 sufficient to securely attach said ceramic to said
base.

28. The method as described in claim 27,
wherein said glass bonding layer is heated to a
30 temperature of about 450°C, to pre-flow the glass of
the bonding layer, prior to providing said multi-
layered ceramic thereon.

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29. The method as described in claim 27, wherein said heating step is carried out at a temperature of about 900°C.

5 30. The method as described in claim 29, wherein said heating step is carried out in a nitrogen atmosphere.

31. A method of minimizing lateral shrinkage
10 in a co-fired, ceramic-on-metal circuit board comprising a multi-layered ceramic on a metal base, said metal base having oppositely disposed major surfaces, said method including the steps of

15 depositing a glass bonding layer on one of said major surfaces of said metal base, said glass bonding layer having a coefficient of thermal expansion not greater than that of said base,

20 providing said multi-layered ceramic on said glass bonding layer, each layer of said multi-layered ceramic comprising a glass-ceramic/filler composition having a coefficient of thermal expansion that closely matches that of said base and said glass bonding layer over a temperature range from room temperature to about 600°C, and

25 co-firing said base, said glass bonding layer and said multi-layered ceramic to an elevated temperature sufficient to securely attach said ceramic to said base, said glass bonding layer having a softening point below that of said ceramic so that said
30 glass of said bonding layer flows and bonds to the metal while minimizing the lateral shrinkage of said ceramic.

32. The method as described in claim 31, wherein said glass bonding layer is heated to a
35 temperature of about 450°C to pre-flow said glass of said glass bonding layer, prior to providing said multi-layered ceramic thereon.





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33. The method as described in claim 31,
wherein said co-firing step is carried out at a
temperature of about 900° to 930°C for about 2 to 20
minutes, in a nitrogen atmosphere.

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