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IR-1113

PROCESS FOR MANUFACTURE OF MOS GATED DEVICE WITH REDUCED MASK COUNT

BACKGROUND OF THE INVENTION

This invention relates to a process for the manufacture of a power MOS gated device, and more specifically relates to a novel process for the manufacture of such devices by a process using a reduced mask count and only one critical alignment step.

MOS gated devices are well known in the art and include such devices as power MOSFETs such as the power MOSFET shown in U.S. Patent 5,008,725, as well as power IGBTs such as the power IGBT shown in application Serial No. 07/521,177, filed May 9, 1990 (now abandoned) and in its continuation application Serial No. 08/041,136 filed March 30, 1993 (now refiled as application Serial No. 08/316,112 on September 30, 1994), the subject matter of which is incorporated herein by reference. MOS gated devices also include MOS gated thyristors, gate turn-off devices and the like.

The manufacturing process for such devices includes a number of photolithographic masking steps and critical mask alignment steps which each require additional manufacturing time and expense and which each produce possible sources of device defects. Reducing the number of masks and alignment steps necessary for the manufacture of such a device is desirable and improves the manufacturing yield and reduces the manufacturing cost.

U.S. Patent 5,302,537 discloses a process for the manufacture of a power MOSFET in which a hole is

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formed through the center of a source region and into an underlying base region. Metallizing enters the hole to connect together the source and base. However, these regions are connected only at the peripheral regions which are the walls of the hole. Thus, a low resistance, reliable contact between the source and base is difficult to form in a mass production process.

The present invention provides a novel manufacturing process which reduces the number of masks needed for the manufacture of a MOS gated power device to three.

SUMMARY OF THE INVENTION

In accordance with the present invention, and for an N channel device, a first mask defines the P-type body of each of the cells of the device, as well as a source region disposed within that P-type body region. Note that the device topology can be interdigitated as well as cellular. It is also to be noted that the body region is sometimes referred to as the channel region of the MOSFET cell. A second mask is then employed which is aligned with a small central area above the N^+ regions of each of the cells or strips of the device and an anisotropic oxide etch forms openings in the oxide layer covering the device which reach the surface of the silicon. An anisotropic silicon etch follows which causes a shallow hole in the surface of the silicon centered on the N^+ regions. The hole is deep enough to cut through the N^+ regions and reach the underlying P-type channels or body regions. The alignment of the second mask, which is the contact mask, is the only critical alignment in the process.

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This anisotropic silicon etch is then followed by an isotropic etch which undercuts the gate oxide and protective low temperature oxide above the gate oxide, thereby to expose shoulders at the silicon surface of the chip, which surround the etched openings into the N^+ cell regions.

Thereafter, a conductive layer, which may be metal, is deposited over the surface of the chip (or wafer in which a plurality of such chips are contained) and the metal fills the holes through the N^+ region, thereby contacting the underlying P body regions, and also overlaps the shoulders surrounding the N^+ source regions at the silicon surface. Consequently, a good contact is made to the N^+ source and to the underlying P region. Note that this contact between the P^+ underlying body region and the N^+ source region is desirable in order to short circuit the parasitic NPN transistor which inherently appears in each cell structure of a MOS gated device. A third mask is used to pattern the metal, followed by a sinter and backside metallization. Thus, the manufacturing process is reduced to only three mask steps, with only one critical alignment at the contact mask.

In an alternative process, in order to improve step coverage of the contact metal over the underlying gate oxide and low temperature oxide, the silicon etch step described above uses a photoresist shadow mask. First, the low temperature oxide and gate oxide area isotropically etched to expose an area of the silicon surface larger than the photoresist opening. This etch will leave a somewhat tapered oxide sidewall. Next, an anisotropic plasma etch using the photoresist as a shadow

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mask is carried out by a CL_2 plasma etch of well-known variety. This process will etch a hole through the N^+ source down to the P+ base, with the same area as the photoresist opening. Thus, a portion of the original N^+ surface remains exposed to receive the aluminum contact metal.

In order to complete the device, it is necessary to provide contact between the gate metal and gate polysilicon electrodes. This is accomplished in the same mask step as the contact to the source and body regions. This means that a hole will be etched in the polysilicon simultaneously with the hole in the silicon. It is necessary, therefore, to control the silicon etch depth such that the P^+ body region is exposed, but a portion of the polysilicon layer remains.

It is also necessary to provide an edge structure capable of withstanding the desired blocking voltage. A preferred edge structure can use a series of polysilicon rings and spaces. By shorting each polysilicon ring to the diffusions in the adjacent space on the active area side, such a structure can be obtained.

Another important feature of the invention is accomplished by implanting the heavy body implant into the same window as the source and deeper than the source. This allows the source to be almost completely surrounded by a heavily doped body region. This prevents punch-through breakdown and drain-source leakage as well, and also provides an extremely low resistance path in the body from the edge of each cell to the contact area in the center. The diffusion parameters can be adjusted in order to leave only a small, lightly doped body region

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immediately adjacent to the surface which forms the inversion channel.

As a further embodiment of the invention, the body region can be formed with a single implant and drive by implanting the body region to a first depth about as deep or deeper than the source and thereafter implanting the source region to a shallower depth. Both implants are carried out through the same mask window. These two regions are thereafter annealed and thus driven, with the body region annealed for three hours at about 975°C to obtain a depth of about 1-2 microns, whereas the source region is annealed for about one hour at 975°C to reach a depth of only about 0.3 microns. Thus, a complete cell can be formed employing only two implants. Thereafter, the manufacturing process can be completed as has been previously described.

In a further embodiment, a heavy base contact implant is carried out through the contact window instead of the polysilicon window. This is done after the hole has been etched in the silicon to expose the body region, and before metal is deposited on the wafer. Remarkably, no anneal is required after implant prior to metallization to achieve low contact resistance between metal and body regions. This is because a sinter of about 420°C is sufficient to activate enough dopant, and this temperature is low enough to be tolerated after the metal is deposited.

Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross sectional view of a portion of a chip within a wafer of silicon after an oxide layer, polysilicon layer and photoresist layer have been formed thereon.

Fig. 2 is a view of a device or structure of Fig. 1 after a first mask step has been carried out to produce a plurality of slots or openings of a symmetric arrangement in the photoresist layer.

Fig. 3 shows the structure of Fig. 2 showing the removal of the polysilicon and gate oxide regions which are exposed by the openings in the photoresist layer.

Fig. 4 shows the structure of Fig. 3 following an implant step for implanting a P^+ region through the windows in the polysilicon.

Fig. 5 shows the structure of Fig. 4 after the photoresist has been stripped and the P^+ implant has been driven to form a more lightly doped deep P region.

Fig. 6 is similar to Fig. 5 but shows the implant of P^+ and N^+ layers by implantation through the mask openings defined by the polysilicon gate.

Fig. 7 shows the structure of Fig. 6 following the deposition of a low temperature oxide over the surface of the device and following a drive for driving in the P^+ and N^+ implanted regions of Fig. 6.

Fig. 8 shows the structure of Fig. 7 following a second mask step which opens a central opening above each of the N^+ regions in the wafer and following an anisotropic etch of the underlying low temperature oxide and polysilicon to the surface of the silicon wafer.

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Fig. 9 shows the structure of Fig. 8 following an anisotropic silicon etch to form a depression cutting through the N^+ layers, followed by an isotropic oxide etch which undercuts the LTO and gate oxides.

Fig. 10 shows the structure of Fig. 9 following the stripping of the photoresist and the deposition of a source metal such as aluminum.

Fig. 11 shows a process modification which can be employed to improve step coverage wherein, following the step of Fig. 8, there is an isotropic etch of the low temperature oxide.

Fig. 12 shows the structure of Fig. 10 following the step whereby a silicon etch is carried out using the photoresist as a shadow mask.

Fig. 13 shows the structure of Fig. 12 following the stripping of the photoresist and the metallizing of the structure with improved step coverage.

Fig. 14 shows an improvement for the process wherein, following the step of Fig. 3, an N^+ implant and a P^+ implant are formed through the openings formed by the first mask.

Fig. 15 shows the structure of Fig. 14 following junction anneals which form cells or strips having P^+ bodies and N^+ source regions, with the structure being completed by the steps previously described.

Fig. 16 shows a further embodiment of the invention in which the P^+ diffusion is formed through the contact mask.

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DETAILED DESCRIPTION OF THE DRAWINGS

The following description of the preferred embodiments of the invention describes the manufacture of an N channel power MOSFET device. However, any suitable junction modification can be employed to use the same reduced mask count process for the manufacture of any MOS gated device such as an IGBT or a MOS gated thyristor whether N channel or P channel. A specific topology is not expressly shown in these drawings, but it is noted that the topology to be used is preferably that of hexagonal cells, such those shown in Patent 5,008,725. However, it will be apparent to those skilled in the art that the process is equally applicable to structures having any polygonal structure such as square or rectangular cells, whether offset or in line, as well as to interdigitated structures. It should be further noted that the termination structure of the device is not shown, but the terminations commonly used for any MOS gated device can also be used here.

Referring first to Fig. 1, there is shown only a very small portion of a wafer or chip which has a repetitive structure, only a few elements of which are shown in cross section. The wafer may be of any desired size and will be diced into a plurality of chips. In the description of the preferred embodiments of the invention herein, the terms "chip" and "wafer" are sometimes interchanged.

Fig. 1 shows a wafer having an N^- body 30 with monocrystalline silicon. The N^- body 30 may be an epitaxially formed layer atop an N^+ substrate (not shown). A drain (or anode) contact may be connected to the N^+ substrate and may be available for connection at

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either surface of the chip. The epitaxially formed body will have a thickness and resistivity depending upon the breakdown voltage of the ultimately formed device.

The first step in the process of the invention is the formation of an insulation layer 31 atop the silicon 30 where the layer 31 can be thermally grown silicon dioxide having a thickness of from 200 to 1,500 angstroms depending upon the desired threshold voltage of the subsequently formed device. The oxide layer 31 is then covered, in turn, by a layer of polysilicon 32 which may have a thickness, for example, of 7,500 angstroms and is formed in any desired manner. Preferably, the polysilicon is doped heavily with implanted arsenic or with a subsequent CVD doping step. A suitable photoresist layer 33 is then formed atop the polysilicon layer 32.

As shown next in Fig. 2, the photoresist 32 has been patterned by an appropriate photolithographic mask step and openings 34 and 35 are formed through the photoresist to the surface of the polysilicon layer 32. If a cellular topology is chosen, each of openings 34 and 35 may be one of many thousands of identical symmetrical openings which have any desired polygonal configuration such as that of a hexagon or square which would have a dimension from side to side of about 5-10 microns and a spacing center to center which depends on voltage and photolithography capability. Note, however, that the openings 34 and 35 could also be parallel elongated strips if the topology chosen is an interdigitated topology.

Following the formation of openings in the photoresist layer 33 in Fig. 2, an anisotropic etch is employed to etch the exposed polysilicon, as shown in

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Fig. 3. Preferably, the anisotropic polysilicon etch should not undercut the photoresist because the area of the subsequent implant should preferably be defined by the polysilicon, not the photoresist. The etch is selective enough to stop prior to removal of gate oxide anywhere on the wafer. The polysilicon sidewall should also be as nearly vertical as possible, which is important to accurately define the deep body implant region.

Thereafter, the underlying exposed silicon dioxide may be removed, if desired, with an isotropic wet etch. The anisotropic and isotropic etches to be used are those which are well known to those of ordinary skill and any etch can be selected for these non-critical steps. Note, however, that it is also possible at this step in the process to leave the gate oxide intact and to do subsequent implant processes with sufficiently high energy to penetrate that thin gate oxide.

Thereafter, and as shown in Fig. 4, an implant is carried out employing boron as the implant species having a dose of 3-8E13 at an energy of about 80 kV. This implant forms P type regions 40 and 41 beneath the bottom of the exposed openings in the photoresist 33 and oxide 31.

Following this implant operation and as shown in Fig. 5, the photoresist 33 is stripped and the P^+ implants 40 and 41 are driven at 1175°C for about 30-60 minutes to reach a depth of from 1.0 - 2.0 microns. Other implant energies and diffusion times and depths could be selected by the designer depending upon the type device he wishes to form.

In the next process step, shown in Fig. 6, a relatively high N^+ dose of arsenic or phosphorus, for

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example, 1E16, is implanted through the windows 34 and 35 at an implant energy of about 120 kEV. A diffusion step can follow. For example, if arsenic is the species used, it can be driven at 975°C for about one hour. A thin oxide (not shown) is grown during this time on the polysilicon sidewalls to encapsulate the polysilicon prior to the deposition of a low temperature oxide. Thereafter, P^+ boron is implanted through windows 34 and 35 at a dose of about 1E15 and implant energy of from 80 to 120 kEV. The N^+ layer 50 will be shallower than the P^+ layer 51 by an amount selected by the designer and determined by the species and doses used.

Thereafter, and as shown in Fig. 7, a layer 60 of low temperature oxide ("LTO") is deposited atop the surface of the wafer of Fig. 6 to a thickness of from 0.6 to 0.8 microns. The LTO deposition conditions employ a silane decomposition reaction with oxygen at about 425°, thus forming the LTO layer 60. The thickness is selected to minimize gate-source overlap capacitance and shorts, while allowing convenient patterning and good step coverage.

After the deposition of the LTO layer 60, the N^+ and P^+ regions 50 and 51 are driven at a temperature of about 975° for about 30 minutes. These junctions then drive to depths of about 0.3 microns for the N^+ region and 1 micron for the P^+ region. By doing the drive after the deposition of the LTO layer 60, the LTO layer will also densify under the drive conditions.

It will be noted that this operation has produced annular channel regions 55 and 56 for the two cells which are shown. These channel regions underlie respective segments of the polysilicon layer 32, which

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defines the polysilicon gate for each cell, and are invertible upon the connection of a gate potential to the polysilicon layer 32. The polysilicon layer 32 will have a lattice configuration between the cells if the cells are of a polygonal structure. This lattice will, at its sides or edges, overlie the underlying channel regions within the cells.

Proper selection of diffusion parameters will prevent the P^+ dopant from reaching the surface channel regions in sufficient quantity to substantially change the threshold voltage. The process can be designed, with careful controls, to allow the P^+ to contribute in part to the peak channel doping. This provides the best punch-through protection and the opportunity for the shortest channel. This requires very careful control of polysilicon sidewall profile as nearly vertical as possible.

Thereafter, and as shown in Fig. 8, a new photoresist layer 70 is applied atop the LTO layer 60 and the photoresist layer 70 is patterned by a second, and contact mask step, to form well aligned small central openings which are located at the axis of each of the individual cells, or along the length of strips if an interdigitated geometry is used. This is the only critical alignment step in the novel process. If a cellular structure is used, the openings in the photoresist 70 have a diameter of about 1.5-2 microns. This dimension depends on the photolithography process and metal-silicon contact system. After the formation of the openings in the photoresist, the LTO layer is etched by an anisotropic oxide etch to open a central opening which reaches the silicon surface.

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Thereafter, and as shown in Fig. 9, an anisotropic etch is carried out which etches the exposed silicon surface so that holes are formed in the silicon surface which penetrate the N^+ layers 51 and reach the P^+ layer 50 for each cell. Thus, by using a chlorine chemistry anisotropic plasma etch, about 0.4 microns of silicon are removed at the surface, forming the depressions or openings 80 and 81 in the centers of the cells formed by regions 40 and 41.

Thereafter, and as is also shown in Fig. 9, the silicon wafer is exposed to an isotropic wet etch which acts to undercut the LTO back to diameters 82 and 83. This action exposes, for a hexagonal or polygonal cell, a shoulder of the surface of the silicon chip which extends around openings 80 and 81.

In a preferred embodiment of the invention, the wet etch forming the undercut in the LTO and gate oxide is a wet 6 to 1 buffered oxide etch for 2-5 minutes. This creates a shoulder of about .2-.5 microns in width, which is sufficient to make a low resistance contact to the source region.

Thereafter, and as seen in Fig. 10, the photoresist 70 is stripped and a source metal 84, for example, aluminum is deposited over the full surface of the device. The aluminum will fill in the openings 80 and 81 and will overlie the exposed silicon shoulders formed by the undercuts 82 and 83 in Figs. 9 and 10. Thus the source metal 84 automatically connects the underlying P region 50 to the N^+ region 51 to make the intentional short between the P and N regions in each cell.

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The structure shown in Fig. 10 produces a complete MOSFET cellular configuration (or interdigitated configuration, if that is chosen) and the remaining steps in the processing of the device will include the usual non-critical mask for patterning gate and source electrode connection regions, and an optional mask for opening windows in an insulating scratch layer or the like. The basic process steps not counting the scratch mask required only three masks for the production of the MOS gated device with only one critical alignment.

It is to be also noted that, to complete the device of Fig. 10, a drain contact is needed. This drain contact can go onto the bottom of the wafer in the usual manner or can, if desired, be placed on the top of the wafer and connected to the common conduction regions between the cells 40 and 41 by sinkers and buried layers or the like as disclosed in Patent 5,191,396. Note also that, if the device is to be made into an IGBT, the usual thin N^+ buffer layer and P^+ bottom layer would be added to the bottom of the wafer structure in the conventional manner.

Fig. 11 shows a second embodiment of the process of the invention wherein, following the step of Fig. 8, the LTO is etched by an isotropic etch to form the radius curve 90 for the walls of the openings. This etch can be carried out with a 6 to 1 buffered oxide etch for about 8 minutes. The lateral dimension of the undercut of the curve will be about 0.5 micron at the bottom and about 1 micron at the top of the LTO layer.

Thereafter, as shown in Fig. 12, the overhanging portion of the photoresist layer, which has been undercut by the earlier isotropic etch, is used as a shadow mask in an anisotropic plasma etch process using a

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chlorine plasma. This anisotropic plasma etch will form a central opening 95 in the cell which may have a depth of 0.4 microns but is deep enough to reach and cut into the P^+ region 50.

The gradual curve 90 in the LTO layer 60 and the reduced diameter opening 95 in the silicon provides a smoother surface over which the aluminum electrode can later be formed. Thus, it is well known that aluminum does not cover sharp angles well, and it is preferred to have surfaces with a gradual curvature to improve aluminum step coverage. That is precisely the effect created by the process step shown in Fig. 12.

As shown in Fig. 13, the photoresist 70 is stripped and an aluminum contact layer 98 is deposited over the surface and more easily follows the gradual curve 90 in the LTO to provide better step coverage for the aluminum electrode. Note that the aluminum electrode also automatically makes contact between the P^+ region 50 and the N^+ region 51, thus accomplishing the desired short of these two layers at their center.

Figs. 14 and 15 show a still further embodiment of the invention wherein, following the step of Fig. 3, the junctions used to produce the ultimate cells or interdigitated regions are formed by the two implants which are a first boron implant of 3E14 at 120 kV forming the P^+ regions 100 and 101 in openings 34 and 35 in the oxide 31. The photoresist is removed, and the region is then annealed for about one hour at 1050°C. Then an implant of arsenic or phosphorus at 1E16 at 120 kV forms the layers 102 and 103 in the openings 34 and 35, respectively. Following the implant, the photoresist layer is removed, and an LTO layer 120 is deposited and

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the source implant is annealed for about one hour at 975°C. This steps drives the P^+ region 110 to about 1.4 microns and the N^+ region 111 to about 0.3 microns.

Thereafter, the wafer containing the two junctions will be processed as described previously. It will be noted that the P^+ region in the channel region at the surface of the device can have a relatively low P type concentration if properly controlled and thus can be an easily invertible channel area.

Referring next to Fig. 16, there is shown a further embodiment of the invention wherein the device is processed as shown in Fig. 9, but the P^+ region 51 is not formed through the polysilicon windows 34 and 35. Instead, in Fig. 16, the heavily doped P^+ contact regions 120 and 121 are formed through the contact mask after the holes 80 and 81 have been etched to expose the surfaces of body regions 40 and 41. The structure is then processed as described in Figs. 10 to 13. Unexpectedly, no anneal is needed following the implants of regions 120 and 121. This is because the subsequent sinter of the metal 84 (Fig. 10) after its deposition at about 420°C is sufficient to activate enough dopant, and the temperature is low enough to be tolerated after metal is deposited as in Fig. 10.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

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WHAT IS CLAIMED IS:

1. A process for the manufacture of a MOS gated semiconductor device; said process comprising the steps of forming a layer of gate insulation material atop a silicon substrate, forming a layer of polysilicon atop said layer of gate insulation material, forming a first photoresist layer atop said layer of polysilicon, forming a plurality of spaced openings in said first photoresist layer through the use of a first photolithographic masking step to expose portions of said layer of polysilicon; etching the portions of said layer of polysilicon which are exposed through said plurality of spaced openings in said photoresist layer to expose corresponding surface regions of the surface of said silicon substrate; diffusing impurities of a first conductivity type into said surface regions of said silicon substrate to form first diffused regions; diffusing impurities of a second conductivity type into said surface regions of the surface of said silicon substrate to form second diffused regions wherein said second diffused regions at each of said surface regions of said silicon substrate have a final depth and lateral extent which is less than that of said first diffused regions; thereafter depositing a second insulation layer over the upper surface of said device, forming a second photoresist layer atop said second insulation layer, forming, by a second photolithographic step which is aligned with said first masking step, a plurality of central openings in said second photoresist layer which are centrally aligned with respective ones of said plurality of spaced openings which were formed in said first photolithographic masking step; said central openings each having a lateral extent which is less than

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the lateral extent of said respective second diffused regions and having side walls which are perpendicular to the plane of the surface of said silicon substrate; etching away the portions of said second insulation layer which are exposed by said central openings to expose respective corresponding underlying second surface regions of said silicon substrate; etching depressions in the second surface regions of said silicon substrate to a depth greater than the depth of said second diffused regions, etching to form undercut portions in said second insulation layer surrounding said second surface regions of said silicon substrate to expose portions of the surface of said substrate which are adjacent said undercut portions of said surface at said silicon substrate, and thereafter depositing a conductive layer over the surface whereby said conductive layer contacts both said first diffused regions at the bottom of said depressions, and said second diffused regions at the upper portions of said undercut portions and the surrounding surfaces of said undercut portions; said first diffused regions being relatively highly doped and closely surrounding respective ones of said second diffused regions to reduce punch-through breakdown and drain to source leakage and to provide a low resistance current carrying path beneath said second diffused regions.

2. The process of claims 1 wherein said thin layer of gate insulation material is silicon dioxide.

3. The process of claim 1 wherein said plurality of spaced openings in said photoresist layer have identical shapes.

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4. The process of claim 3 wherein said plurality of spaced openings are selected from the group consisting of closed polygons and elongated strips.

5. The process of claim 1 wherein said first and second diffused regions are formed by the steps of implanting impurity atoms and then heating said substrate to diffuse said impurity atoms into said substrate.

6. The process of claim 1 wherein said second insulation layer is a low temperature oxide.

7. The process of claim 1 wherein said depressions in the second surface regions are formed by an anisotropic etch, and said undercut portions in said second insulation layer are formed by an isotropic etch.

8. The process of claim 1 wherein said conductive layer is a main electrode layer for the device being formed.

9. The process of claim 1 wherein said undercut portions in said second insulation layer are formed by an isotropic etch which etches curved walls in said undercut portions of said second insulation layer to define overhanging shadow-mask lips in said second photoresist layer which border said depressions, and wherein said etch of the exposed second surface regions is an anisotropic silicon etch using said overhanging shadow mask lips as a shadow mask thereby to reduce sharp edges on the surface of said silicon substrate and to

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improve the subsequent formation of said conductive layer.

10. The process of claim 9 wherein said plurality of spaced openings in said photoresist layer have identical shapes.

11. The process of claim 10 wherein said plurality of spaced openings are selected from the group consisting of closed polygons and elongated strips.

12. The process of claim 9 wherein said second insulation layer is a low temperature oxide.

13. The process of claim 9 wherein said conductive layer is a main electrode layer for the device being formed.

14. The process of claim 1 which includes the step of forming diffused regions of impurities of said first conductivity type which are deeper and wider and which have a lower concentration than that of said first and second diffused regions.

15. The process of claim 9 which includes the step of forming diffused regions of impurities of said first conductivity type which are deeper and wider and which have a lower concentration than that of said first and second diffused regions.

16. The process of claim 1 wherein the areas of said second insulation layer which underlie said central openings are etched by an anisotropic etch which

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does not undercut said second insulation layer beneath said first photoresist layer to leave the side of said central openings as vertical as possible.

17. The process of claim 6 wherein, following the formation of said low temperature oxide, said substrate is heated to simultaneously drive said first and second diffused regions and to densify said low temperature oxide layer.

18. A process for the manufacture of a MOS gated semiconductor device; said process comprising the steps of forming a layer of gate insulation material atop a silicon substrate, forming a layer of polysilicon atop said layer of gate insulation material, forming a first photoresist layer atop said layer of polysilicon, forming a plurality of spaced openings in said first photoresist layer through the use of a first photolithographic masking step to expose portions of said layer of polysilicon; etching the portions of said layer of polysilicon and of said layer of gate insulation material which are exposed through spaced openings in said first photoresist layer to expose corresponding surface regions of the surface of said silicon substrate; said spaced openings having side walls which are perpendicular to the plane of the surface of said silicon substrate; diffusing impurities of a first conductivity type into said surface regions of said silicon substrate to form first diffused regions; diffusing impurities of a second conductivity type into said surface regions of the surface of said silicon substrate to form second diffused regions wherein said second diffused regions at each of said surface regions of said silicon substrate have a final depth and

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lateral extent which is less than that of said first diffused regions; said first diffused regions being relatively heavily doped and closely surrounding respective ones of said second diffused regions.

19. The device of claim 1 which further includes the diffusion of a third region of impurities of said first type into said exposed surface regions prior to the diffusion of said first diffused regions; said third diffused regions defining channel regions of lower concentration than that of said first diffused regions.

20. The device of claim 1 which further includes the diffusion of a third region of impurities of said first conductivity type into said surface regions prior to the diffusion of said first diffused regions; said third diffused regions defining channel regions of lower concentration than that of said first diffused regions.

21. The process of claim 1 which includes the further step of diffusing impurities of the first conductivity type into said silicon substrate exposed by the etching of said second surface regions; said impurities which are diffused during said further step forming third regions of said first conductivity type which are more heavily doped than said first diffused regions.

22. The process of claim 19 which further includes the step of sintering said conductive layer at a temperature of less than about 450°C, thereby to anneal said third diffused regions.

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23. A MOS gated semiconductor device; said device comprising a wafer of monocrystalline silicon having at least one flat surface having a first conductivity; a plurality of spaced cells symmetrically distributed over and formed into said one flat surface; each of said cells having an identical structure, including a first region of a second conductivity type and having a first depth and a first lateral extent and extending from said first surface and into the body of said wafer, a second region of said first conductivity type formed at least partly within said first region and extending from said first surface; said second region being laterally spaced from said first region at at least portions of their coextensive lengths on said first surface, a gate insulation layer overlying at least the area on said first surface formed between the laterally spaced first and second regions, a gate electrode overlying said gate insulation layer; characterized in that a laterally central depression is etched into each cell, extending from said first surface, through said second region and into said first region; and a contact layer extending over said first surface and into each of said central depressions, thereby to electrically connect together said first and second regions.

24. The process of claim 1 wherein said layer of gate insulation material is etched during the step of etching the portions of said layer of polysilicon.

FIG. 1

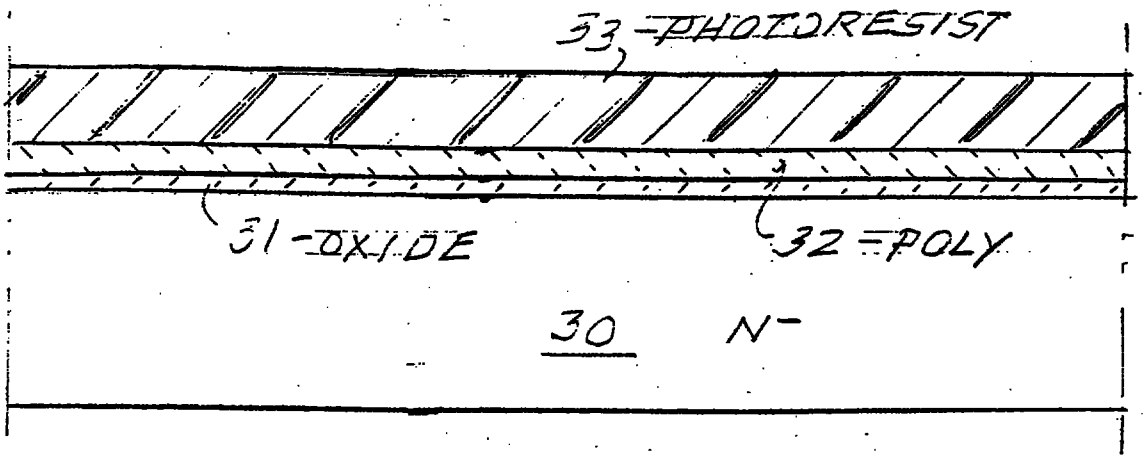

FIG. 2

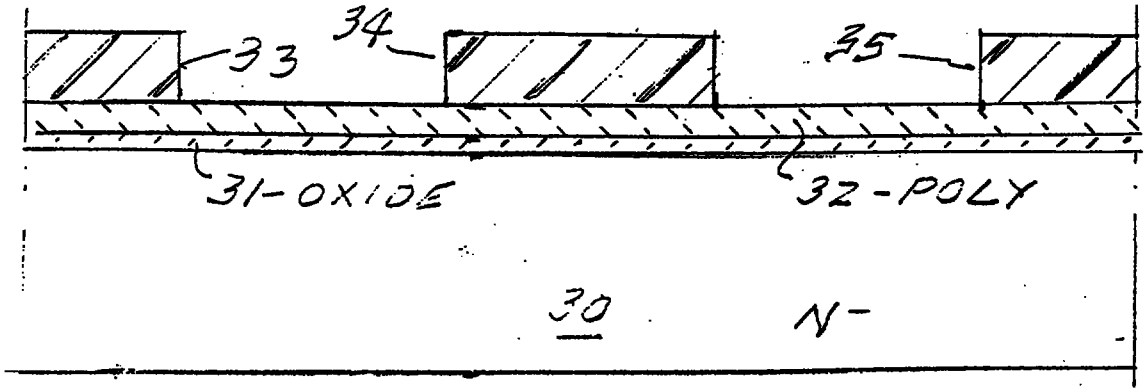

FIG. 3

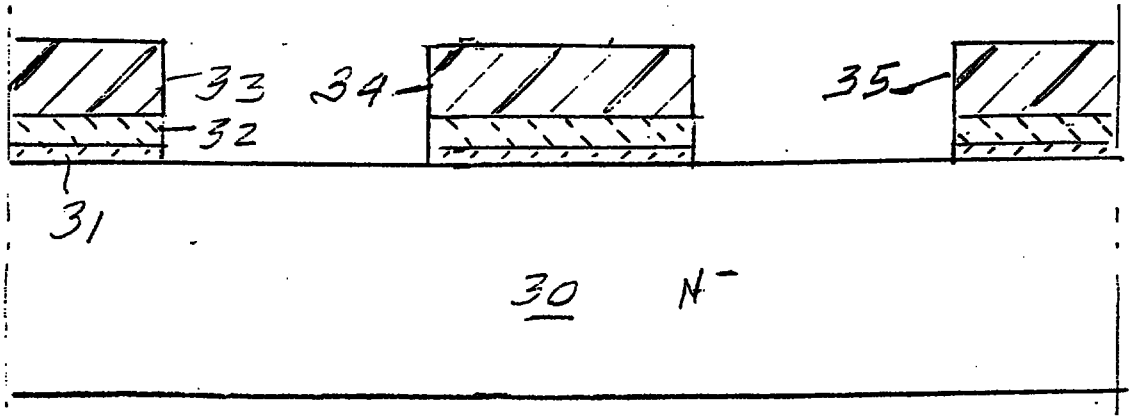

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FIG. 4

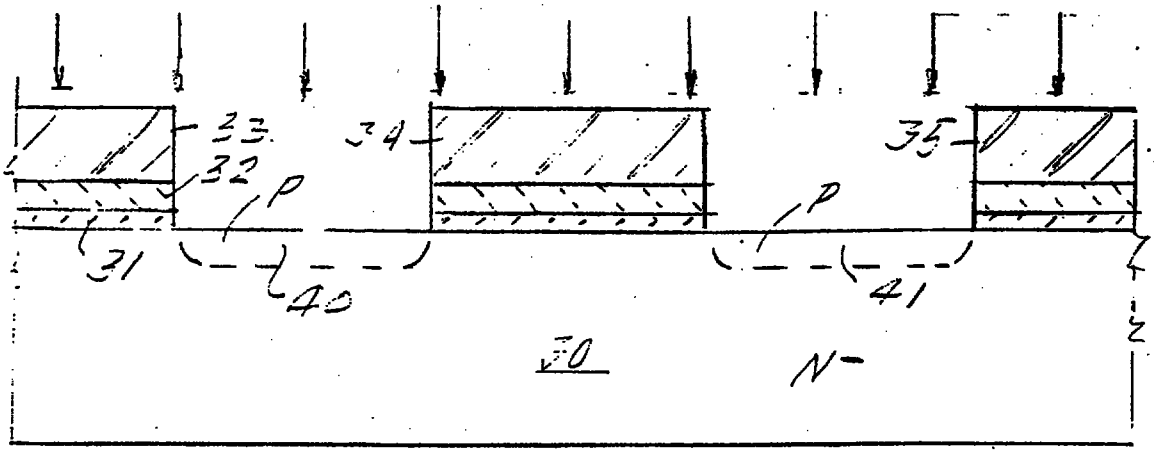

FIG. 5

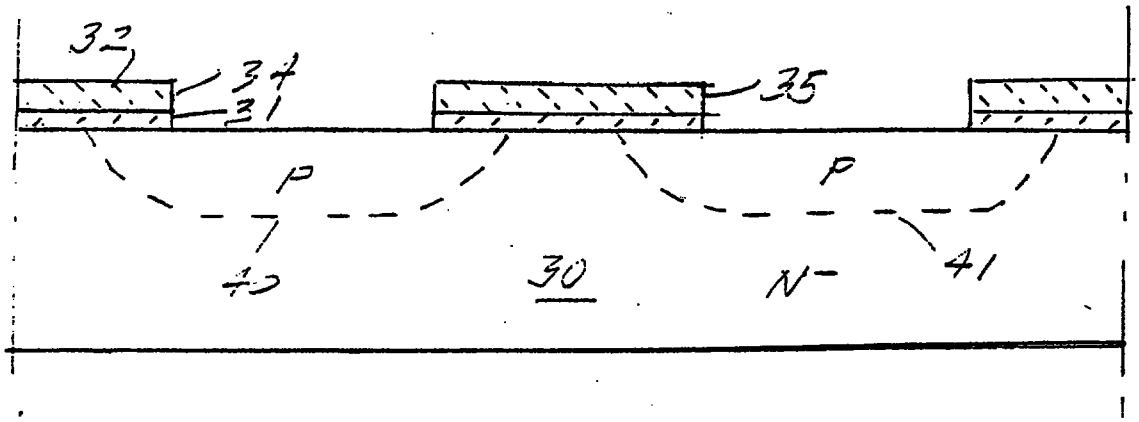

FIG. 6

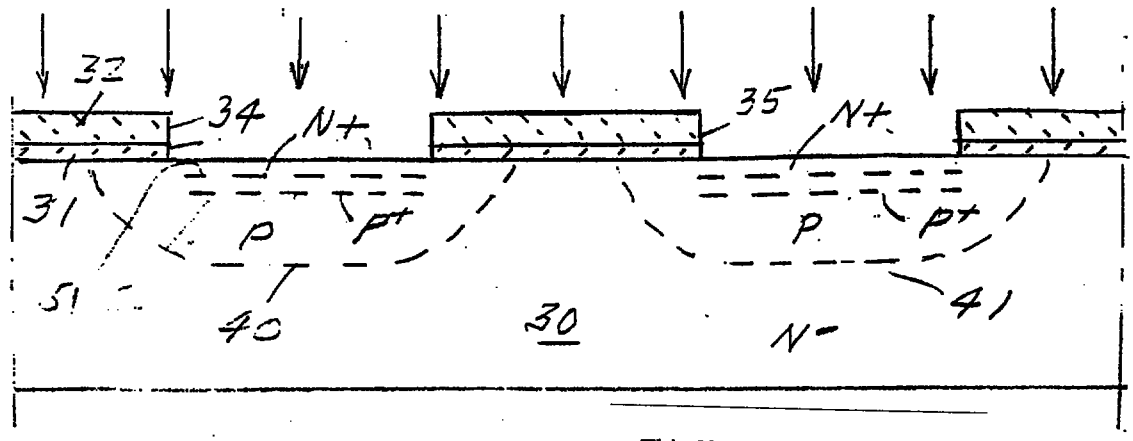

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FIG. 7

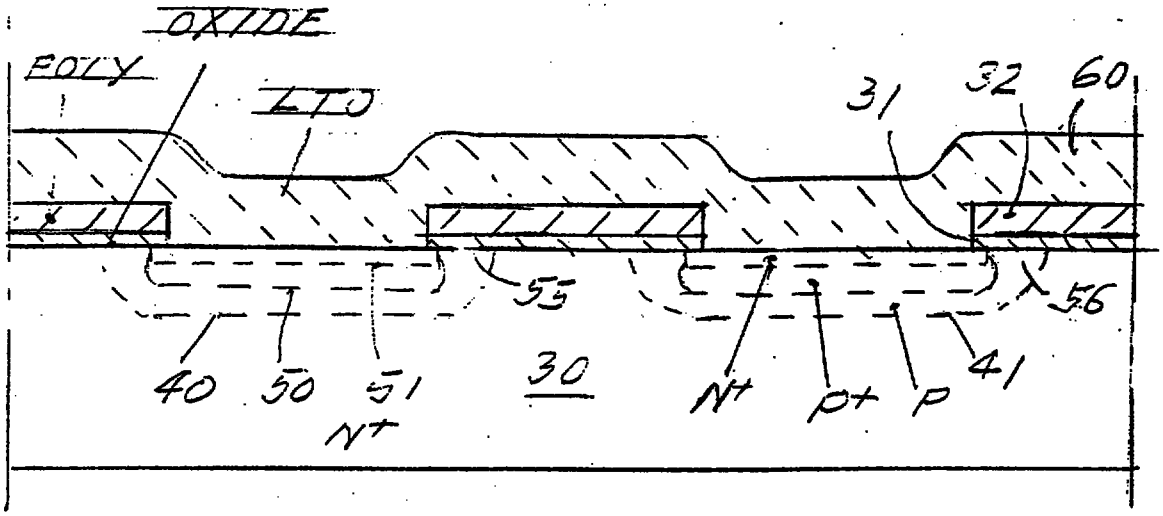

FIG. 8

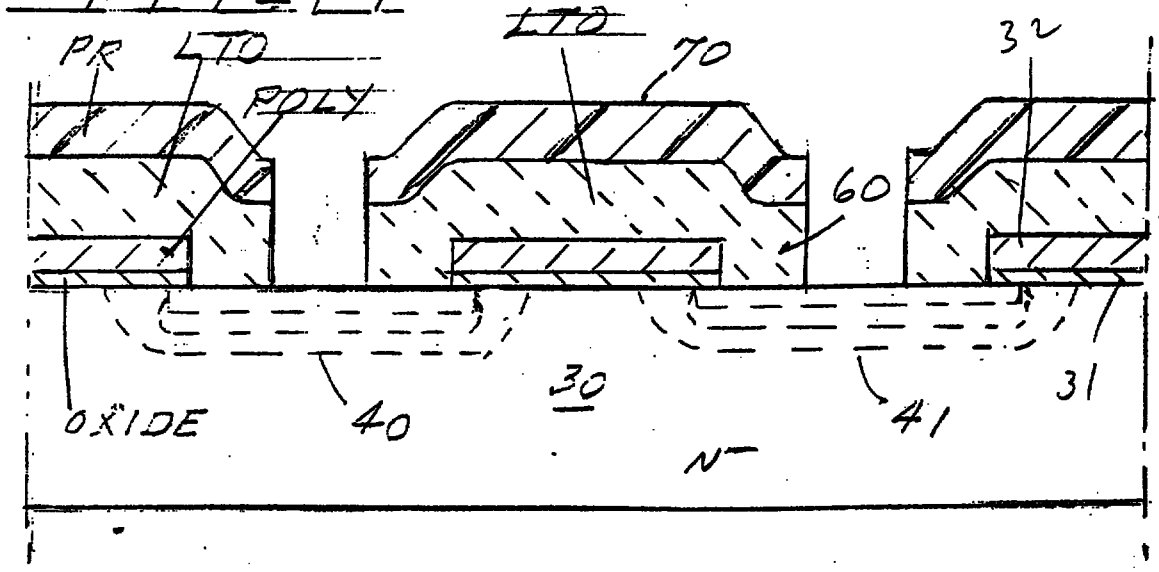

FIG. 9

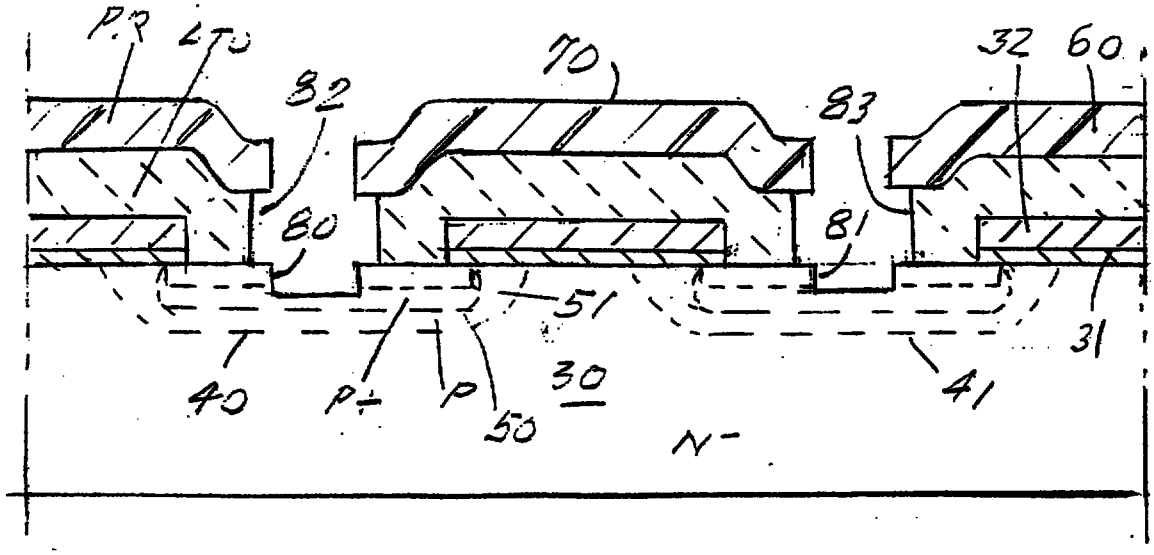

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FIG. 10.

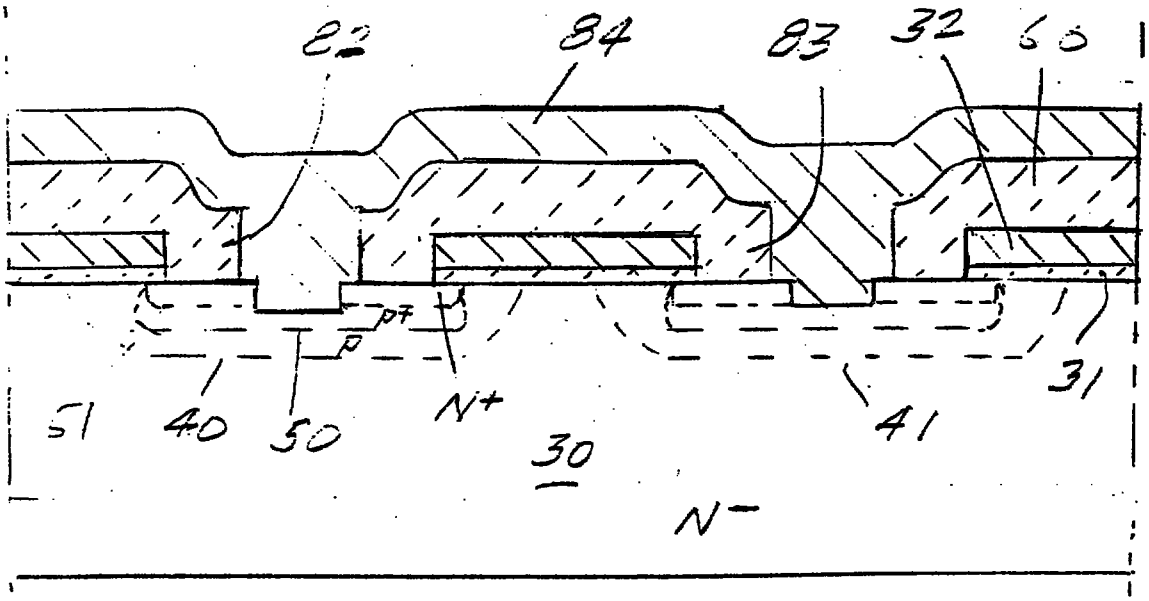

FIG. 11.

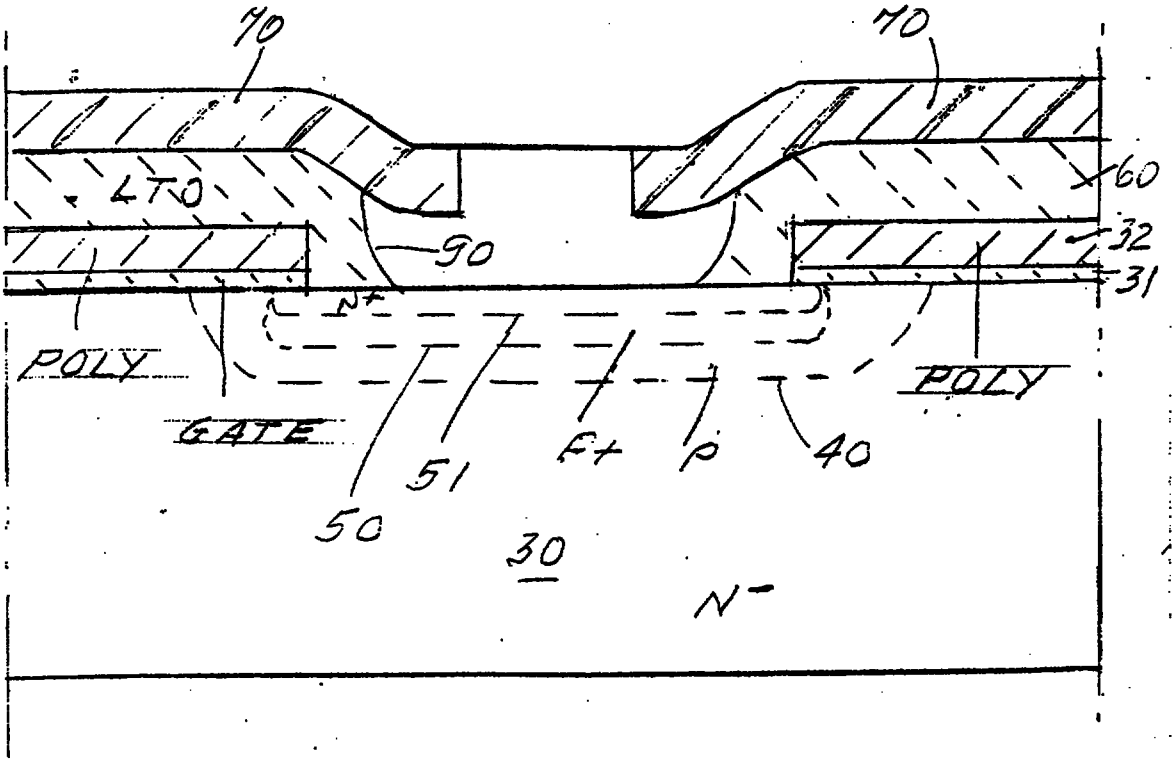

FIG. 12

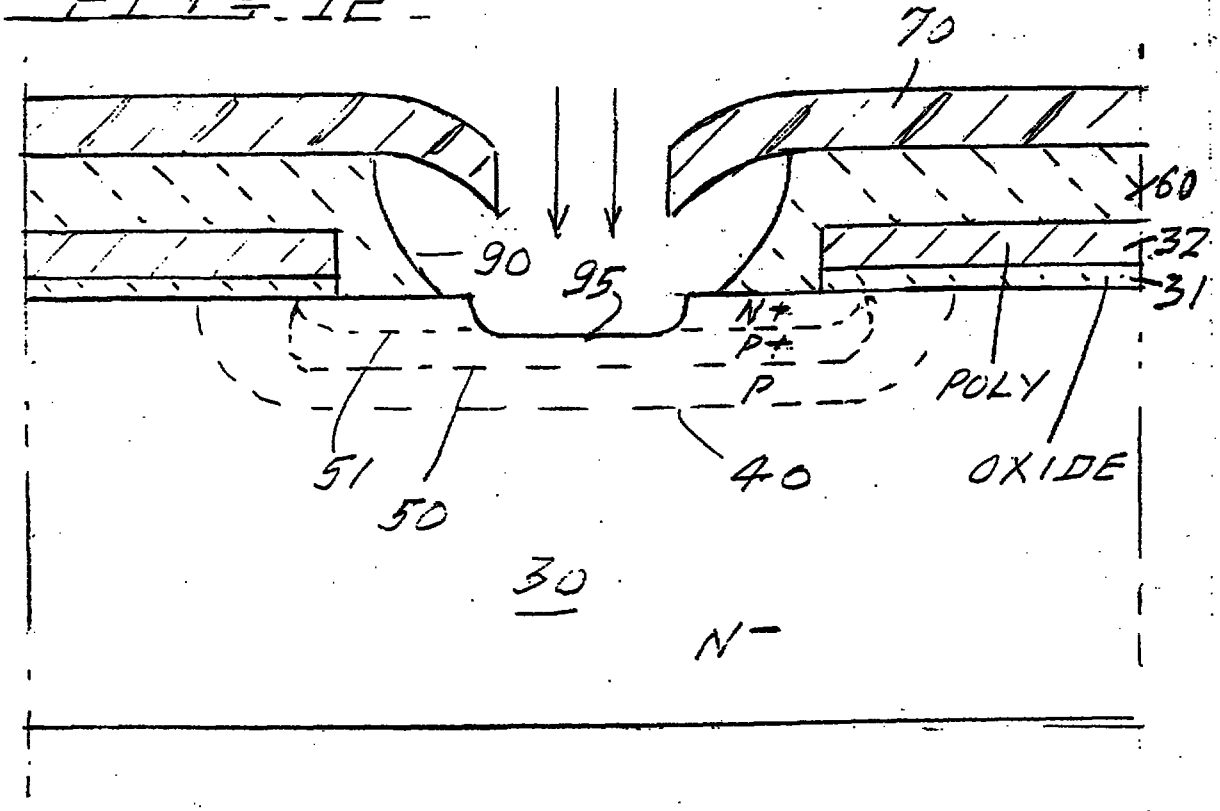

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FIG. 13

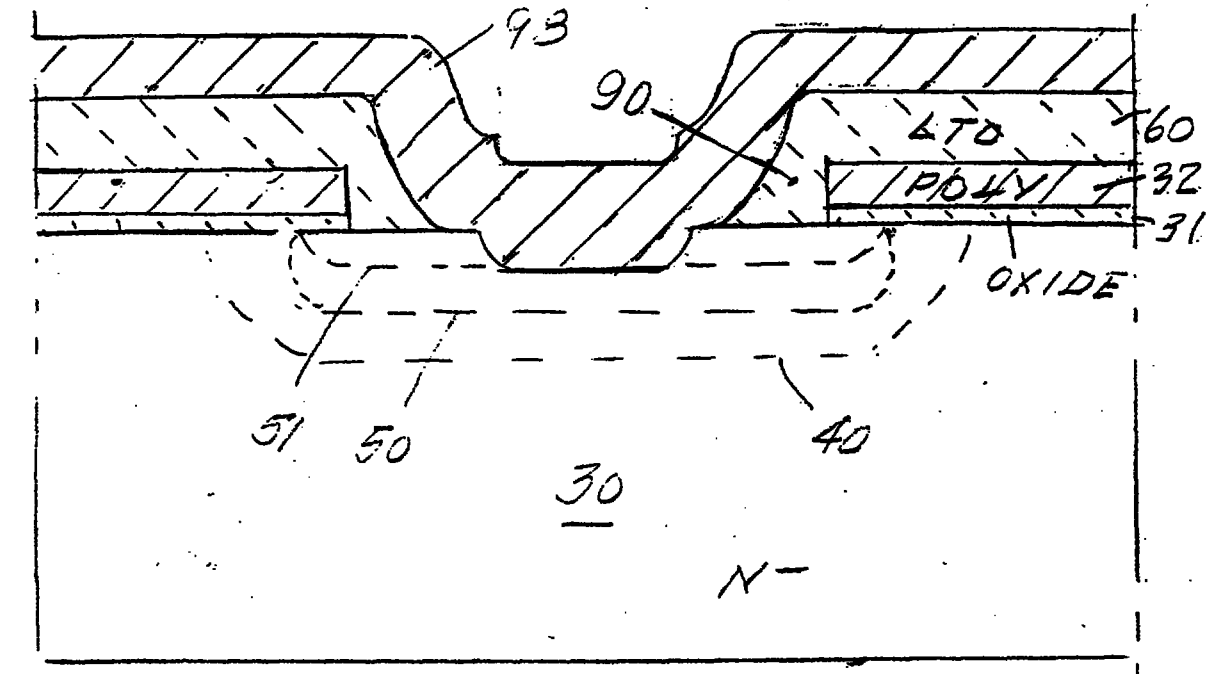

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FIG. 14

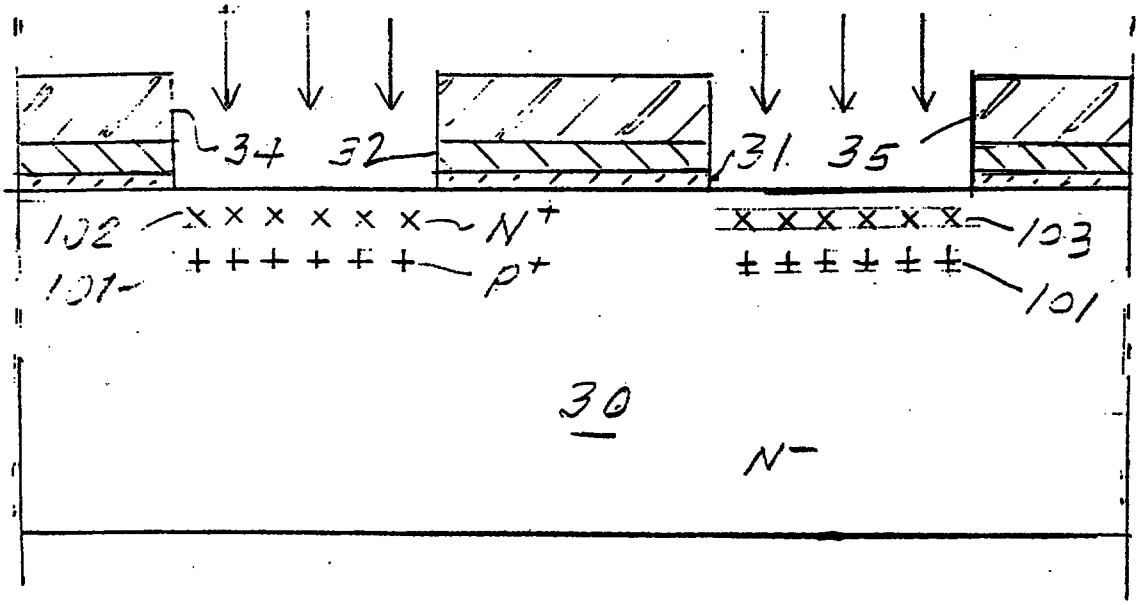

FIG. 15

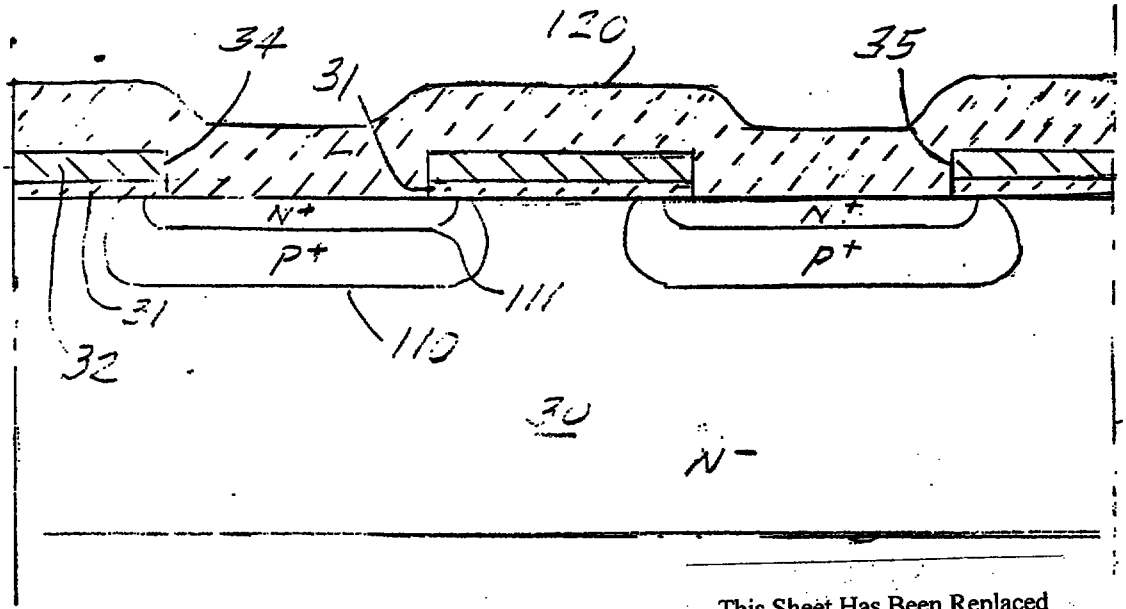

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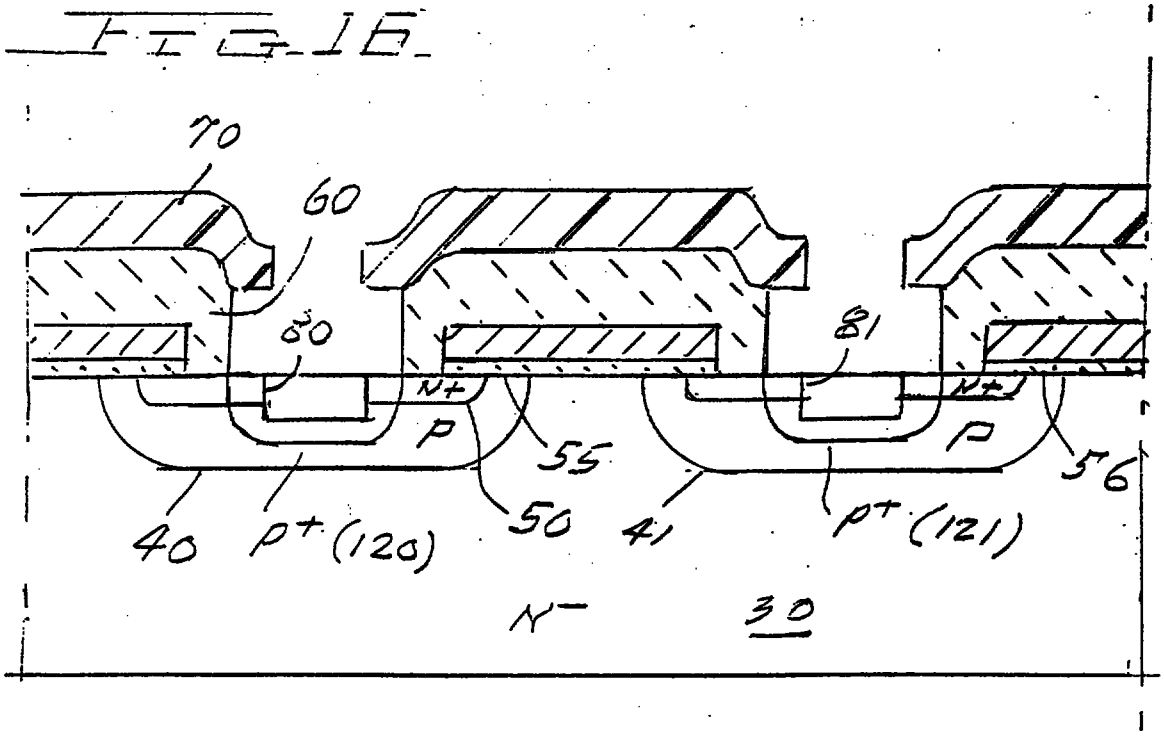
FIG. 1B



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PROCESS FOR MANUFACTURE OF MOS
GATED DEVICE WITH REDUCED MASK COUNT

ABSTRACT OF THE DISCLOSURE

A reduced mask process for forming a MOS gated device such as a power MOSFET uses a first mask to sequentially form a cell body and a source region within the cell body, and a second mask step to form, by a silicon etch, a central opening in the silicon surface at each cell and to subsequently undercut the oxide surrounding the central opening. A contact layer then fills the openings of each cell to connect together the body and source regions. Only one critical mask alignment step is used in the process.

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☑ Claim(s) : paged 17 to paged 23
☑ Drawing(s) : paged 1 to paged 7
☑ Abstract : paged - to paged -
DATE OF RECEIPT 13 MAR 1996

PROCESS FOR MANUFACTURE OF MOS GATED DEVICE WITH REDUCED MASK COUNT

BACKGROUND OF THE INVENTION

This invention relates to a process for the manufacture of a power MOS gated device, and more specifically relates to a novel process for the manufacture of such devices by a process using a reduced mask count and only one critical alignment step.

MOS gated devices are well known in the art and include such devices as power MOSFETs such as the power MOSFET shown in U.S. Patent 5,008,725, as well as power IGBTs such as the power IGBT shown in application Serial No. 07/521,177, filed May 9, 1990 (now abandoned) and in its continuation application Serial No. 08/041,136 filed March 30, 1993 (now refiled as application Serial No. 08/316,112 on September 30, 1994), the subject matter of which is incorporated herein by reference. MOS gated devices also include MOS gated thyristors, gate turn-off devices and the like.

The manufacturing process for such devices includes a number of photolithographic masking steps and critical mask alignment steps which each require additional manufacturing time and expense and which each produce possible sources of device defects. Reducing the number of masks and alignment steps necessary for the manufacture of such a device is desirable and improves the manufacturing yield and reduces the manufacturing cost.

U.S. Patent 5,302,537 discloses a process for the manufacture of a power MOSFET in which a hole is

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formed through the center of a source region and into an underlying base region. Metallizing enters the hole to connect together the source and base. However, these regions are connected only at the peripheral regions which are the walls of the hole. Thus, a low resistance, reliable contact between the source and base is difficult to form in a mass production process.

The present invention provides a novel manufacturing process which reduces the number of masks needed for the manufacture of a MOS gated power device to three.

SUMMARY OF THE INVENTION

In accordance with the present invention, and for an N channel device, a first mask defines the P-type body of each of the cells of the device, as well as a source region disposed within that P-type body region. Note that the device topology can be interdigitated as well as cellular. It is also to be noted that the body region is sometimes referred to as the channel region of the MOSFET cell. A second mask is then employed which is aligned with a small central area above the N^+ regions of each of the cells or strips of the device and an anisotropic oxide etch forms openings in the oxide layer covering the device which reach the surface of the silicon. An anisotropic silicon etch follows which causes a shallow hole in the surface of the silicon centered on the N^+ regions. The hole is deep enough to cut through the N^+ regions and reach the underlying P-type channels or body regions. The alignment of the second mask, which is the contact mask, is the only critical alignment in the process.

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This anisotropic silicon etch is then followed by an isotropic etch which undercuts the gate oxide and protective low temperature oxide above the gate oxide, thereby to expose shoulders at the silicon surface of the chip, which surround the etched openings into the N^+ cell regions.

Thereafter, a conductive layer, which may be metal, is deposited over the surface of the chip (or wafer in which a plurality of such chips are contained) and the metal fills the holes through the N^+ region, thereby contacting the underlying P body regions, and also overlaps the shoulders surrounding the N^+ source regions at the silicon surface. Consequently, a good contact is made to the N^+ source and to the underlying P region. Note that this contact between the P^+ underlying body region and the N^+ source region is desirable in order to short circuit the parasitic NPN transistor which inherently appears in each cell structure of a MOS gated device. A third mask is used to pattern the metal, followed by a sinter and backside metallization. Thus, the manufacturing process is reduced to only three mask steps, with only one critical alignment at the contact mask.

In an alternative process, in order to improve step coverage of the contact metal over the underlying gate oxide and low temperature oxide, the silicon etch step described above uses a photoresist shadow mask. First, the low temperature oxide and gate oxide area isotropically etched to expose an area of the silicon surface larger than the photoresist opening. This etch will leave a somewhat tapered oxide sidewall. Next, an anisotropic plasma etch using the photoresist as a shadow

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mask is carried out by a CL_2 plasma etch of well-known variety. This process will etch a hole through the N^+ source down to the P+ base, with the same area as the photoresist opening. Thus, a portion of the original N^+ surface remains exposed to receive the aluminum contact metal.

In order to complete the device, it is necessary to provide contact between the gate metal and gate polysilicon electrodes. This is accomplished in the same mask step as the contact to the source and body regions. This means that a hole will be etched in the polysilicon simultaneously with the hole in the silicon. It is necessary, therefore, to control the silicon etch depth such that the P^+ body region is exposed, but a portion of the polysilicon layer remains.

It is also necessary to provide an edge structure capable of withstanding the desired blocking voltage. A preferred edge structure can use a series of polysilicon rings and spaces. By shorting each polysilicon ring to the diffusions in the adjacent space on the active area side, such a structure can be obtained.

Another important feature of the invention is accomplished by implanting the heavy body implant into the same window as the source and deeper than the source. This allows the source to be almost completely surrounded by a heavily doped body region. This prevents punch-through breakdown and drain-source leakage as well, and also provides an extremely low resistance path in the body from the edge of each cell to the contact area in the center. The diffusion parameters can be adjusted in order to leave only a small, lightly doped body region

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immediately adjacent to the surface which forms the inversion channel.

As a further embodiment of the invention, the body region can be formed with a single implant and drive by implanting the body region to a first depth about as deep or deeper than the source and thereafter implanting the source region to a shallower depth. Both implants are carried out through the same mask window. These two regions are thereafter annealed and thus driven, with the body region annealed for three hours at about 975°C to obtain a depth of about 1-2 microns, whereas the source region is annealed for about one hour at 975°C to reach a depth of only about 0.3 microns. Thus, a complete cell can be formed employing only two implants. Thereafter, the manufacturing process can be completed as has been previously described.

In a further embodiment, a heavy base contact implant is carried out through the contact window instead of the polysilicon window. This is done after the hole has been etched in the silicon to expose the body region, and before metal is deposited on the wafer. Remarkably, no anneal is required after implant prior to metallization to achieve low contact resistance between metal and body regions. This is because a sinter of about 420°C is sufficient to activate enough dopant, and this temperature is low enough to be tolerated after the metal is deposited.

Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross sectional view of a portion of a chip within a wafer of silicon after an oxide layer, polysilicon layer and photoresist layer have been formed thereon.

Fig. 2 is a view of a device or structure of Fig. 1 after a first mask step has been carried out to produce a plurality of slots or openings of a symmetric arrangement in the photoresist layer.

Fig. 3 shows the structure of Fig. 2 showing the removal of the polysilicon and gate oxide regions which are exposed by the openings in the photoresist layer.

Fig. 4 shows the structure of Fig. 3 following an implant step for implanting a P^+ region through the windows in the polysilicon.

Fig. 5 shows the structure of Fig. 4 after the photoresist has been stripped and the P^+ implant has been driven to form a more lightly doped deep P region.

Fig. 6 is similar to Fig. 5 but shows the implant of P^+ and N^+ layers by implantation through the mask openings defined by the polysilicon gate.

Fig. 7 shows the structure of Fig. 6 following the deposition of a low temperature oxide over the surface of the device and following a drive for driving in the P^+ and N^+ implanted regions of Fig. 6.

Fig. 8 shows the structure of Fig. 7 following a second mask step which opens a central opening above each of the N^+ regions in the wafer and following an anisotropic etch of the underlying low temperature oxide and polysilicon to the surface of the silicon wafer.

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Fig. 9 shows the structure of Fig. 8 following an anisotropic silicon etch to form a depression cutting through the N^+ layers, followed by an isotropic oxide etch which undercuts the LTO and gate oxides.

Fig. 10 shows the structure of Fig. 9 following the stripping of the photoresist and the deposition of a source metal such as aluminum.

Fig. 11 shows a process modification which can be employed to improve step coverage wherein, following the step of Fig. 8, there is an isotropic etch of the low temperature oxide.

Fig. 12 shows the structure of Fig. 10 following the step whereby a silicon etch is carried out using the photoresist as a shadow mask.

Fig. 13 shows the structure of Fig. 12 following the stripping of the photoresist and the metallizing of the structure with improved step coverage.

Fig. 14 shows an improvement for the process wherein, following the step of Fig. 3, an N^+ implant and a P^+ implant are formed through the openings formed by the first mask.

Fig. 15 shows the structure of Fig. 14 following junction anneals which form cells or strips having P^+ bodies and N^+ source regions, with the structure being completed by the steps previously described.

Fig. 16 shows a further embodiment of the invention in which the P^+ diffusion is formed through the contact mask.

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DETAILED DESCRIPTION OF THE DRAWINGS

The following description of the preferred embodiments of the invention describes the manufacture of an N channel power MOSFET device. However, any suitable junction modification can be employed to use the same reduced mask count process for the manufacture of any MOS gated device such as an IGBT or a MOS gated thyristor whether N channel or P channel. A specific topology is not expressly shown in these drawings, but it is noted that the topology to be used is preferably that of hexagonal cells, such those shown in Patent 5,008,725. However, it will be apparent to those skilled in the art that the process is equally applicable to structures having any polygonal structure such as square or rectangular cells, whether offset or in line, as well as to interdigitated structures. It should be further noted that the termination structure of the device is not shown, but the terminations commonly used for any MOS gated device can also be used here.

Referring first to Fig. 1, there is shown only a very small portion of a wafer or chip which has a repetitive structure, only a few elements of which are shown in cross section. The wafer may be of any desired size and will be diced into a plurality of chips. In the description of the preferred embodiments of the invention herein, the terms "chip" and "wafer" are sometimes interchanged.

Fig. 1 shows a wafer having an N^- body 30 with monocrystalline silicon. The N^- body 30 may be an epitaxially formed layer atop an N^+ substrate (not shown). A drain (or anode) contact may be connected to the N^+ substrate and may be available for connection at

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either surface of the chip. The epitaxially formed body will have a thickness and resistivity depending upon the breakdown voltage of the ultimately formed device.

The first step in the process of the invention is the formation of an insulation layer 31 atop the silicon 30 where the layer 31 can be thermally grown silicon dioxide having a thickness of from 200 to 1,500 angstroms depending upon the desired threshold voltage of the subsequently formed device. The oxide layer 31 is then covered, in turn, by a layer of polysilicon 32 which may have a thickness, for example, of 7,500 angstroms and is formed in any desired manner. Preferably, the polysilicon is doped heavily with implanted arsenic or with a subsequent CVD doping step. A suitable photoresist layer 33 is then formed atop the polysilicon layer 32.

As shown next in Fig. 2, the photoresist 32 has been patterned by an appropriate photolithographic mask step and openings 34 and 35 are formed through the photoresist to the surface of the polysilicon layer 32. If a cellular topology is chosen, each of openings 34 and 35 may be one of many thousands of identical symmetrical openings which have any desired polygonal configuration such as that of a hexagon or square which would have a dimension from side to side of about 5-10 microns and a spacing center to center which depends on voltage and photolithography capability. Note, however, that the openings 34 and 35 could also be parallel elongated strips if the topology chosen is an interdigitated topology.

Following the formation of openings in the photoresist layer 33 in Fig. 2, an anisotropic etch is employed to etch the exposed polysilicon, as shown in

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Fig. 3. Preferably, the anisotropic polysilicon etch should not undercut the photoresist because the area of the subsequent implant should preferably be defined by the polysilicon, not the photoresist. The etch is selective enough to stop prior to removal of gate oxide anywhere on the wafer. The polysilicon sidewall should also be as nearly vertical as possible, which is important to accurately define the deep body implant region.

Thereafter, the underlying exposed silicon dioxide may be removed, if desired, with an isotropic wet etch. The anisotropic and isotropic etches to be used are those which are well known to those of ordinary skill and any etch can be selected for these non-critical steps. Note, however, that it is also possible at this step in the process to leave the gate oxide intact and to do subsequent implant processes with sufficiently high energy to penetrate that thin gate oxide.

Thereafter, and as shown in Fig. 4, an implant is carried out employing boron as the implant species having a dose of 3-8E13 at an energy of about 80 kV. This implant forms P type regions 40 and 41 beneath the bottom of the exposed openings in the photoresist 33 and oxide 31.

Following this implant operation and as shown in Fig. 5, the photoresist 33 is stripped and the P^+ implants 40 and 41 are driven at 1175°C for about 30-60 minutes to reach a depth of from 1.0 - 2.0 microns. Other implant energies and diffusion times and depths could be selected by the designer depending upon the type device he wishes to form.

In the next process step, shown in Fig. 6, a relatively high N^+ dose of arsenic or phosphorus, for

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example, 1E16, is implanted through the windows 34 and 35 at an implant energy of about 120 kEV. A diffusion step can follow. For example, if arsenic is the species used, it can be driven at 975°C for about one hour. A thin oxide (not shown) is grown during this time on the polysilicon sidewalls to encapsulate the polysilicon prior to the deposition of a low temperature oxide. Thereafter, P^+ boron is implanted through windows 34 and 35 at a dose of about 1E15 and implant energy of from 80 to 120 kEV. The N^+ layer 50 will be shallower than the P^+ layer 51 by an amount selected by the designer and determined by the species and doses used.

Thereafter, and as shown in Fig. 7, a layer 60 of low temperature oxide ("LTO") is deposited atop the surface of the wafer of Fig. 6 to a thickness of from 0.6 to 0.8 microns. The LTO deposition conditions employ a silane decomposition reaction with oxygen at about 425°, thus forming the LTO layer 60. The thickness is selected to minimize gate-source overlap capacitance and shorts, while allowing convenient patterning and good step coverage.

After the deposition of the LTO layer 60, the N^+ and P^+ regions 50 and 51 are driven at a temperature of about 975° for about 30 minutes. These junctions then drive to depths of about 0.3 microns for the N^+ region and 1 micron for the P^+ region. By doing the drive after the deposition of the LTO layer 60, the LTO layer will also densify under the drive conditions.

It will be noted that this operation has produced annular channel regions 55 and 56 for the two cells which are shown. These channel regions underlie respective segments of the polysilicon layer 32, which

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defines the polysilicon gate for each cell, and are invertible upon the connection of a gate potential to the polysilicon layer 32. The polysilicon layer 32 will have a lattice configuration between the cells if the cells are of a polygonal structure. This lattice will, at its sides or edges, overlie the underlying channel regions within the cells.

Proper selection of diffusion parameters will prevent the P^+ dopant from reaching the surface channel regions in sufficient quantity to substantially change the threshold voltage. The process can be designed, with careful controls, to allow the P^+ to contribute in part to the peak channel doping. This provides the best punch-through protection and the opportunity for the shortest channel. This requires very careful control of polysilicon sidewall profile as nearly vertical as possible.

Thereafter, and as shown in Fig. 8, a new photoresist layer 70 is applied atop the LTO layer 60 and the photoresist layer 70 is patterned by a second, and contact mask step, to form well aligned small central openings which are located at the axis of each of the individual cells, or along the length of strips if an interdigitated geometry is used. This is the only critical alignment step in the novel process. If a cellular structure is used, the openings in the photoresist 70 have a diameter of about 1.5-2 microns. This dimension depends on the photolithography process and metal-silicon contact system. After the formation of the openings in the photoresist, the LTO layer is etched by an anisotropic oxide etch to open a central opening which reaches the silicon surface.

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Thereafter, and as shown in Fig. 9, an anisotropic etch is carried out which etches the exposed silicon surface so that holes are formed in the silicon surface which penetrate the N^+ layers 51 and reach the P^+ layer 50 for each cell. Thus, by using a chlorine chemistry anisotropic plasma etch, about 0.4 microns of silicon are removed at the surface, forming the depressions or openings 80 and 81 in the centers of the cells formed by regions 40 and 41.

Thereafter, and as is also shown in Fig. 9, the silicon wafer is exposed to an isotropic wet etch which acts to undercut the LTO back to diameters 82 and 83. This action exposes, for a hexagonal or polygonal cell, a shoulder of the surface of the silicon chip which extends around openings 80 and 81.

In a preferred embodiment of the invention, the wet etch forming the undercut in the LTO and gate oxide is a wet 6 to 1 buffered oxide etch for 2-5 minutes. This creates a shoulder of about .2-.5 microns in width, which is sufficient to make a low resistance contact to the source region.

Thereafter, and as seen in Fig. 10, the photoresist 70 is stripped and a source metal 84, for example, aluminum is deposited over the full surface of the device. The aluminum will fill in the openings 80 and 81 and will overlie the exposed silicon shoulders formed by the undercuts 82 and 83 in Figs. 9 and 10. Thus the source metal 84 automatically connects the underlying P region 50 to the N^+ region 51 to make the intentional short between the P and N regions in each cell.

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The structure shown in Fig. 10 produces a complete MOSFET cellular configuration (or interdigitated configuration, if that is chosen) and the remaining steps in the processing of the device will include the usual non-critical mask for patterning gate and source electrode connection regions, and an optional mask for opening windows in an insulating scratch layer or the like. The basic process steps not counting the scratch mask required only three masks for the production of the MOS gated device with only one critical alignment.

It is to be also noted that, to complete the device of Fig. 10, a drain contact is needed. This drain contact can go onto the bottom of the wafer in the usual manner or can, if desired, be placed on the top of the wafer and connected to the common conduction regions between the cells 40 and 41 by sinkers and buried layers or the like as disclosed in Patent 5,191,396. Note also that, if the device is to be made into an IGBT, the usual thin N^+ buffer layer and P^+ bottom layer would be added to the bottom of the wafer structure in the conventional manner.

Fig. 11 shows a second embodiment of the process of the invention wherein, following the step of Fig. 8, the LTO is etched by an isotropic etch to form the radius curve 90 for the walls of the openings. This etch can be carried out with a 6 to 1 buffered oxide etch for about 8 minutes. The lateral dimension of the undercut of the curve will be about 0.5 micron at the bottom and about 1 micron at the top of the LTO layer.

Thereafter, as shown in Fig. 12, the overhanging portion of the photoresist layer, which has been undercut by the earlier isotropic etch, is used as a shadow mask in an anisotropic plasma etch process using a

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chlorine plasma. This anisotropic plasma etch will form a central opening 95 in the cell which may have a depth of 0.4 microns but is deep enough to reach and cut into the P^+ region 50.

The gradual curve 90 in the LTO layer 60 and the reduced diameter opening 95 in the silicon provides a smoother surface over which the aluminum electrode can later be formed. Thus, it is well known that aluminum does not cover sharp angles well, and it is preferred to have surfaces with a gradual curvature to improve aluminum step coverage. That is precisely the effect created by the process step shown in Fig. 12.

As shown in Fig. 13, the photoresist 70 is stripped and an aluminum contact layer 98 is deposited over the surface and more easily follows the gradual curve 90 in the LTO to provide better step coverage for the aluminum electrode. Note that the aluminum electrode also automatically makes contact between the P^+ region 50 and the N^+ region 51, thus accomplishing the desired short of these two layers at their center.

Figs. 14 and 15 show a still further embodiment of the invention wherein, following the step of Fig. 3, the junctions used to produce the ultimate cells or interdigitated regions are formed by the two implants which are a first boron implant of 3E14 at 120 kV forming the P^+ regions 100 and 101 in openings 34 and 35 in the oxide 31. The photoresist is removed, and the region is then annealed for about one hour at 1050°C. Then an implant of arsenic or phosphorus at 1E16 at 120 kV forms the layers 102 and 103 in the openings 34 and 35, respectively. Following the implant, the photoresist layer is removed, and an LTO layer 120 is deposited and

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the source implant is annealed for about one hour at 975°C. This steps drives the P^+ region 110 to about 1.4 microns and the N^+ region 111 to about 0.3 microns.

Thereafter, the wafer containing the two junctions will be processed as described previously. It will be noted that the P^+ region in the channel region at the surface of the device can have a relatively low P type concentration if properly controlled and thus can be an easily invertible channel area.

Referring next to Fig. 16, there is shown a further embodiment of the invention wherein the device is processed as shown in Fig. 9, but the P^+ region 51 is not formed through the polysilicon windows 34 and 35. Instead, in Fig. 16, the heavily doped P^+ contact regions 120 and 121 are formed through the contact mask after the holes 80 and 81 have been etched to expose the surfaces of body regions 40 and 41. The structure is then processed as described in Figs. 10 to 13. Unexpectedly, no anneal is needed following the implants of regions 120 and 121. This is because the subsequent sinter of the metal 84 (Fig. 10) after its deposition at about 420°C is sufficient to activate enough dopant, and the temperature is low enough to be tolerated after metal is deposited as in Fig. 10.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

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* C L M S *

WHAT IS CLAIMED IS:

1. A process for the manufacture of a MOS gated semiconductor device; said process comprising the steps of forming a layer of gate insulation material atop a silicon substrate, forming a layer of polysilicon atop said layer of gate insulation material, forming a first photoresist layer atop said layer of polysilicon, forming a plurality of spaced openings in said first photoresist layer through the use of a first photolithographic masking step to expose portions of said layer of polysilicon; etching the portions of said layer of polysilicon which are exposed through said plurality of spaced openings in said photoresist layer to expose corresponding surface regions of the surface of said silicon substrate; diffusing impurities of a first conductivity type into said surface regions of said silicon substrate to form first diffused regions; diffusing impurities of a second conductivity type into said surface regions of the surface of said silicon substrate to form second diffused regions wherein said second diffused regions at each of said surface regions of said silicon substrate have a final depth and lateral extent which is less than that of said first diffused regions; thereafter depositing a second insulation layer over the upper surface of said device, forming a second photoresist layer atop said second insulation layer, forming, by a second photolithographic step which is aligned with said first masking step, a plurality of central openings in said second photoresist layer which are centrally aligned with respective ones of said plurality of spaced openings which were formed in said first photolithographic masking step; said central openings each having a lateral extent which is less than

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the lateral extent of said respective second diffused regions and having side walls which are perpendicular to the plane of the surface of said silicon substrate; etching away the portions of said second insulation layer which are exposed by said central openings to expose respective corresponding underlying second surface regions of said silicon substrate; etching depressions in the second surface regions of said silicon substrate to a depth greater than the depth of said second diffused regions, etching to form undercut portions in said second insulation layer surrounding said second surface regions of said silicon substrate to expose portions of the surface of said substrate which are adjacent said undercut portions of said surface at said silicon substrate, and thereafter depositing a conductive layer over the surface whereby said conductive layer contacts both said first diffused regions at the bottom of said depressions, and said second diffused regions at the upper portions of said undercut portions and the surrounding surfaces of said undercut portions; said first diffused regions being relatively highly doped and closely surrounding respective ones of said second diffused regions to reduce punch-through breakdown and drain to source leakage and to provide a low resistance current carrying path beneath said second diffused regions.

2. The process of claims 1 wherein said thin layer of gate insulation material is silicon dioxide.

3. The process of claim 1 wherein said plurality of spaced openings in said photoresist layer have identical shapes.

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4. The process of claim 3 wherein said plurality of spaced openings are selected from the group consisting of closed polygons and elongated strips.

5. The process of claim 1 wherein said first and second diffused regions are formed by the steps of implanting impurity atoms and then heating said substrate to diffuse said impurity atoms into said substrate.

6. The process of claim 1 wherein said second insulation layer is a low temperature oxide.

7. The process of claim 1 wherein said depressions in the second surface regions are formed by an anisotropic etch, and said undercut portions in said second insulation layer are formed by an isotropic etch.

8. The process of claim 1 wherein said conductive layer is a main electrode layer for the device being formed.

9. The process of claim 1 wherein said undercut portions in said second insulation layer are formed by an isotropic etch which etches curved walls in said undercut portions of said second insulation layer to define overhanging shadow-mask lips in said second photoresist layer which border said depressions, and wherein said etch of the exposed second surface regions is an anisotropic silicon etch using said overhanging shadow mask lips as a shadow mask thereby to reduce sharp edges on the surface of said silicon substrate and to

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improve the subsequent formation of said conductive layer.

10. The process of claim 9 wherein said plurality of spaced openings in said photoresist layer have identical shapes.

11. The process of claim 10 wherein said plurality of spaced openings are selected from the group consisting of closed polygons and elongated strips.

12. The process of claim 9 wherein said second insulation layer is a low temperature oxide.

13. The process of claim 9 wherein said conductive layer is a main electrode layer for the device being formed.

14. The process of claim 1 which includes the step of forming diffused regions of impurities of said first conductivity type which are deeper and wider and which have a lower concentration than that of said first and second diffused regions.

15. The process of claim 9 which includes the step of forming diffused regions of impurities of said first conductivity type which are deeper and wider and which have a lower concentration than that of said first and second diffused regions.

16. The process of claim 1 wherein the areas of said second insulation layer which underlie said central openings are etched by an anisotropic etch which

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does not undercut said second insulation layer beneath said first photoresist layer to leave the side of said central openings as vertical as possible.

17. The process of claim 6 wherein, following the formation of said low temperature oxide, said substrate is heated to simultaneously drive said first and second diffused regions and to densify said low temperature oxide layer.

18. A process for the manufacture of a MOS gated semiconductor device; said process comprising the steps of forming a layer of gate insulation material atop a silicon substrate, forming a layer of polysilicon atop said layer of gate insulation material, forming a first photoresist layer atop said layer of polysilicon, forming a plurality of spaced openings in said first photoresist layer through the use of a first photolithographic masking step to expose portions of said layer of polysilicon; etching the portions of said layer of polysilicon and of said layer of gate insulation material which are exposed through spaced openings in said first photoresist layer to expose corresponding surface regions of the surface of said silicon substrate; said spaced openings having side walls which are perpendicular to the plane of the surface of said silicon substrate; diffusing impurities of a first conductivity type into said surface regions of said silicon substrate to form first diffused regions; diffusing impurities of a second conductivity type into said surface regions of the surface of said silicon substrate to form second diffused regions wherein said second diffused regions at each of said surface regions of said silicon substrate have a final depth and

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lateral extent which is less than that of said first diffused regions; said first diffused regions being relatively heavily doped and closely surrounding respective ones of said second diffused regions.

19. The device of claim 1 which further includes the diffusion of a third region of impurities of said first type into said exposed surface regions prior to the diffusion of said first diffused regions; said third diffused regions defining channel regions of lower concentration than that of said first diffused regions.

20. The device of claim 1 which further includes the diffusion of a third region of impurities of said first conductivity type into said surface regions prior to the diffusion of said first diffused regions; said third diffused regions defining channel regions of lower concentration than that of said first diffused regions.

21. The process of claim 1 which includes the further step of diffusing impurities of the first conductivity type into said silicon substrate exposed by the etching of said second surface regions; said impurities which are diffused during said further step forming third regions of said first conductivity type which are more heavily doped than said first diffused regions.

22. The process of claim 19 which further includes the step of sintering said conductive layer at a temperature of less than about 450°C, thereby to anneal said third diffused regions.

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23. A MOS gated semiconductor device; said device comprising a wafer of monocrystalline silicon having at least one flat surface having a first conductivity; a plurality of spaced cells symmetrically distributed over and formed into said one flat surface; each of said cells having an identical structure, including a first region of a second conductivity type and having a first depth and a first lateral extent and extending from said first surface and into the body of said wafer, a second region of said first conductivity type formed at least partly within said first region and extending from said first surface; said second region being laterally spaced from said first region at at least portions of their coextensive lengths on said first surface, a gate insulation layer overlying at least the area on said first surface formed between the laterally spaced first and second regions, a gate electrode overlying said gate insulation layer; characterized in that a laterally central depression is etched into each cell, extending from said first surface, through said second region and into said first region; and a contact layer extending over said first surface and into each of said central depressions, thereby to electrically connect together said first and second regions.

24. The process of claim 1 wherein said layer of gate insulation material is etched during the step of etching the portions of said layer of polysilicon.

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FIG. 1.

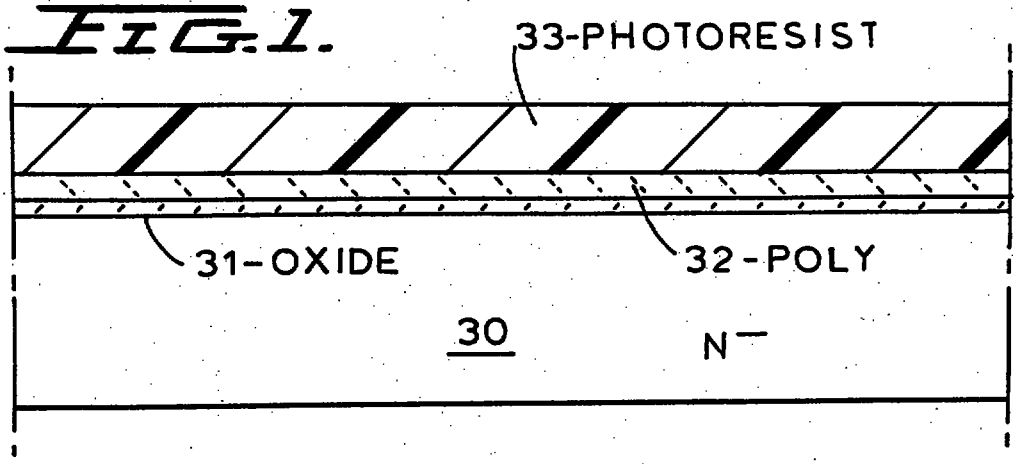

FIG. 2.

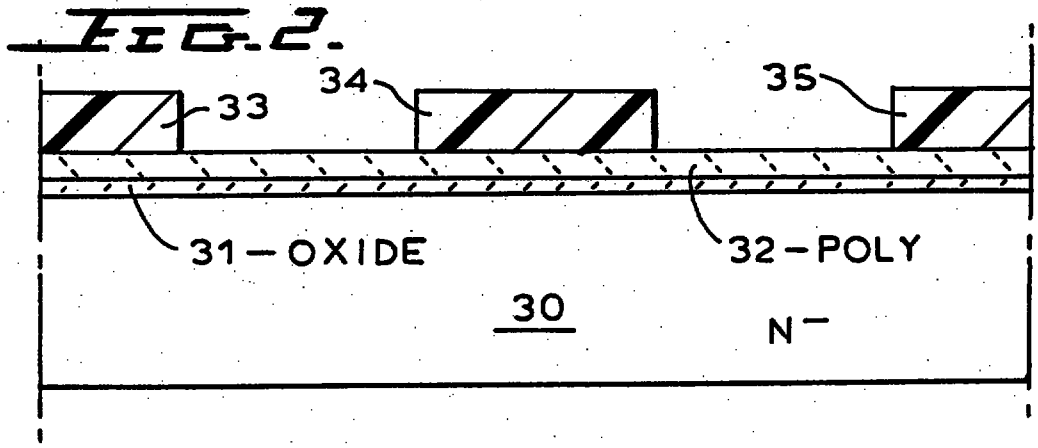

FIG. 3.

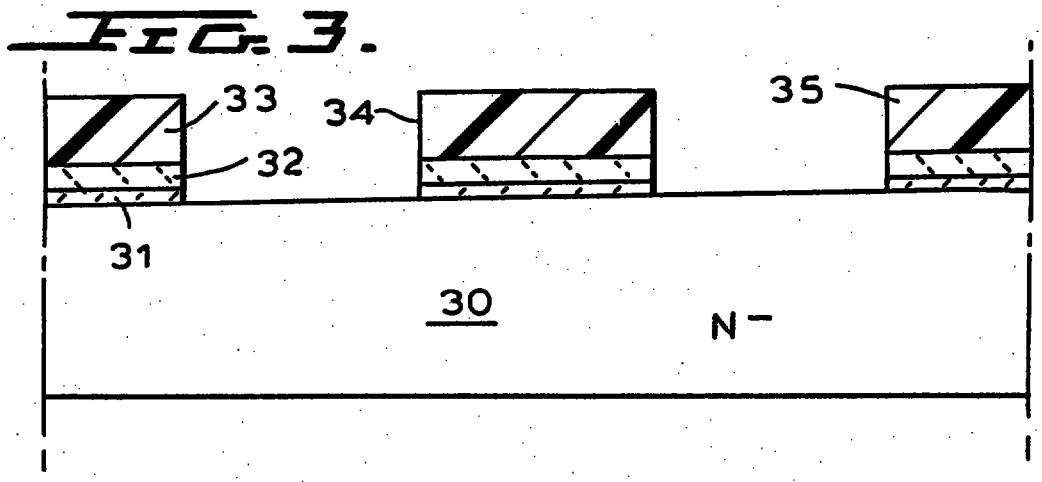

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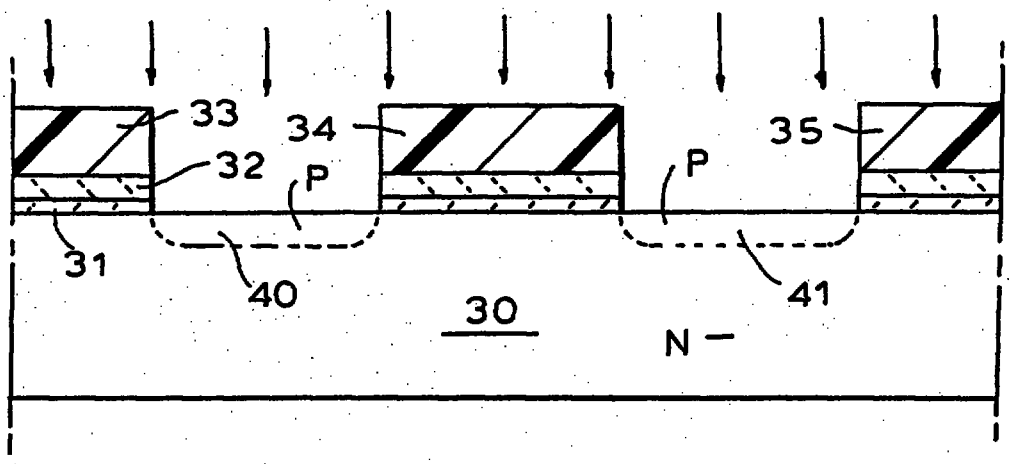
FIG. 4.



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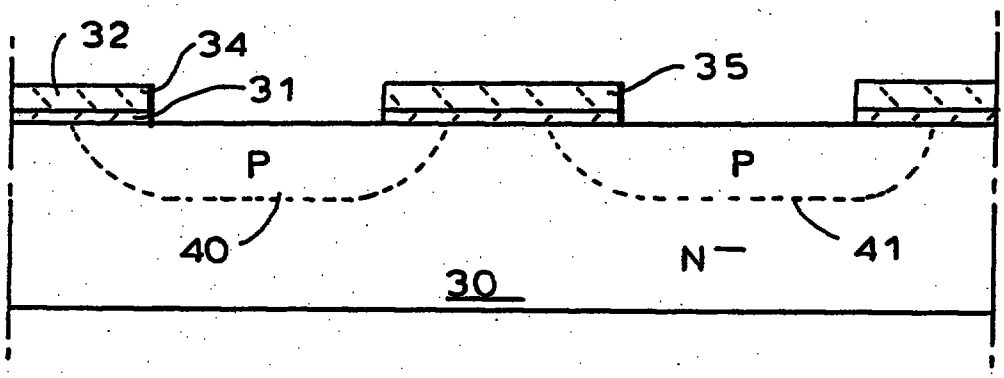

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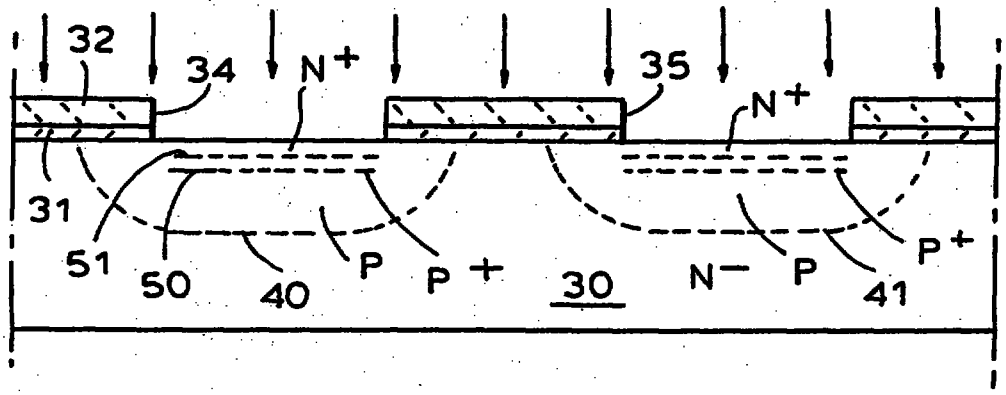

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FIG. 7

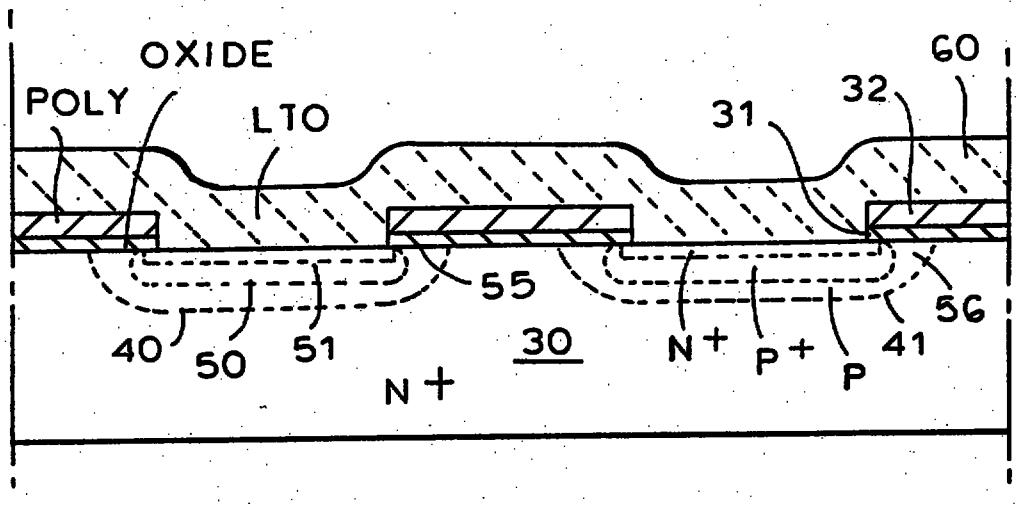

FIG. 8

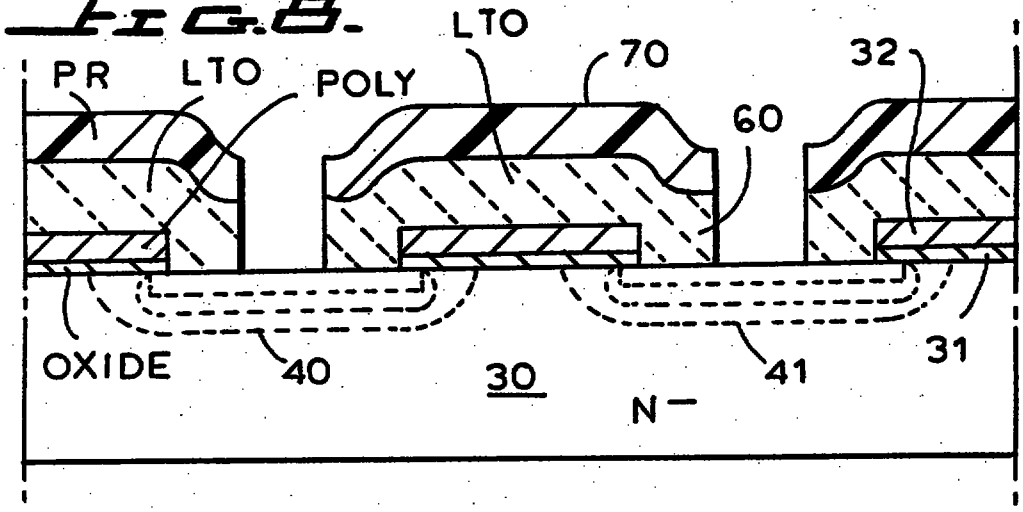

FIG. 9

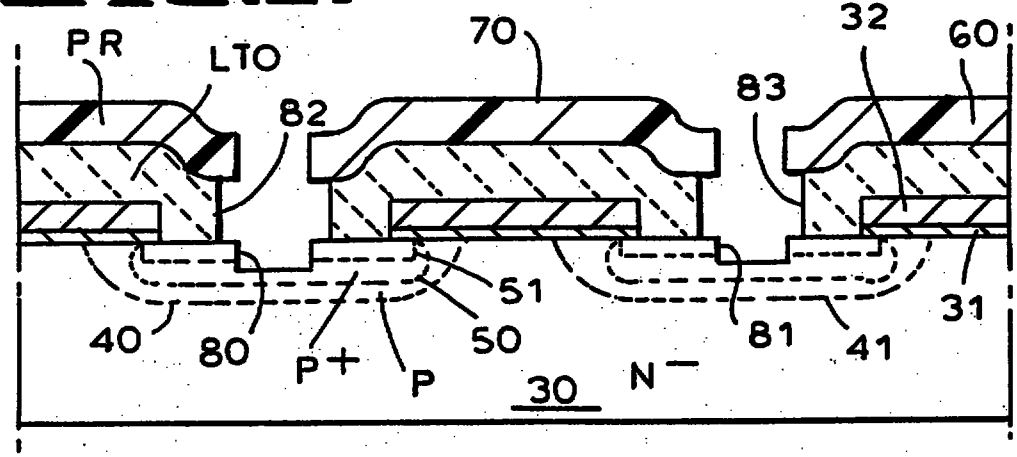

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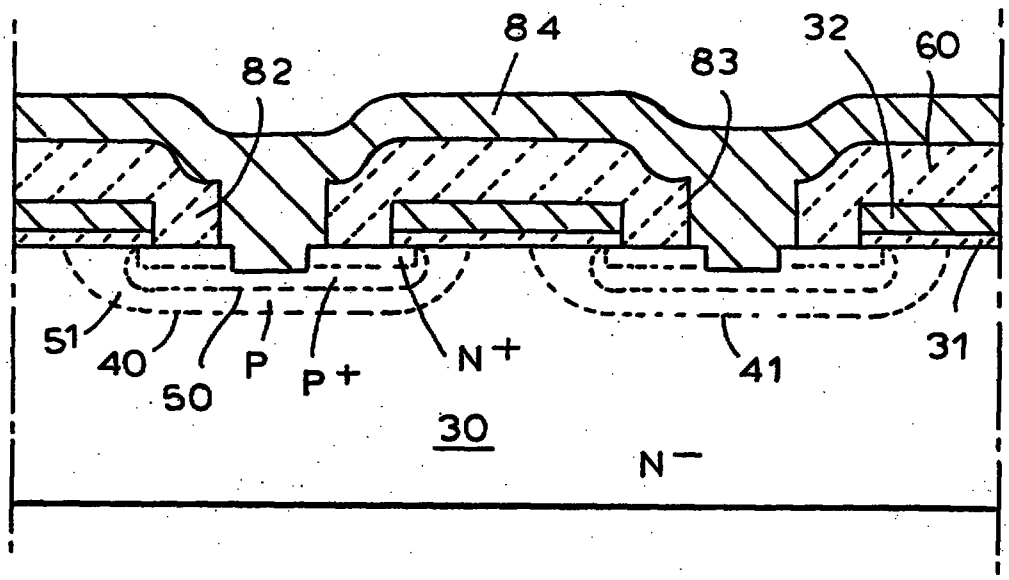
FIG. 10.



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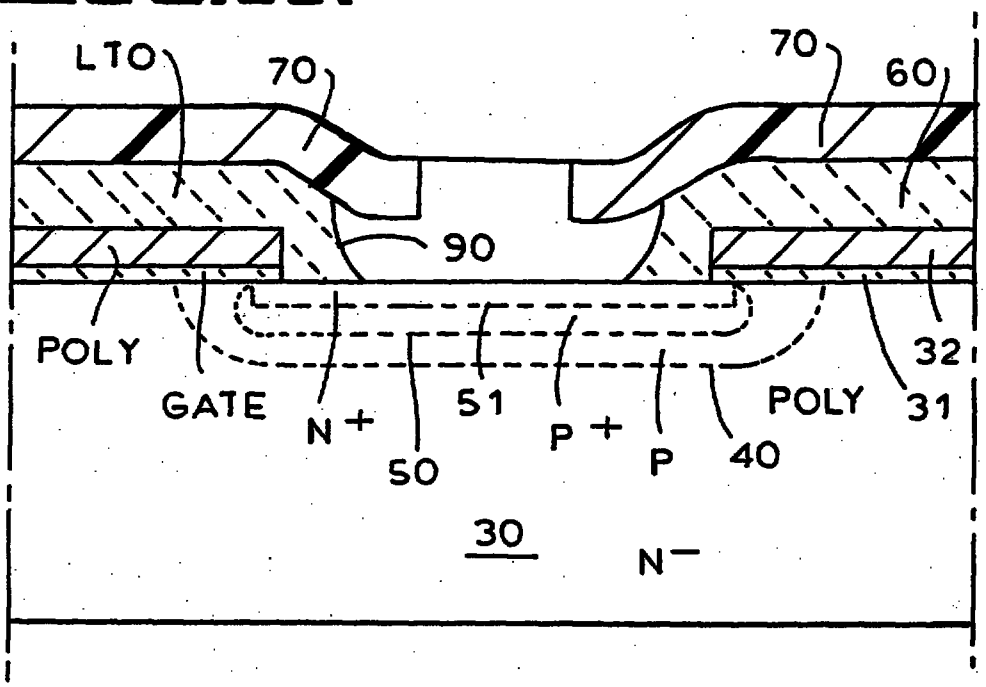

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FIG. 12.

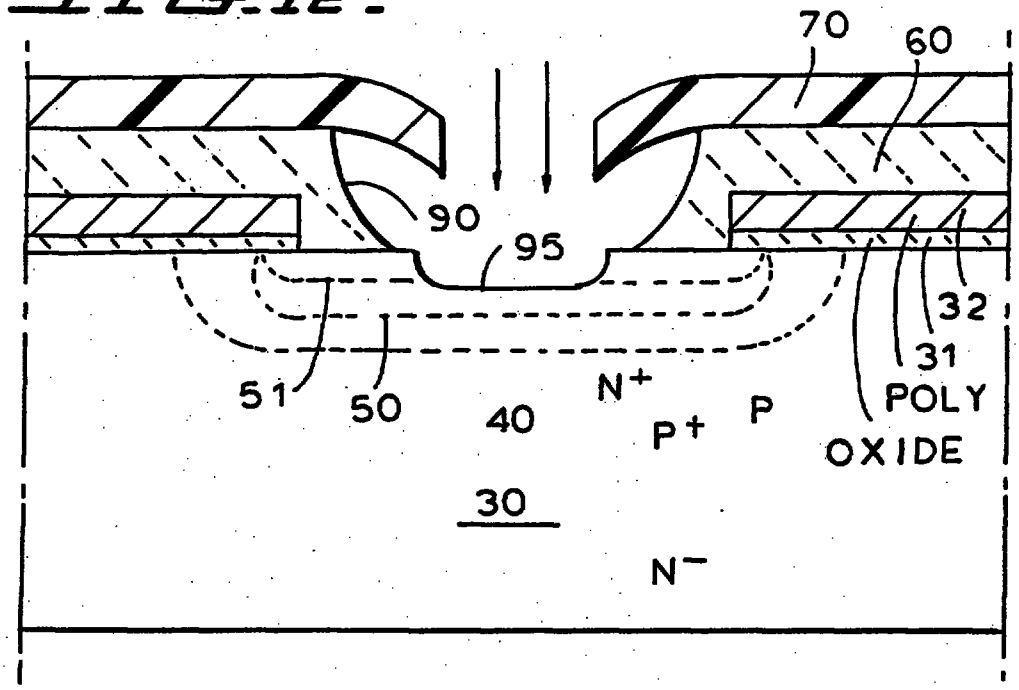

FIG. 13.

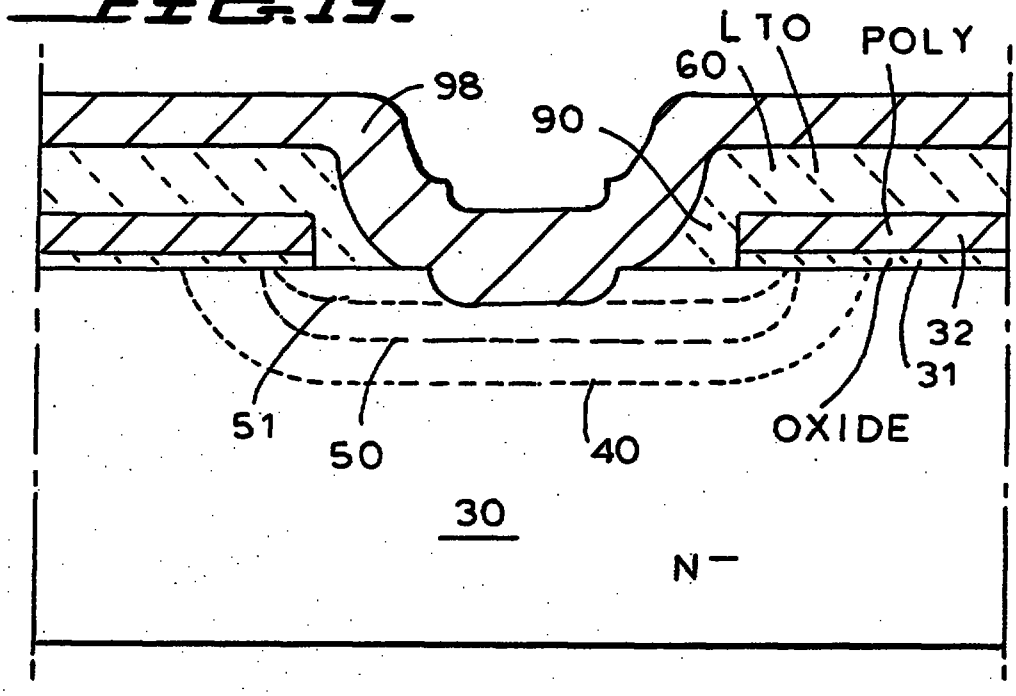

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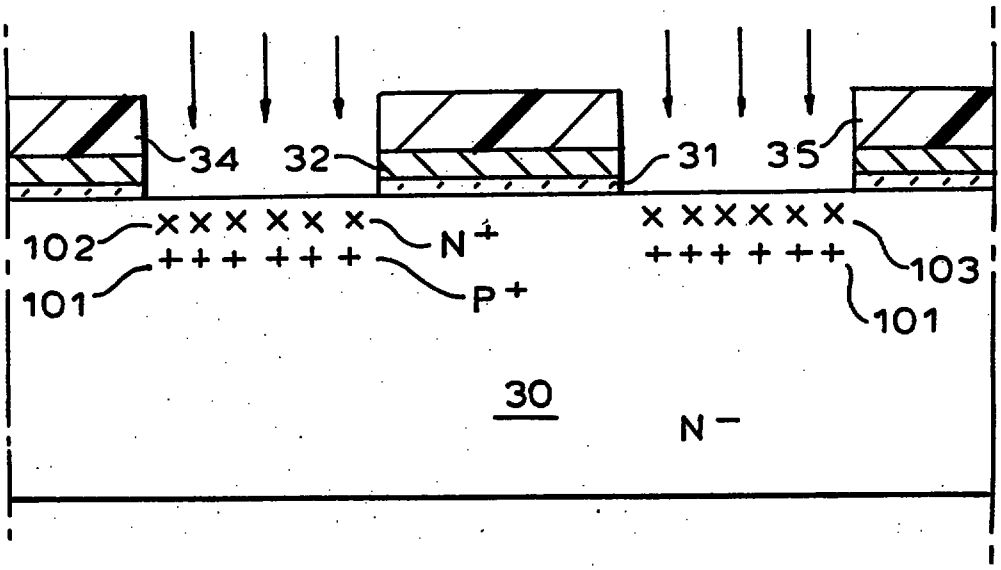
FIG. 14.



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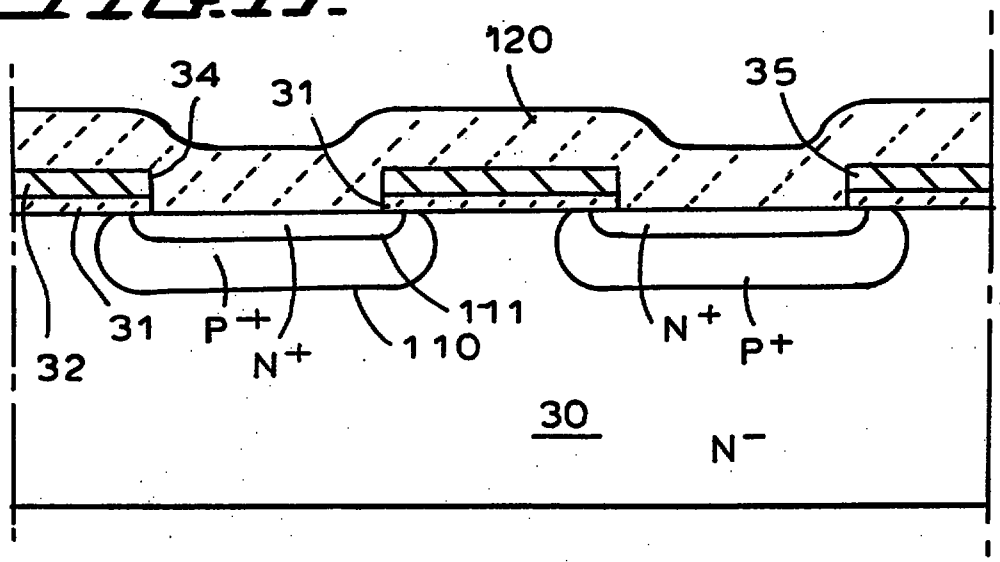

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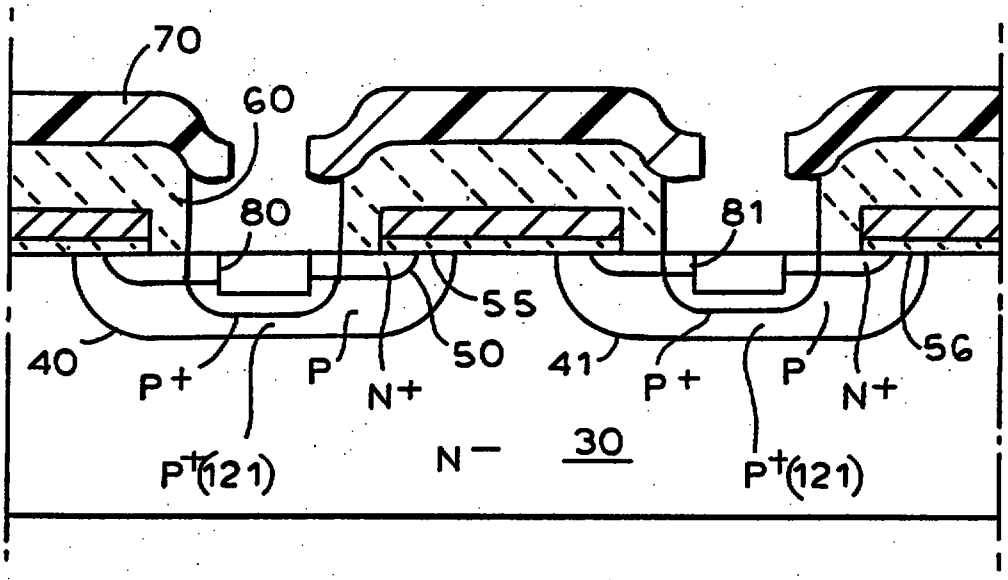
FIG. 16.



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PROCESS FOR MANUFACTURE OF MOS
GATED DEVICE WITH REDUCED MASK COUNT

ABSTRACT OF THE DISCLOSURE

A reduced mask process for forming a MOS gated device such as a power MOSFET uses a first mask to sequentially form a cell body and a source region within the cell body, and a second mask step to form, by a silicon etch, a central opening in the silicon surface at each cell and to subsequently undercut the oxide surrounding the central opening. A contact layer then fills the openings of each cell to connect together the body and source regions. Only one critical mask alignment step is used in the process.

Figure 10

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