layer 102, improve surface mount yield and solder joint reliability. Further, solder formation is improved around the vertical sides of the terminals 132.

Referring now to FIG. 3, therein is shown an isometric topside view of the CSP 100 without the encapsulant 150. The integrated circuit die 108 is shown surrounded by the ground ring 144 and by the signal terminals 142. The ground wires 112 may be bonded any place along the ground ring 144 thereby increasing the possibility of heat transfer as well as multiple ground paths.

Referring now to FIG. 4, therein is shown a cross-sectional side view of an embodiment of a thermally/electrically enhanced super thin die down CSP 400. The CSP 400 includes a core layer 402 having a first conductive layer 404 and a second conductive layer 406 on opposite sides. The core layer 402 can be a non-conductive material such as such as thin core glass (bismaleimide triazine resin), epoxy laminate, or polyimide and the first and second conductive layers 404 and 406 can be of conductive metals such as aluminum, copper, or gold.

An integrated circuit die 408 is bonded with a die attach adhesive 410 to the second conductive layer 406. The die attach adhesive 410 may be of thermally and/or electrically conductive or non-conductive material such as epoxy or glass. The integrated circuit die 408 is connected by ground wires 412 and signal wires 414 to the second conductive layer 406. The ground and signal wires 412 and 414 are of materials such as aluminum, copper, or gold.

The core layer 402 has a central opening 420 for containing the integrated circuit die 408 and a number of perimeter openings or vias 422 surrounding the central opening 420. The central opening 420 and the perimeter vias 422 extend through the core layer 402.

The first conductive layer 404 closes the central opening 420 and the perimeter vias 422 in the core layer 402, and forms a ground or thermal pad.

The second conductive layer 406 is processed to form ground or thermal terminals 440 and 442 with a number of signal terminals 444 in between. The ground or thermal terminals 440 extend through the central opening 420 of the core layer 402 to form a ground or thermal pad 446 in contact with the first conductive layer 404. This means that no additional processes or material are required for a silicon substrate backside ground. Similarly, the ground or thermal terminals 442 extend through the perimeter openings or vias 422 to form blind vias in contact with the first conductive layer 404. The second conductive layer 406 can be of a predetermined thickness 407, and when extending through the vias 422, can fold on itself, so that the fold of the second conductive layer 406 has substantially twice

the predetermined thickness 407 in the vias 422. It will also be understood from this disclosure that, if the first conductive layer 404 is patterned, the ground or thermal terminals 442 can be used as signal terminals.

THE INVENTION CLAIMED IS:

~~1. A method of manufacturing an integrated circuit package comprising:~~

~~forming a substrate including:~~

~~forming a core layer, and~~

~~forming vias in the core layer;~~

~~forming a conductive layer having a predetermined thickness on the core layer and having substantially twice the predetermined thickness in the vias; and~~

~~forming connections between an integrated circuit die and the conductive layer.~~

~~2. The method as claimed in claim 1 further comprising:~~

~~encapsulating the integrated circuit die with an encapsulant, the encapsulant extending into the vias.~~

~~3. The method as claimed in claim 1 further comprising:~~

~~forming terminals on the conductive layer of the predetermined thickness in the vias, the terminals having a shape of at least one of square, rectangular, and round.~~

~~4. The method as claimed in claim 1 further comprising:~~

~~forming terminals on the conductive layer of the predetermined thickness in the vias; and~~

~~forming solder balls connected to the terminals.~~

~~5. The method as claimed in claim 1 further comprising:~~

~~forming solder balls on the conductive layer on the core layer.~~

~~6.~~1. A method of manufacturing an integrated circuit package comprising:

forming a substrate including:

forming a core layer, and

forming vias in the core layer;

forming a conductive layer having a predetermined thickness on the core layer and having substantially twice the predetermined thickness in the vias;

forming connections between an integrated circuit die and the conductive layer; and

forming a solder mask over the core layer having openings therein to the conductive layer.

~~7.~~2. The method as claimed in claim ~~6~~1 wherein:

forming the solder mask includes forming the solder mask to extend into the vias.

~~8.~~3. The method as claimed in claim ~~6~~1 further comprising:

forming terminals on the conductive layer of the predetermined thickness in the vias, the terminals having a shape of at least one of square, rectangular, and round; and

forming a further solder mask over the core layer having openings therein to the terminals.

~~9.~~4. The method as claimed in claim ~~6~~1 further comprising:

forming terminals on the conductive layer of the predetermined thickness in the vias;

forming a further solder mask over the core layer having openings therein to the terminals; and

forming solder balls connected to the terminals through the futher solder mask.

~~10.~~5. The method as claimed in claim ~~6~~1 further comprising:

forming solder balls through the solder mask on the conductive layer on the core layer; and

forming the substrate includes forming an opening through the substrate.

~~11.~~6. An integrated circuit package comprising:

a substrate including a core layer having vias provided therein;

a conductive layer having a predetermined thickness on the core layer and having substantially twice the predetermined thickness in the vias;

an integrated circuit over the substrate; ~~and~~

connections between the integrated circuit die and the conductive layer; and

a solder mask formed over the core layer having openings therein to the conductive layer..

~~12.~~7. The package as claimed in claim ~~11~~6 further comprising:

an encapsulant encapsulating the integrated circuit die with the encapsulant extending into the vias.

~~13.~~8. The package as claimed in claim ~~11~~6 further comprising:

terminals on the conductive layer of the predetermined thickness in the vias, the terminals having a shape of at least one of square, rectangular, and round.

~~14.~~9. The package as claimed in claim ~~11~~6 further comprising:

terminals on the conductive layer of the predetermined thickness in the vias; and

solder balls connected to the terminals.

~~15.~~10. The package as claimed in claim ~~11~~6 further comprising:
solder balls on the conductive layer on the core layer.

~~16. The package as claimed in claim 11 further comprising:~~
~~a solder mask formed over the core layer having openings therein to the conductive layer.~~

~~17.~~11. The package as claimed in claim ~~1~~6 wherein:
the solder mask extends into the vias.

~~18.~~12. The package as claimed in claim ~~1~~6 further comprising:
terminals on the conductive layer of the predetermined thickness in the vias, the terminals having a shape of at least one of square, rectangular, and round; and
a further solder mask over the core layer having openings therein to the terminals.

~~19.~~13. The package as claimed in claim ~~1~~6 further comprising:
terminals on the conductive layer of the predetermined thickness in the vias;
a further solder mask over the core layer having openings therein to the terminals; and
solder balls connected to the terminals through the futher solder mask.

~~20.~~14. The package as claimed in claim ~~1~~6 further comprising:
solder balls through the solder mask on the conductive layer on the core layer; and
the substrate having an opening therethrough.

~~21. A method of manufacturing an integrated circuit package comprising:~~
~~forming a substrate including:~~
~~forming a core layer,~~
~~forming a through opening and vias in the core layer,~~
~~forming a first conductive layer on the core layer covering the through opening, and~~
~~forming a second conductive layer on the core layer opposite the first conductive layer, the second conductive layer formed in the through opening and in the vias contacting the first conductive layer;~~
~~bonding an integrated circuit die to the second conductive layer and in the through opening;~~

~~forming connections between the integrated circuit die and the second conductive layer; and~~

~~encapsulating the integrated circuit die and the connections.~~