WHAT IS CLAIMED IS:

1. An apparatus (100) for computing comprising:

at least one processing circuitry (110) configured for computing an outcome of executing a set of computer instructions comprising a group of data variables, by:

identifying (201) an initial state of the at least one processing circuitry;

identifying (405) at least one likely data value, where the at least one likely data value is at least one value of at least one of the group of data variables anticipated to be computed by executing the set of computer instructions and computed using one or more program data values of the set of computer instructions; and

configuring (420) the at least one processing circuitry for:

executing (203) at least part of a set of anticipated computer instructions produced according to a likely order of execution of the set of computer instructions predicted based on the set of computer instructions and the at least one likely data value~~, such that the set of anticipated computer instructions is not limited by an amount of branch instructions~~; and

when, while executing (203) the at least part of the set of anticipated computer instructions, identifying (210) a failed prediction where the at least one data variable is not equal to the at least one likely data value according to at least one data variable test:

restoring (211) the initial state of the at least one processing circuitry; and

executing (212) one of at least one set of alternative computer instructions, produced based on the set of computer instructions and the at least one likely data value.

2. The apparatus of claim 1, wherein the at least one processing circuitry is further configured for:

collecting (310) a plurality of statistical values comprising a plurality of data-statistic values indicative of one or more data values of the group of data variables while executing the set of computer instructions, and additionally or alternatively at least one branch-statistic value, indicative of a selected instruction executed in response to executing at least one branch instruction of the set of computer instructions; and

providing (320) the plurality of statistical values to at least one hardware processor for the purpose of identifying the at least one likely data value according to the plurality of statistical values.

3. The apparatus of claim 2, wherein the at least one processing circuitry comprises telemetry circuitry (112) for collecting at least one of the plurality of statistical values.

4. The apparatus of claim 2, wherein the set of computer instructions comprises at least one monitoring instruction for collecting at least one of the plurality of statistical values.

5. The apparatus of claim 1, wherein the at least one processing circuitry comprises a processing circuitry having a von Neumann architecture.

~~6. The apparatus of claim 5, wherein the at least one processing circuitry comprises at least one of: a central processing unit, a data processing unit (DPU), a multi-core central processing unit (CPU), a microcontroller unit (MCU) and an accelerated processing unit (ACU).~~

6~~7~~. The apparatus of claim 1, wherein the at least one processing circuitry comprises a processing circuitry having a non-von Neumann architecture.

~~8. The apparatus of claim 7, wherein the at least one processing circuitry comprises at least one of: a data processing unit (DPU), a field-programmable gate array (FPGA), a coarse-grained reconfigurable architecture (CGRA), a neural-network accelerator, an intelligence processing unit (IPU), an application-specific integrated circuit (ASIC), a quantum computer, and an interconnected computing grid, comprising a plurality of reconfigurable logical elements connected by a plurality of configurable data routing junctions.~~

7~~9~~. The apparatus of claim 1, wherein the at least one processing circuitry comprises a first processing circuitry and a second processing circuitry;

wherein the first processing circuitry is not the second processing circuitry;

wherein executing the at least part of the set of anticipated computer instructions is by the first processing circuitry; ~~and~~

wherein executing the set of alternative computer instructions is by the second processing circuitry;~~.~~

~~10. The apparatus of claim 9,~~ wherein identifying the initial state of the at least one processing circuitry comprises identifying a plurality of state values of the first processing circuitry; and

wherein restoring the initial state of the at least one processing circuitry comprises configuring the second processing circuitry according to the plurality of state values.

8~~11~~. The apparatus of claim 1, wherein the at least one processing circuitry has a set of supported instructions;

wherein the set of supported instructions comprises a restore instruction for configuring a state of the processing circuitry according to a previously known state of the processing circuitry; and

wherein restoring the initial state of the at least one processing circuitry comprises executing the restore instruction subject to identifying the failed prediction while executing the at least part of the set of anticipated computer instructions.

9~~12~~. A method for computing, comprising:

identifying (201) an initial state of at least one processing circuitry;

identifying (405) at least one likely data value, where the at least one likely data value is at least one value of at least one of a group of data variables of a set of computer instructions, anticipated to be computed by executing the set of computer instructions and computed using one or more program data values of the set of computer instructions; and

configuring (420) the at least one processing circuitry for:

executing (203) at least part of a set of anticipated computer instructions produced according to a likely order of execution of the set of computer instructions predicted based on the set of computer instructions and the at least one likely data value~~, such that the set of anticipated computer instructions is not limited by an amount of branch instructions~~; and

when, while executing (203) the at least part of the set of anticipated computer instructions, identifying (210) a failed prediction where the at least one data variable is not equal to the at least one likely data value according to at least one data variable test:

restoring (211) the initial state of the at least one processing circuitry; and

executing (212) one of at least one set of alternative computer instructions, produced based on the set of computer instructions and the at least one likely data value.

10~~3~~. An apparatus (100) for computing, comprising at least one hardware processor (101) adapted for:

identifying (405) at least one likely data value, where the at least one likely data value is at least one value of at least one of a group of data variables of a set of computer instructions, anticipated to be computed by executing the set of computer instructions and computed using one or more program data values of the set of computer instructions;

identifying (201) an initial state of at least one processing circuitry;

producing (410) a set of anticipated computer instructions and at least one set of alternative computer instructions, produced according to a likely order of execution of the set of computer instructions predicted based on the set of computer instructions and the at least one likely data value~~, such that the set of anticipated computer instructions is not limited by an amount of branch instructions~~; and

configuring (420) at least one processing circuitry to execute the set of computer instructions by:

executing (203) at least part of the set of anticipated computer instructions; and

when, while executing (203) the at least part of the set of anticipated computer instructions, identifying (210) a failed prediction where the at least one data variable is not equal to the at least one likely data value according to at least one data variable test:

restoring (211) the initial state of the at least one processing circuitry; and

executing (212) one of the at least one set of alternative computer instructions.

11~~4~~. The apparatus of claim 10~~3~~, wherein the at least one hardware processor is further configured for:

receiving (401), from at least one other hardware processor, a plurality of statistical values comprising a plurality of data-statistic values indicative of one or more data values of the group of data variables while executing the set of computer instructions and additionally or alternatively at least one branch-statistic value, indicative of a selected instruction executed in response to executing at least one branch instruction of the set of computer instructions; and

identifying the at least one likely data value according to the plurality of statistical values.

125. The apparatus of claim 103, wherein producing the set of anticipated computer instructions comprises adding to the set of anticipated computer instructions:

(501) at least one store instruction for storing the initial state of the at least one processing circuitry;

(503) the at least part of the set of anticipated computer instructions produced based on the set of computer instructions and the at least one likely data value;

(505) at least one state test instruction for identifying the failed prediction; and

(508) at least one restore instruction to restore the initial state of the at least one processing circuitry.

136. The apparatus of claim 125, wherein producing the at least part of the set of anticipated computer instructions comprises identifying in the set of computer instructions at least one set of tentative instructions, each associated with at least one local test instruction, such that each set of tentative instructions is anticipated to be executed subject to an outcome of the respective at least one local test instruction associated therewith; and

wherein the at least one state test instruction is produced according to the at least one local test instruction.

147. The apparatus of claim 114, wherein producing the set of anticipated computer instructions comprises:

identifying (601) in the set of computer instructions at least one loop of computer instructions;

identifying (603), according to the plurality of statistical values, an expected amount of iterations of the loop of computer instructions; and

generating (607) a rolled-out loop of instructions by repeating at least some of the loop of computer instructions the expected amount of iterations of the loop.

158. The apparatus of claim 147, wherein producing the set of anticipated computer instructions further comprises:

identifying (610) in the rolled-out loop of instructions a plurality of data-independent operations, where an expected outcome of executing the plurality of data-independent operations does not depend on modifying a runtime value of another of the group of data variables while executing the rolled-out loop of instructions; and

producing (620) the set of anticipated computer instructions according to the expected outcome.

169. The apparatus of claim 158, wherein producing the set of anticipated computer instructions according to the expected outcome further comprises:

identifying (701) in the rolled-out loop of instructions a plurality of memory access operations to a plurality of vector elements of a vector data variable of the set of computer instructions; and

replacing (705) the plurality of memory access operations with a single equivalent memory operation.

1720. The apparatus of claim 114, wherein producing the set of anticipated computer instructions comprises:

producing (620) a first set of anticipated computer instructions according to the expected outcome;

identifying (610) in the first set of anticipated computer instructions a plurality of other data-independent operations, where another expected outcome of executing the plurality of other data-independent operations does not depend on modifying another runtime value of yet another of the group of data variables while executing the first set of anticipated computer instructions; and

producing (620) a second set of anticipated computer instructions according to the other expected outcome.

1821. The apparatus of claim 114, wherein producing the set of anticipated computer instructions comprises:

producing (410) another first anticipated set of instructions based on the at least one likely data value;

identifying (405) according to the plurality of statistical values at least one other likely data value, where the at least one other likely data value is at least one other value of at least one other of the group of data variables anticipated while executing the other first anticipated set of instructions; and

producing (410) another second anticipated set of instructions based on the at least one other likely data value.

1922. The apparatus of claim 114, wherein configuring the at least one processing circuitry comprises at least one of:

computing (801) at least one anticipated data-flow graph according to the set of anticipated computer instructions; and

projecting (802) the at least one data-flow graph onto at least part of the at least one processing circuitry; and

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23. The apparatus of claim 14, wherein configuring the at least one processing circuitry comprises:

computing (810) at least one alternative data-flow graph according to at least one of the at least one set of alternative computer instructions; and

projecting (812) the at least one alternative data-flow graph onto at least another part of the at least one processing circuitry.

2024. A method for computing, comprising:

identifying (405) at least one likely data value, where the at least one likely data value is at least one value of at least one of a group of data variables of a set of computer instructions, anticipated to be computed by executing the set of computer instructions and computed using one or more program data values of the set of computer instructions;

identifying (201) an initial state of at least one processing circuitry;

producing (410) a set of anticipated computer instructions and at least one set of alternative computer instructions, produced according to a likely order of execution of the set of computer instructions predicted based on the set of computer instructions and the at least one likely data value, such that the set of anticipated computer instructions is not limited by an amount of branch instructions; and

configuring (420) at least one processing circuitry to execute the set of computer instructions by:

executing (203) at least part of the set of anticipated computer instructions; and

when, while executing (203) the at least part of the set of anticipated computer instructions, identifying (210) a failed prediction where the at least one data variable is not equal to the at least one likely data value according to at least one data variable test:

restoring (211) the initial state of the at least one processing circuitry; and

executing (212) one of the at least one set of alternative computer instructions.