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Method and Structure for Contact to Copper Metallization In an Insulating Via on a Semiconductor

Field of the Invention

This invention generally relates to contact to copper wiring on semiconductor components. More particularly, it relates to a process for providing intimate contact between the copper wiring and a next level of metallization while avoiding copper contamination of insulators. Even more particularly it relates to a process for removing copper oxide from a copper contact surface on an integrated circuit chip.

Background of the Invention

Copper wires provide significantly lower resistivity than conventional aluminum wires on integrated circuits and bring the promise of significantly higher speed chips. The wires on a chip are fabricated in patterned layers of metal separated by layers of insulator, the layers of insulator having windows or vias to selectively allow connection between the layers of metal. When copper is exposed to air when these vias are opened, copper oxide is likely to form on the copper. This copper oxide can provide a source of electrical resistance or even block electrical contact to the next layer of metal, and it therefore must be removed before that next metal is deposited.

Wet etchants, such as hydrofluoric acid have been used and are highly effective at removing copper oxide before metal deposition. But copper oxide can regrow quickly on the copper surface between the time of the HF treatment and subsequent metal deposition.

Argon sputter etching has been used to clean vias on semiconductor chips having aluminum metallization, effectively removing aluminum oxide in the same vacuum chamber used to then deposit the next layer of metal. This technique has also been used to remove copper oxide. Because exposure to an oxidizing environment is avoided between the oxide removal step and the deposition step the reoxidation problem has been avoided. But the present inventors recognized a problem that argon sputtering would generate for copper that was not a problem for aluminum, as described herein below.

Thus, a better solution is needed that provides for oxide-free interfaces between layers of metallization while protecting via sidewalls from splashed copper without additional processing steps, and this solution is provided by the following invention.

Summary of the Invention

It is therefore an object of the present invention to provide an alternative to argon sputter cleaning for removing oxide in vias that is suitable for copper metallized wafers.

It is still another object of the present invention to provide a process for removing copper oxide in a via in insulation on a semiconductor chip without splashing copper onto via sidewalls.

It is an advantage of the present invention that copper oxide is removed without additional processing steps to protect the copper or via sidewalls prior to oxide removal.

These and other objects, features, and advantages of the invention are accomplished by a method of processing a semiconductor wafer having copper

metallization, comprising the steps of: providing the wafer having a patterned copper layer and an insulating layer on said copper layer; providing a via in said insulating layer wherein a copper oxide may have formed on copper exposed in said via; providing said wafer in a chamber; providing a reducing environment in said chamber to reduce said copper oxide to elemental copper; and without exposing the wafer to an oxidizing environment depositing a conductor in said via.

In an alternative, the invention is a semiconductor structure, comprising: a patterned copper layer; an insulating layer on said copper layer; a via in said insulating layer to said copper layer, said via comprising sidewalls formed of said insulating layer; and a conductive liner contacting an elemental copper surface of said copper layer in said via, said conductive liner further coating said sidewalls, wherein said liner provides a barrier to copper diffusion, there being no copper directly contacting said sidewalls.

Brief Description of the Drawings

FIG. 1a is a cross sectional view of a via in a wafer having a copper metal wire after sputter etching to clean copper oxide from the surface of the copper metal, showing the problem of copper splashing recognized by the present inventors.

FIG. 1b is a cross sectional view of the method of protecting sidewalls from copper splashing provided in US patent application 08/858,139.

FIGS. 2a-2f are cross sectional views showing the process steps of the present invention.

FIG. 3a-3c are cross sectional views of chambers used to process wafers of the present invention.

FIG. 4 is a cross sectional view of a dual damascene structure encompassing the present invention.

FIG. 5 is a cross sectional view of a slanted wall via structure encompassing the present invention.

Description of the Invention

The present inventors recognized that sputter etching would splatter copper onto sidewalls of each via, contaminating via sidewalls with unwanted copper as shown in FIG. 1a. The present inventors also recognized that copper splattered on unprotected sidewalls could then migrate through the insulator, reducing its effectiveness as an insulator, or the copper could migrate to the silicon level and cause gate oxide leakage, reduce gate oxide reliability, or cause junction leakage.

Commonly assigned US patent application 08/858,139, to Geffken et al. addresses the copper splatter problem, as shown in FIG. 1b, by providing barrier material 5 over the copper oxide at the bottom of the via and along via sidewalls 6 to protect those sidewalls from copper splash during the argon sputtering step. Barrier material 5 can be a thin layer of tantalum, tantalum nitride, tungsten nitride, tungsten silicon nitride, tantalum silicon nitride, titanium silicon nitride, or silicon nitride. In the process, after via 6 is opened barrier material 5 is deposited. Barrier material 5 is then directionally etched to remove barrier material 5 from horizontal surfaces. The directional etch removes both the barrier

material and copper oxide thereby exposed. A sputter etching step can also be performed to open contact to elemental copper wire 3. During the directional etching or sputter etching step barrier material 5 is effective to protect sidewalls 6 from contact with copper that splashes up. However, this process involves an additional deposition and directional etch step, which adds cost to the process.

The present invention addresses the splatter problem by eliminating argon sputtering; in the present invention copper oxide is chemically reduced to a pristine copper surface. The wafers with reduced copper in vias are then presented for the next metal deposition without exposure to an oxidizing ambient. The chemical reaction to reduce copper does not involve any mechanical action, as in argon sputtering, that can splash copper along insulating sidewalls. Thus, additional process steps to provide a sidewall protective layer are not needed during the reduction step. In addition, because reoxidation is avoided, additional process steps to protect the copper surface are not needed.

In the first step, an electronic component is provided, such as semiconductor wafer 20, having copper layer 22 and insulating layer 24, as shown in FIG. 2a. Insulating layer 24 is formed of silicon dioxide or a polymer. Silicon dioxide is deposited by a method such as CVD or plasma enhanced CVD. Insulating layer 24 can also be formed of a material that can be spun on and cured, such as spun on glass or an organic polymer. An insulator, such as silicon dioxide can contain dopants like phosphorous or boron. Polymers include such materials as polyimide and hydrogen silsequioxane.

Via 26 having sidewall 26' is then formed in insulating layer 24 using standard photolithographic patterning and an etch, such as a wet etch or a plasma etch as shown in FIG. 2b. Vias 26 can have either tapered sidewalls for conventional interconnection or vertical sidewalls for stud interconnects using single or dual damascene processes, well

known in the art. No particular attention need be paid to avoiding oxidation of the copper surface exposed after via 26 is formed. Thus, thin copper oxide layer 28 is likely to form on copper wire 22 where copper is exposed in via 26.

In the next step, wafer 20 is provided in processing chamber 30 and provided with reducing environment 32 to reduce copper oxide 28 that may have formed in via 26, as illustrated in FIGS. 2c and 3a. Copper oxide 28 is reduced to provide elemental copper surface 22'.

In the reducing process, copper oxide 28 is chemically reduced using a reducing gas, such as H_2, forming gas (N_2 and H_2), NO_x, or CO. Atomic hydrogen or hydrogen ions may also be used. Pure hydrogen at a pressure in the range of about 10T to about 760T is provided at 350°C for a time in the range from about 1 to about 10 minutes to reduce the copper oxide and leave elemental copper surface 22'. Higher pressures, at least in the range of 500T have been found to work better than lower pressures. Good results were obtained in about 4 minutes with 500T. Water, a byproduct of the reduction reaction, boils off and is pumped away. Alternatively, a plasma of H_2 or a plasma with H_2 and a carrier like He or Ar can be used to provide hydrogen ions.

In the next step, wafer 20 is moved out of chamber 30 and into transport chamber 34 having vacuum environment 36 using wafer handler 37, as shown in FIG. 3b. Wafer 20 is then moved to processing chamber 40 having vacuum environment 42 for sputter deposition of the next conductor without exposing the component to an oxidizing environment, as shown in FIG. 3c. To accomplish the transfer, chamber 30 is first pumped down and evacuated. Wafer 20 is then moved to transport chamber 34 and then to chamber 40 in vacuum for metal deposition at a pressure in the mT range. Chamber 30, used for the reducing step is connected with chamber 40, used for the metal deposition

step, so that wafer 20 can be moved from one to the other without being exposed to an oxidizing environment. It is, of course, also possible to provide the reducing environment and the metal deposition in a single chamber and to do the reducing step and deposition step sequentially in this single chamber.

In chamber 40 conductor 50 is deposited in contact with elemental copper surface 22' in via 26 as shown in FIG. 2d-2e. If conductor 50 is another copper wiring level then conductor 50 is formed of at least two parts, thin liner 52 and copper 54. Thin liner 52, selected to provide adhesion and to stop copper diffusion, is deposited first to coat elemental copper surface 22' and protect sidewalls 26' from contact with copper 54, as more fully described in commonly assigned US Patent 5,676,587, to Landers et al., and US patent 5,695,810, both incorporated herein by reference, and illustrated in FIG. 2d. Thin liner 52, generally not more than 1000A thick, comprises thin films of titanium and titanium nitride disposed over one another to form a Ti/TN stack, or tantalum and tantalum nitride to form a Ta/TaN stack or Ta. Such a liner is deposited by physical vapor deposition, otherwise known as sputter deposition, or it may be deposited by chemical vapor deposition to form a more conformal coating. Then copper 54 is deposited on liner 52 to fill via 26, as shown in FIG. 2e.

The invention is particularly useful where the patterning of copper layers is by the damascene technique in which conductor 54 is deposited to fill grooves in insulating layer 24 and liner 52, and then wafer 20 is polished to planarize conductor 54 and liner 52 to surface 24' of insulating layer 24. It is equally useful where the patterning of copper is by a dual damascene technique as shown in FIG. 4. This process follows the sequence of FIGS. 2a-2f except both studs 60 and wiring channels 62 are opened in insulating layer 24 in two masking and etching steps before the reducing step of FIG. 2c and the liner deposition step of FIG. 2d.

In addition, the invention is advantageous for vias 26 having slanted sidewalls 26" as shown in FIG. 5. The process of the 08, 858,139 patent application would not be applicable in this case since the directional etch step would remove liner 5, 52 from slanted sidewall surfaces. In the present invention, no directional etch step need be performed; liner 52 remains in place on horizontal, vertical, and slanted surfaces. After copper 54 is deposited it is patterned and etched to provide copper wire 70 making contact to wire 22 through via 26" in insulator 24.

While several embodiments of the invention, together with modifications thereof, have been described in detail herein and illustrated in the accompanying drawings, it will be evident that various further modifications are possible without departing from the scope of the invention. Nothing in the above specification is intended to limit the invention more narrowly than the appended claims. The examples given are intended only to be illustrative rather than exclusive.



CLAIMS

1. A method of processing a semiconductor wafer having copper metallization, comprising the steps of:

   a) providing the wafer having a patterned copper layer and an insulating layer on said copper layer;

   b) providing a via in said insulating layer wherein a copper oxide may have formed on copper exposed in said via;

   c) providing said wafer in a chamber;

   d) providing a reducing environment in said chamber to reduce said copper oxide to elemental copper; and

   e) without exposing the wafer to an oxidizing environment depositing a conductor in said via.

2. The method as recited in claim 1, wherein said conductor of said step (e) comprises a thin liner, said thin liner for providing a barrier to copper diffusion,

3. The method as recited in claim 2, wherein said thin liner is deposited along sidewalls of said via.

4. The method as recited in claim 3, said thin liner comprises one of tantalum, tantalum nitride, titanium, titanium nitride, tantalum silicon nitride and tungsten nitride.

5. The method as recited in claim 2, wherein said thin liner is deposited on said elemental copper.

6. The method as recited in claim 2, further comprising the step of depositing a conductor on said liner to fill said via.

7. The method as recited in claim 6, further comprising the step of polishing said conductor stopping on said insulator.

8. The method as recited in claim 2, wherein said conductor comprises copper.

9. The method as recited in claim 1, wherein said insulating layer of said step (a) comprises silicon dioxide.

10. The method as recited in claim 1, wherein said insulating layer of said step (a) comprises a polymer.

11. The method as recited in claim 10, wherein said polymer comprises polyimide.

12. The method as recited in claim 1, wherein said reducing environment of said step (d) comprises hydrogen.

13. The method as recited in claim 1, wherein said reducing environment of said step (d) comprises hydrogen ions.

14. The method as recited in claim 1, wherein said reducing environment of said step (d) comprises carbon monoxide.

15. The method as recited in claim 1, wherein said reducing environment of said step (d) comprises NO_x.

16. The method as recited in claim 1, wherein said depositing step (e) is performed in said chamber of said step (c).

17. The method as recited in claim 1, wherein said depositing step (e) is performed in a second chamber.

18. The method as recited in claim 1, wherein said depositing step (e) is performed after moving said wafer from said chamber of said step (c) to said second chamber through a transport chamber.

19. A semiconductor structure, comprising:

a patterned copper layer;

an insulating layer on said copper layer;

a via in said insulating layer to said copper layer, said via comprising sidewalls formed of said insulating layer; and

a conductive liner coating an elemental copper surface of said copper layer in said via, said conductive liner further coating said sidewalls, wherein said liner provides a barrier to copper diffusion, there being no copper directly contacting said sidewalls.

20. The structure as recited in claim 19, wherein said thin liner comprises one of tantalum, tantalum nitride, titanium, titanium nitride, tantalum silicon nitride and tungsten nitride.

21. The structure as recited in claim 19, further comprising a conductor on said liner filling said via.

22. The structure as recited in claim 21, wherein said conductor is planar with said insulating layer.

23. The structure as recited in claim 19, wherein said insulating layer comprises silicon dioxide.

24. The structure as recited in claim 19, wherein said insulating layer comprises a polymer.

25. The structure as recited in claim 24, wherein said polymer comprises polyimide.

26. The structure as recited in claim 19, wherein said via comprises slanted sidewalls.

27. The structure as recited in claim 19, wherein said via comprises vertical sidewalls.

28. The structure as recited in claim 27, wherein said via comprises both vertical and horizontal sidewalls.