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ABSTRACT



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A Clock Switching Circuit

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A clock switching circuit 10 for switching between a first clock signal, CLK A, and a second clock signal, CLK B, without generating a glitch at the output is described herein. The clock switching circuit 10 comprises a first flip-flop 20 arranged to receive a CLK SEL signal, a second flip-flop 30 cascaded with the first flip-flop 20, a multiplexer 40 arranged to receive the first clock signal CLK A and the second clock signal CLK B, an XNOR gate 50 and an AND gate 60 having an output providing the first clock signal. When the CLK SEL signal is detected by the first flip-flop which includes an indication to switch from the first clock signal CLK A to the second clock signal CLK B, the output of the AND gate switches from the first clock signal CLK A to an intermediate state and subsequently to the second clock signal, such that the switching from the intermediate state to the second clock signal is synchronised to a falling edge of the second clock signal.

20 Figure 1