CLAIMS

1. A semiconductor memory device comprising:

a plurality of planes including a plurality of blocks each being a set of memory cells;

a sequencer which executes a first operation and a second operation shorter than the first operation; and

a voltage generator which includes first and second driver modules, wherein

upon receiving a first command set that instructs execution of the first operation, the sequencer executes the first operation, and upon receiving a second command set that instructs execution of the second operation while the first operation is being executed, the sequencer suspends the first operation and executes the second operation or executes the second operation in parallel with the first operation, based on an address of a block that is a target of the first operation and an address of a block that is a target of the second operation,

the plurality of planes includes a first plane and a second plane to which power is supplied from the first driver module, and a third plane and a fourth plane to which power is supplied from the second driver module,

the sequencer is, while executing a first operation targeted at a block included in the first plane, configured to:

suspend the first operation and execute the second operation upon receiving a second command set targeted at a block included in the first plane; and

execute the second operation in parallel with the first operation upon receiving a second command set targeted at a block included in one of the second plane, the third plane, or the fourth plane,

the plurality of planes further includes a fifth plane to which power is supplied from the first driver module and which shares a part of a power-supply circuit with the first plane, and

upon receiving a second command set targeted at a block included in the fifth plane while executing a first operation targeted at a block included in the first plane, the sequencer suspends the first operation, and executes the second operation.

2. The semiconductor memory device according to claim 1, wherein

the first operation is an erase operation, and

the second operation is a read operation.

3. The semiconductor memory device according to claim 2, wherein

a timing at which the sequencer executes the second operation upon receiving the second command set while the

first operation is being executed changes based on a timing at which the second command is received.

4. The semiconductor memory device comprising:

a plurality of planes including a plurality of blocks each being a set of memory cells;

a sequencer which executes a first operation and a second operation shorter than the first operation;

a voltage generator which includes first and second driver modules; and

a plurality of well lines respectively provided in a plurality of planes, wherein

upon receiving a first command set that instructs execution of the first operation, the sequencer executes the first operation, and upon receiving a second command set that instructs execution of the second operation while the first operation is being executed, the sequencer suspends the first operation and executes the second operation or executes the second operation in parallel with the first operation, based on an address of a block that is a target of the first operation and an address of a block that is a target of the second operation,

the plurality of planes includes a first plane and a second plane to which power is supplied from the first driver module, and a third plane and a fourth plane to which power is supplied from the second driver module,

the sequencer is, while executing a first operation targeted at a block included in the first plane, configured to:

suspend the first operation and execute the second operation upon receiving a second command set targeted at a block included in the first plane; and

execute the second operation in parallel with the first operation upon receiving a second command set targeted at a block included in one of the second plane, the third plane, or the fourth plane,

the first operation is an erase operation,

the second operation is a read operation,

a timing at which the sequencer executes the second operation upon receiving the second command set while the first operation is being executed changes based on a timing at which the second command is received,

the block includes a plurality of string units,

the erase operation includes:

a voltage rise period in which a voltage of a well line corresponding to a block in which the first or second driver module has been selected rises from a first voltage to an erase voltage;

an erase period in which the erase voltage is applied to the corresponding well line by the first or second driver module;

a voltage drop period in which a voltage of the corresponding well line is dropped from the erase

voltage to the first voltage by the first or second driver module; and

an erase verify period in which the sequencer executes an erase verify in units of string units, and

the timing at which the sequencer executes the second operation upon receiving the second command set for a block included in the second plane while the first operation for a block included in the first plane is being executed differs according to which of the voltage rise period, the erase period, the voltage drop period, and the erase verify period the second command set has been received.

5. The semiconductor memory device according to claim 4, wherein

upon receiving a second command set targeted at a block included in the second plane during the voltage rise period when a first operation targeted at a block included in the first plane is being executed, the sequencer stops raising the voltage of the corresponding well line and executes the second operation and resumes raising the voltage of the corresponding well line after the second operation has ended.

6. The semiconductor memory device according to claim 4, wherein upon receiving a second command set targeted at a block included in the second plane during the voltage rise period when a first operation targeted at a block

included in the first plane is being executed, the sequencer starts the second operation based on the voltage rise period having ended.

7. The semiconductor memory device according to claim 4, wherein, when a first operation targeted at a block included in the first plane is being executed,

the first driver module steps up the erase voltage and applies the stepped-up voltage to the corresponding well line during the erase period, and

upon receiving a second command set targeted at a block included in the second plane during the erase period, the sequencer stops stepping up the erase voltage to be applied to the corresponding well line, and executes the second operation, and resumes stepping up the erase voltage after the second operation has ended.

8. The semiconductor memory device according to claim 4, wherein

upon receiving a second command set targeted at a block included in the second plane during the erase period when a first operation targeted at a block included in the first plane is being executed, the sequencer starts the second operation based on the erase period having ended.

9. The semiconductor memory device according to claim 4, wherein

upon receiving a second command set targeted at a block included in the second plane during the voltage drop period when a first operation targeted at a block included in the first plane is being executed, the sequencer starts the second operation based on the voltage drop period having ended.

10. The semiconductor memory device according to claim 4, wherein

upon receiving a second command set targeted at a block included in the second plane during the erase verify period when a first operation targeted at a block included in the first plane is being executed, the sequencer suspends, based on a determination operation in an erase verify that is executed in units of string units having ended, the erase verify and starts the second operation, and resumes the erase verify on a subsequent string unit after the second operation has ended.

11. The semiconductor memory device according to claim 4, wherein

upon receiving a second command set targeted at a block included in the first plane during the erase period when a first operation targeted at a block included in the first plane is being executed, the sequencer drops the voltage of the corresponding well line from the erase

voltage to the first voltage and starts the second operation.

12. The semiconductor memory device according to claim 11, wherein

the first driver module raises the voltage of the corresponding well line from the first voltage to the erase voltage again after the second operation has ended.

13. The semiconductor memory device according to claim 4, wherein

upon receiving a second command set targeted at a block included in the first plane during the erase verify period when a first operation targeted at a block included in the first plane is being executed, the sequencer suspends an erase verify that is executed in units of string units and starts the second operation, and executes the suspended erase verify of the string unit from a start after the second operation has ended.

14. The semiconductor memory device according to claim 2, wherein

the first operation is resumed regardless of an instruction from an external memory controller after data read by the second operation has been output.

15. The semiconductor memory device according to claim 2, wherein

the first operation is resumed based on a command that has been externally received, after data read by the second operation has been output.

16. The semiconductor memory device according to claim 4, wherein

upon receiving the first command set, the sequencer causes the semiconductor memory device to transition from a ready state to a busy state and starts the first operation, and causes the semiconductor memory device to transition from the busy state to the ready state after starting the first operation and progresses with the first operation in the ready state.

17. The semiconductor memory device according to claim 16, wherein

upon receiving the second command set while executing the first operation, the sequencer causes the semiconductor memory device to transition from a ready state to a busy state and starts the second operation, and causes the semiconductor memory device to transition from the busy state to the ready state after the second operation has ended.

18. The semiconductor memory device according to claim 16, wherein the sequencer is configured to:

cause the semiconductor memory device to transition from the ready state to the busy state after receiving the second command set while executing the first operation,

if the second command set includes a first command, suspend the first operation and start the second operation before the first operation completes, and causes the semiconductor memory device to transition from the busy state to the ready state after the second operation has ended, and

if the second command set includes a second command different from the first command, continue the first operation and start the second operation after the first operation has completed, and cause the semiconductor memory device to transition from the busy state to the ready state after the second operation has ended.