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(54) IMPROVEMENTS IN SEMICONDUCTOR PROTECTIVE ELEMENTS

(71) We, HITACHI LIMITED, of 1—5—1 Marunouchi, Chiyoda-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to semiconductor protective elements, and more particulary to a protective element for preventing electrostatic puncture in a semiconductor integrated circuit.

One known method of preventing the electrostatic puncture of a semiconductor integrated circuit (IC) is illustrated in Figure 3 of the accompanying drawings. As shown a resistor R is connected on the input side and in series with an integrated circuit 7. The waveform of a surge pulse is smoothed by the time constant between a stray capacitance C and the resistor R, so as to prevent the abrupt surge pulse from entering the integrated circuit 7.

A second known method is shown in Figure 4 of the accompanying drawings, in which a diode D is connected on the input side of and in parallel with the integrated circuit 7. The diode D breaks down when the surge pulse is received and thus prevents it from reaching the circuit 7.

Regarding the former case, it has been observed that in the case where the resistor consists of a P-type region which is formed in an N-type semiconductor substrate, when a forward surge pulse is applied to the P—N junction between the substrate and the P-type region, that is, a positive potential is applied to the resistor, the resistor does not puncture, whereas when a large surge pulse is applied in the reverse direction, the resistor itself punctures if the voltage magnitude of the pulse exceeds the voltage which the P—N junction can withstand.

Regarding the latter case, it has frequently occurred that with reverse voltages which exceed the voltage which the junction of the diode can withstand, the diode itself punctures.

For these reasons, the prior-art protective elements are not satisfactory because they themselves are not sufficiently strong to withstand the surge voltages. For example, they have been punctured by a surge pulse of a reverse voltage of one hundred and several tens of volts from an external terminal.

Thus, they have been punctured when a reverse surge pulse of a voltage exceeding 100 to 130 volts has been applied to them and it has previously been impossible to make an integrated circuit which can withstand a reverse voltage of over 100 volts.

Consequently, integrated circuits can easily be permanently punctured even by electrostatic energy stored in the human body.

Particularly in the case where an integrated circuit is used in an electric circuit which generates a high voltage such as in a television circuit or automobile ignition, a surge pulse of 250 V, 500 V or higher can be impressed on the circuit, with the result that the integrated circuit is liable to be punctured.

We have found that where a forward surge pulse is applied to the P—N junction of a semiconductor, it does not puncture the semiconductor even when the surge voltage reaches a magnitude of several hundreds of volts, whereas where a reverse surge pulse is applied, it punctures the semiconductor at a relatively low voltage of between 100 and 130 volts.

The reason for this is not definitely known, but the phenomenon is considered to be attributed to the fact that where a high reverse bias voltage is suddenly applied, currents are locally concentrated when a high voltage is applied on both the sides of a depletion layer before the occurrence of breakdown.

We have therefore sought to connect an element of the transistor structure in parallel with the input terminal of the circuit to-be-protected in an integrated circuit substrate so as to spuriously effect the forward operation, whereby when a surge pulse in either the forward or reverse direction enters, the element portion is caused to operate as a transistor to absorb the surge pulse.

It is therefore an object of the present invention to provide a puncture preventing element which is difficult to puncture against surge pulses in both the forward and reverse directions.

According to the present invention there is provided a semiconductor protective element connected across the input terminals of an integrated circuit for preventing the electrostatic puncture thereof, said element having a semiconductor substrate of first conductivity type, a second conductivity type region selectively formed in the surface of the substrate, a first conductivity type region selectively formed in the surface of the second conductivity type region, said first and second conductivity type regions being partially short-circuited in order that the element can operate as a bipolar transistor in the case where a surge pulse voltage of at least one polarity is applied between the substrate and the first conductivity type region.

The present invention will now be described in greater detail by way of example with reference to the remaining figures of the accompanying drawings, wherein:—

Figures 1*a* to 1*c* are sectional views of one preferred type of semiconductor protective element; and

Figures 2*a* to 2*c* are sectional views of a second type of semiconductor protective element.

The protective element shown in Figure 1 includes an N-type semiconductor substrate 1, a P-type doped layer 2 selectively formed in the surface of the substrate 1, which layer is formed simultaneously with the base region of an N—P—N transistor (not shown). An N-type doped layer 3 is selectively formed in the surface portion of the P-type doped layer 2, which layer 3 is formed simultaneously with the emitter region of the N—P—N transistor (not shown).

A silicon dioxide film 4 protects a part of the semiconductor surface. An interconnection film 5 connects the input terminal side and one end of the N-type doped layer 3, whilst an interconnection film 6 connects the input side of an integrated circuit and the other end of the N-type doped layer 3 as well as the one end of the P-type doped layer 2.

In normal use, an input signal is fed in the direction of arrow, that is, from the interconnection film 5 through the interior of the N-type doped layer 3 via the interconnection film 6 to the input side of the circuit.

However, where a negative polarity surge pulse enters the input terminal, the situation becomes as is shown in Figure 1*b*. Whilst a surge current is passing through the N-type doped layer 3 in order to reach the interconnection film 6, a voltage drop arises due to the internal resistance of the doped layer 3. Thus, through the N-type doped layer 3, the electric potential differs, whereas the potential of the P-type doped layer 2 is at a negative value which is equal to the highest potential in the N-type doped layer 3 since the P-type doped layer 2 and the N-type doped layer 3 are short-circuited. For this reason, directly under the interconnection film 5 in a zone A depicted in Figure 1*b*, a forward bias potential exists at the P—N junction between the N-type doped layer 3 and the P-type doped layer 2. On the other hand, a reverse bias voltage is impressed between the N-type semiconductor substrate 1 and the P-type doped layer 2. Such a puncture element thereby becomes similar to an N—P—N transistor with the P-type doped layer 2 the base, the N-type doped layer 3 the emitter and the N-type semiconductor substrate 1 the collector. In particular, the current flows in such manner that the injection of electrons arises at and around the zone A in Figure 1*b*, whereby the surge pulse can be absorbed to prevent the surge from entering the input circuit. Since any surge voltage in the reverse direction is not directly exerted on one P—N junction portion, the puncture preventing element is not affected and can withstand a reverse surge pulse of approximately 1,000 volts.

Where a forward surge pulse enters the input terminal, the situation is shown in Figure 1*c*. Also in this case, whilst a surge current advances inside the N-type doped layer 3, the voltage drops, and eventually a reverse bias potential exists in the P—N junction portion in the zone A and in the vicinity thereof. On the other hand, the semiconductor substrate 1 is at a negative potential, so that a forward voltage is applied between the P-type doped layer 2 and the semiconductor substrate 1.

Consequently, the semiconductor substrate 1 becomes the emitter, the P-type doped layer 2 becomes the base and the N-type doped layer 3 becomes the collector of a transistor. Thus, the forward surge pulse causes current to flow in such manner that

electrons are injected from the substrate 1 to the P-type doped layer 2, whereby the surge pulse can be absorbed.

Therefore, regardless of whether the surge pulse is positive or negative going, it can be absorbed by the above described protective element.

Referring now to the second embodiment shown in Figure 2*a* the semiconductor protective element is constructed such that an electrode is led from that part of the P—N junction portion between a P-type doped layer 2 and an N-type doped layer 3 which is exposed at the semiconductor surface. Also the electrode and the substrate 1 are connected on the input side and in parallel with the circuit.

Where a reverse surge pulse enters at the input terminal, the situation becomes as shown in Figure 2*b*.

More specifically, the element does not operate as a transistor from the beginning in this case, but since a leakage current flows, the N-type doped layer 3 reaches the lowest negative potential, the P-type doped layer subsequently reaches a negative potential higher that it, and an N-type substrate 1 reaches a positive potential. Accordingly, a forward bias is impressed between the N-type doped layer 3 and the P-type doped layer 2, whilst a reverse bias is impressed between the P-type doped layer 2 and the N-type substrate 1.

Consequently, the N-type doped layer 3 becomes the emitter, the P-type doped layer 2 becomes the base and the N-type semiconductor substrate 1 becomes the collector. The injection of electrons arises from the N-type doped layer 3 being the emitter, so that the element operates as a transistor. The surge pulse is thus absorbed.

Where a forward surge pulse enters at the input terminal, a forward bias occurs between the N-type semiconductor substrate 1 and the P-type doped layer 2 as is illustrated in Figure 2*c*, so that the element operates as a diode and can absorb the surge pulse.

As in the first embodiment, when the surge pulse in either the forward or reverse direction is applied, it can be absorbed, and the puncture of the integrated circuit can be prevented.

WHAT WE CLAIM IS:—

1. A semiconductor protective element connected across the input terminals of an integrated circuit for preventing the electrostatic puncture thereof, said element having a semiconductor substrate of first conductivity type, a second conductivity type region selectively formed in the surface of the substrate, a first conductivity type region selectively formed in the surface of the second conductivity type region, said first and second conductivity type regions being partially short-circuited in order that the element can operate as a bipolar transistor in the case where a surge pulse voltage of at least one polarity is applied between the substrate and the first conductivity type region.

2. A semiconductor protective element according to claim 1, wherein said semiconductor substrate is of the N-type.

3. A semiconductor protective element according to claim 1 or 2, wherein a silicon dioxide film protects at least part of the semiconductor surface in the area of the first conductivity type region.

4. A semiconductor protective element according to claim 3, wherein interconnection films connect the first conductivity type region in series with the input terminals of the semiconductor integrated circuit to be protected.

5. A semiconductor protective element for preventing the electrostatic puncture of an integrated circuit, constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figure 1 or Figure 2 of the accompanying drawings.

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Consequently, the N-type doped layer 3 becomes the emitter, the P-type doped layer 2 becomes the base and the N-type semiconductor substrate 1 becomes the collector. The injection of electrons arises from the N-type doped layer 3 being the emitter, so that the element operates as a transistor. The surge pulse is thus absorbed.

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