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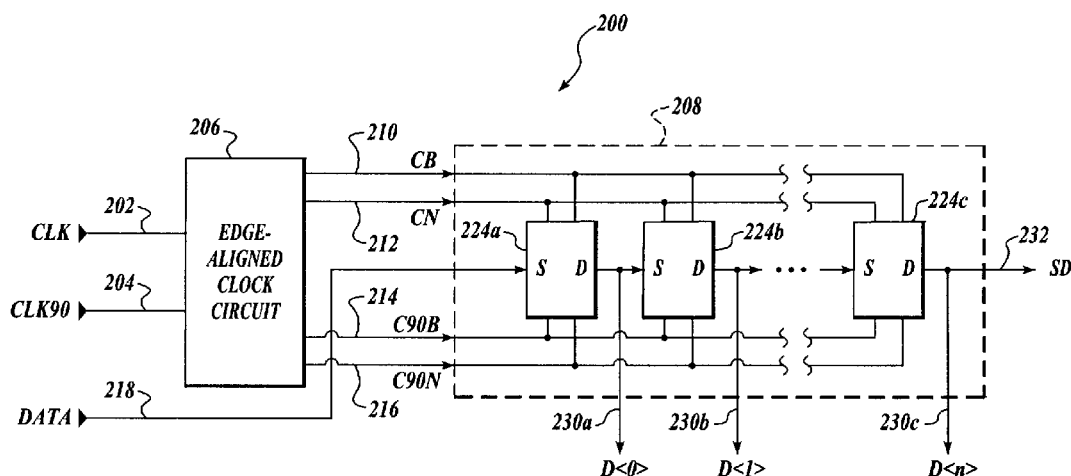
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(54) Title: **BALANCED DUAL-EDGE TRIGGERED DATA BIT SHIFTING CIRCUIT AND METHOD**



(57) Abstract: A balanced dual-edge triggered bit shifting circuit (200) includes a clock circuit (206) to generate low skew, or edge-aligned, complementary clock signals, and a shift register (208) that shifts a data bit in response to the complementary clock signals.