ABSTRACT

FULLY SILICIDED NMOS DEVICE FOR ELECTROSTATIC DISCHARGE PROTECTION

A device and method are described for forming a grounded gate NMOS (GGNMOS) device used to provide protection against electrostatic discharge (ESD) in an integrated circuit (IC). The device is achieved by adding n-wells below the source and drain regions. By tailoring the dopant concentration profiles of the p-well and n-wells provided in the fabrication process, peak dopant concentrations are moved below the silicon surface. This moves ESD conduction deeper into the IC where thermal conductivity is improved, thereby avoiding thermal damage occurring with surface conduction. The device does not require a salicidation block or additional implantation and uses standard NMOS fabrication processing steps, making it advantageous over prior art solutions.

FIGURE 4

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