CLAIMS

1. A method of maintaining a state of a memory cell without interrupting access to said memory cell, said method comprising:

applying a back bias to the cell to offset charge leakage out of a floating body of the cell, wherein a charge level of the floating body indicates a state of the memory cell; and

accessing the cell.

2. The method of claim 1, wherein said applying comprises applying said back bias to a terminal of said cell that is not used for address selection of said cell.

3. The method of claim 1, wherein said back bias is applied as a constant positive voltage bias.

4. The method of claim 1, wherein said back bias is applied as a periodic pulse of positive voltage.

5. The method of claim 1, wherein a maximum potential that can be stored in said floating body is increased by said applying back bias to the cell, resulting in a relatively larger memory window.

6. The method of claim 1, wherein said application of back bias performs a holding operation on said cell, said method further comprises simultaneously performing a read operation on said cell at the same time that said holding operation is being performed.

7. A method of operating a memory array having rows and columns of memory cells assembled into an array of said memory cells, each said memory cell having a floating body region for storing data; the method comprising:

performing a holding operation on at least all of said cells not aligned in a row or column of a selected cell; and

accessing said selected cell and performing a read or write operation on said selected cell while performing said hold operation on said at least all of said cells not aligned in a row or column of said selected cell.

8. The method of claim 7, wherein said performing a holding operation comprises performing said holding operation on all of said cells and wherein said performing a read or write operation comprises performing a read operation on said selected cell.

9. The method of claim 7, wherein said holding operation is performed by applying back bias to a terminal not used for memory address selection.

10. The method of claim 9, wherein said terminal is segmented to allow independent control of the applied back bias to a selected portion of the memory array.

11. The method of claim 7, wherein said performing a holding operation comprises performing said holding operation on all of said cells except for said selected cell, and wherein said performing a read or write operation comprises performing a write “0” operation on said selected cell, wherein a write “0” operation is also performed on all of said cells sharing a common source line terminal with said selected cell during said performing a write“0” operation.

12. The method of claim 7, comprising an individual bit write “0” operation, wherein said performing a holding operation comprises performing said holding operation on all of said cells except for said selected cell, while said performing a read or write operation comprises performing a write “0” operation on said selected cell.

13. The method of claim 7, wherein said performing a holding operation comprises performing said holding operation on all of said cells except for said selected cell while said performing a read or write operation comprises performing a write “1” operation on said selected cell.

14. The method of claim 7, wherein said performing a holding operation comprises performing said holding operation on all of said cells except for said selected cell while said performing a read or write operation comprises performing a multi-level write operation on said selected cell, using an alternating write and verify algorithm.

15. The method of claim 7, wherein said performing a holding operation comprises performing said holding operation on all of said cells except for said selected cell while said performing a read or write operation comprises performing a single-level or multi-level write operation on said selected cell, wherein said single-level and each level of said multi-level write operation includes: ramping a voltage applied to said selected cell to perform said write operation; reading the state of said selected cell by monitoring a change in current toward an addressable terminal of said selected cell; and verifying a state of said write operation using a reference memory cell.

16. The method of claim 15, further comprising configuring a state of said reference memory cell using a write-then-verify operation, prior to performing said write operation.

17. The method of claim 15, wherein said configuring a state of said reference memory cell comprises configuring said state upon power up of said memory array.

18. A method of operating a memory array having rows and columns of memory cells assembled into an array of said memory cells, each said memory cell having a floating body region for storing data; the method comprising:

refreshing a state of at least one of said memory cells; and

accessing at least one other of said memory cells, wherein access of said at least one other of said memory cells in not interrupted by said refreshing, and wherein said refreshing is performed without alternating read and write operations.

CLAIMS

1. A method of maintaining a state of a memory cell without interrupting access to said memory cell, said method comprising:
applying a back bias to the cell to offset charge leakage out of a floating body of the cell, wherein a charge level of the floating body indicates a state of the memory cell; and

accessing the cell.

2. The method of claim 1, wherein said applying comprises applying said back bias to a terminal of said cell that is not used for address selection of said cell.

3. The method of claim 1, wherein said back bias is applied as a constant positive voltage bias.

4. The method of claim 1, wherein said back bias is applied as a periodic pulse of positive voltage.

5. The method of claim 1, wherein a maximum potential that can be stored in said floating body is increased by said applying back bias to the cell, resulting in a relatively larger memory window.

6. The method of claim 1, wherein said application of back bias performs a holding operation on said cell, said method further comprises simultaneously performing a read operation on said cell at the same time that said holding operation is being performed.

7. A method of operating a memory array having rows and columns of memory cells assembled into an array of said memory cells, each said memory cell having a floating body region for storing data; the method comprising:
performing a holding operation on at least all of said cells not aligned in a row or column of a selected cell; and

accessing said selected cell and performing a read or write operation on said selected cell while performing said hold operation on said at least all of said cells not aligned in a row or column of said selected cell.

8. The method of claim 7, wherein said performing a holding operation comprises performing said holding operation on all of said cells and wherein said performing a read or write operation comprises performing a read operation on said selected cell.

9. The method of claim 7, wherein said holding operation is performed by applying back bias to a terminal not used for memory address selection.

10. The method of claim 9, wherein said terminal is segmented to allow independent control of the applied back bias to a selected portion of the memory array.

11. The method of claim 7, wherein said performing a holding operation comprises performing said holding operation on all of said cells except for said selected cell, and wherein said performing a read or write operation comprises performing a write “0” operation on said selected cell, wherein a write “0” operation is also performed on all of said cells sharing a common source line terminal with said selected cell during said performing a write“0” operation.

12. The method of claim 7, comprising an individual bit write “0” operation, wherein said performing a holding operation comprises performing said holding operation on all of said cells except for said selected cell, while said performing a read or write operation comprises performing a write “0” operation on said selected cell.

13. The method of claim 7, wherein said performing a holding operation comprises performing said holding operation on all of said cells except for said selected cell while said performing a read or write operation comprises performing a write “1” operation on said selected cell.

14. The method of claim 7, wherein said performing a holding operation comprises performing said holding operation on all of said cells except for said selected cell while said performing a read or write operation comprises performing a multi-level write operation on said selected cell, using an alternating write and verify algorithm.

15. The method of claim 7, wherein said performing a holding operation comprises performing said holding operation on all of said cells except for said selected cell while said performing a read or write operation comprises performing a single-level or multi-level write operation on said selected cell, wherein said single-level and each level of said multi-level write operation includes: ramping a voltage applied to said selected cell to perform said write operation; reading the state of said selected cell by monitoring a change in current toward an addressable terminal of said selected cell; and verifying a state of said write operation using a reference memory cell.

16. The method of claim 15, further comprising configuring a state of said reference memory cell using a write-then-verify operation, prior to performing said write operation.

17. The method of claim 15, wherein said configuring a state of said reference memory cell comprises configuring said state upon power up of said memory array.

18. A method of operating a memory array having rows and columns of memory cells assembled into an array of said memory cells, each said memory cell having a floating body region for storing data; the method comprising:
refreshing a state of at least one of said memory cells; and

accessing at least one other of said memory cells, wherein access of said at least one other of said memory cells is not interrupted by said refreshing, and wherein said refreshing is performed without alternating read and write operations.