

ESD PROTECTION CIRCUIT

ABSTRACT

A device which includes a substrate defined with a device region with an ESD protection circuit having at least first and second transistors is disclosed. Each of the transistors includes a gate having first and second sides, a first diffusion region in the device region adjacent to the first side of the gate, a second diffusion region in the device region displaced away from the second side of the gate, and a drift isolation region disposed between the gate and the second diffusion region. A first device well encompasses the device region and a second device well is disposed within the first device well. The device also includes a drift well which encompasses the second diffusion region. Edges of the drift well do not extend below the gate and is away from a channel region. A drain well is disposed under the second diffusion region and within the drift well.

Fig. 1