



159159

-230-

principle drawing of Fig. 109A, the semiconductor memory cell of Example 10 comprises;

- 5 (1) a first transistor TR_1 for readout, having a first conductivity type (for example, n-channel type) and having source/drain regions, a semi-conductive channel forming region CH_1 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_1 ,
- 10 (2) a second transistor TR_2 for switching, having a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_2 which is in contact with the source/drain regions and spaces out the source/drain
- 15 regions, and a gate G capacitively coupled with the channel forming region CH_2 ,
- (3) a junction-field-effect transistor JF_1 for current control, having source/drain regions, a channel region CH_{J1} and gate regions, and
- 20 (4) an MIS type diode DT for retaining information, the semiconductor memory cell having;
 - (a) a semi-conductive first region SC_1 having a first conductivity type (for example, n-type),
 - (b) a semi-conductive second region SC_2 which is
 - 25 in contact with the first region SC_1 and has a second conductivity type (for example, p^+ -type),
 - (c) a third region SC_3 which is formed in a surface region of the first region SC_1 and is in contact with the first region SC_1 so as to form a rectifier
 - 30 junction together with the first region SC_1 , the third region SC_3 being a region which is semi-conductive and has the second conductivity type (for example, p^+ -type) or which is conductive and composed of a silicide, a metal or a metal compound,
 - 35 (d) a semi-conductive fourth region SC_4 which is formed in a surface region of the second region SC_2 and has the first conductivity type (for example, n^+ -type),



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-231-

(e) a fifth region SC_5 which is formed in a surface region of the fourth region SC_4 and is in contact with the fourth region SC_4 so as to form a rectifier junction together with the fourth region SC_4 ,
5 the fifth region SC_5 being a region which is semi-conductive and has the second conductivity type (for example, p^+ -type) or which is conductive and composed of a silicide, a metal or a metal compound, and

(f) the gate G which is formed, through an
10 insulation layer, so as to bridge the first region SC_1 and the fourth region SC_4 and so as to bridge the second region SC_2 and the third region SC_3 , and is shared by the first transistor TR_1 and the second transistor TR_2 .

In the semiconductor memory cell shown in
15 Fig. 114, the first region SC_1 and the second region SC_2 are in contact with each other, while, specifically, the second region SC_2 is formed in a surface region of the first region SC_1 . In the semiconductor memory cell shown in Fig. 120, the first region SC_1 is formed in a
20 surface region of the second region SC_2 .

Concerning the first transistor TR_1 ,

(A-1) one source/drain region is formed of a surface region of the first region SC_1 ,

(A-2) the other source/drain region is formed of a
25 surface region of the fourth region SC_4 , and

(A-3) the channel forming region CH_1 is formed of a surface region of the second region SC_2 which surface region is interposed between the surface region of the first region SC_1 and the surface region of the fourth
30 region SC_4 .

Concerning the second transistor TR_2 ,

(B-1) one source/drain region is formed of the surface region of the second region SC_2 which surface region constitutes the channel forming region CH_1 of the
35 first transistor TR_1 ,

(B-2) the other source/drain region is formed of the third region SC_3 , and

-232-

(B-3) the channel forming region CH_2 is formed of the surface region of the first region SC_1 which surface region constitutes one source/drain region of the first transistor TR_1 .

5 Concerning the junction-field-effect transistor JF_1 ,

(C-1) the gate regions are formed of the fifth region SC_5 and part of the second region SC_2 which part is opposed to the fifth region SC_5 ,

10 (C-2) the channel region CH_{J1} is formed of part of the fourth region SC_4 which part is interposed between the fifth region SC_5 and said part of the second region SC_2 ,

(C-3) one source/drain region is formed of the
15 surface region of the fourth region SC_4 which surface region extends from one end of the channel region CH_{J1} of the junction-field-effect transistor JF_1 and constitutes the other source/drain region of the first transistor TR_1 , and

20 (C-4) the other source/drain region is formed of a portion of the fourth region SC_4 which portion extends from the other end of the channel region CH_{J1} of the junction-field-effect transistor JF_1 .

Concerning the MIS type diode DT ,

25 (D-1) one end thereof is formed of part SC_{2A} of the second region SC_2 , and

(D-2) an electrode constituting the other end thereof is formed to be opposed to said part SC_{2A} of the second region SC_2 which part SC_{2A} constitutes one end of
30 the MIS type diode DT , through a wide gap thin film WG .

The wide gap thin film WG can be composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the second region SC_2 (the channel forming
35 region CH_1 of the first transistor TR_1) and the potential in the other end (electrode EL) of the MIS type diode DT . Specifically, it can be composed, for

-233-

example, of an SiO_2 or SiON film having a thickness of 5 nm or smaller, or an SiN film having a thickness of 9 nm or smaller.

The electrode EL constituting the other end
5 of the MIS type diode DT is connected to the line (third line) through a high-resistance element R having a resistance of approximately 10^9 to $10^{12} \Omega$. Specifically, the electrode EL constituting the other end of the MIS type diode DT and the high-resistance element R are
10 integrally formed and are composed of a polysilicon thin layer containing an impurity having the first conductivity type.

In the above semiconductor memory cell,
further,

15 (E) the gate G is connected to a first line (for example, word line) for memory cell selection,

(F) the third region SC_3 is connected to a write-in information setting line WISL,

(G) the portion of the fourth region SC_4 which
20 portion constitutes the other source/drain region of the junction-field-effect transistor JF_1 is connected to a second line,

(H) the electrode EL constituting the other end of the MIS type diode DT is connected to a third line
25 having a predetermined potential, and

(I) the fifth region SC_5 is connected to a fourth line.

The first region SC_1 and the third region SC_3 constitute a pn junction diode D, and the first region
30 SC_1 is connected to the write-in information setting line WISL through the third region SC_3 . In this case, it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line WISL is used
35 as a bit line as well and a second predetermined potential is applied to the second line.

The semiconductor memory cell (specifically,

-234-

the first region SC_1) shown in Fig. 114 is formed in a well structure which is formed, for example, in a p-type semiconductor substrate and has the first conductivity type (for example, n-type). Further, when a first high-concentration-impurity-containing layer SC_{10} having the first conductivity type (for example, n^{++} -type) is formed below the second region SC_2 , the potential or charge to be stored in the channel forming region CH_1 of the first transistor TR_1 for readout can be increased.

The semiconductor memory cell (specifically, the second region SC_2) shown in Fig. 120 is formed in a well structure which is formed, for example, in an n-type semiconductor substrate and has the second conductivity type (for example, p-type). Further, when a first high-concentration-impurity-containing layer SC_{10} having the first conductivity type (for example, n^{++} -type) is formed below the second region SC_2 , the potential or charge to be stored in the channel forming region CH_1 of the first transistor TR_1 for readout can be increased.

The junction-field-effect transistor JF_1 is formed by

(X) optimizing the distance between the facing gate regions (the fifth region SC_5 and the part of the second region SC_2 which part is opposed to the fifth region SC_5), that is, the thickness of the channel region CH_{J1} , and

(Y) optimizing the impurity concentration of each of the facing gate regions (the fifth region SC_5 and the part of the second region SC_2 which part is opposed to the fifth region SC_5) and the impurity concentration of the channel region CH_{J1} .

In the semiconductor memory cell shown in Fig. 114, there may be employed an embodiment in which the formation of the pn junction diode D is omitted and a second high-concentration-impurity-containing layer (not shown) which has the first conductivity type (for

-235-

example, n^{++} -type) and works as a fifth line is formed below the first region SC_1 . In the semiconductor memory cell shown in Fig. 120, there may be employed an embodiment in which the formation of the pn junction diode D is omitted and the first region SC_1 is connected to a fifth line (not shown). Fig. 108 shows the principle of these semiconductor memory cells. In these cases, it is preferred to employ a constitution in which the second line is used as a bit line and a second predetermined potential is applied to the fifth line, or a constitution in which the fifth line is used as a bit line and a second predetermined potential is applied to the second line.

Figs. 115 to 119 and Figs. 121 to 125 show schematic partial cross-sectional views of variants of the semiconductor memory cell of Example 10. In the semiconductor memory cells shown in Figs. 115 to 119, the first region SC_1 and the second region SC_2 are in contact, and specifically, the second region SC_2 is formed in a surface region of the first region SC_1 . In the semiconductor memory cells shown in Figs. 121 to 125, the first region SC_1 is formed in a surface region of the second region SC_2 .

In the semiconductor memory cells shown in the principle drawing of Fig. 109A and the schematic partial cross-sectional views of Figs. 115 and 121, there is further provided a diode-constituting region SC_D which is formed in a surface region of the first region SC_1 and is in contact with the first region SC_1 to form a rectifier junction together with the first region SC_1 , the diode-constituting region SC_D and the first region SC_1 constitute a majority carrier diode DS, and the first region SC_1 is connected to the write-in information setting line WISL through the majority carrier diode DS. In this case, it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in

-236-

information setting line WISL is used as a bit line as well and a second predetermined potential is applied to the second line. In Fig. 115, the diode-constituting region SC_D is formed in the center of the third region SC_3 and is surrounded by the third region SC_3 , while the position of the diode-constituting region SC_D shall not be limited thereto.

Further, as is shown in the principle drawings of Fig. 110 and Figs. 111A and 111B and the schematic partial cross-sectional views of Figs. 116, 117, 122 and 123, there may be employed a constitution in which the fifth region SC_5 is connected to the write-in information setting line WISL in place of being connected to the fourth line. Further, as is shown in the principle drawings of Fig. 112 and Figs. 113A and 113B and the schematic partial cross-sectional views of Figs. 118, 119, 124 and 125, there may be employed a constitution in which the fifth region SC_5 is connected to the second region SC_2 in place of being connected to the fourth line. In these cases, as is shown in Figs. 116, 118, 122 and 124, there may be employed a constitution in which the first region SC_1 and the third region SC_3 constitute a pn junction diode D, and the first region SC_1 is connected to the write-in information setting line WISL through the third region SC_3 . Otherwise, as is shown in Figs. 117, 119, 123 and 125, there may be employed a constitution in which there is further provided a diode-constituting region SC_D which is formed in a surface region of the first region SC_1 and is in contact with the first region SC_1 to form a rectifier junction together with the first region SC_1 , the diode-constituting region SC_D and the first region SC_1 constitute a majority carrier diode DS, and the first region SC_1 is connected to the write-in information setting line WISL through the diode-constituting region SC_D . In these cases where the diode or the majority carrier diode DS is formed, it is

-237-

preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line WISL is used as a bit line as well and a second predetermined potential is applied to the second line.

Example 11

Example 11 is concerned with the semiconductor memory cell according to the sixth and eighteenth aspects of the present invention. In the semiconductor memory cell of Example 11, the other gate region of the junction-field-effect transistor JF_1 is connected to one gate region of the junction-field-effect transistor JF_1 in place of being connected to the fourth line. More specifically, one end of the MIS type diode DT and the other gate region of the junction-field-effect transistor JF_1 are formed as a common region. Further, the fifth region SC_5 constituting the other gate region of the junction-field-effect transistor JF_1 corresponds to an extending region of the channel forming region CH_1 of the first transistor TR_1 .

That is, as is shown in the principle drawing of Fig. 127A and the schematic partial cross-sectional views of Figs. 128 and 130, the semiconductor memory cell of Example 11 comprises;

(1) a first transistor TR_1 for readout, having a first conductivity type (for example, n-channel type), and having source/drain regions, a semi-conductive channel forming region CH_1 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_1 ,

(2) a second transistor TR_2 for switching, having a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_2 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the

-238-

channel forming region CH_2 ,

(3) a junction-field-effect transistor JF_1 for current control, having source/drain regions, a channel region CH_{J1} and gate regions, and

5 (4) an MIS type diode DT for retaining information, the semiconductor memory cell having;

(a) a semi-conductive first region SC_1 having a first conductivity type (for example, n-type),

10 (b) a semi-conductive second region SC_2 which is in contact with the first region SC_1 and has a second conductivity type (for example, p^+ -type),

(c) a third region SC_3 which is formed in a surface region of the first region SC_1 and is in contact with the first region SC_1 so as to form a rectifier
15 junction together with the first region SC_1 , the third region SC_3 being a region which is semi-conductive and has the second conductivity type (for example, p^+ -type) or which is conductive and is composed of a silicide, a metal or a metal compound,

20 (d) a semi-conductive fourth region SC_4 which is formed in a surface region of the second region SC_2 and has the first conductivity type (for example, n^+ -type),

(e) a semi-conductive fifth region SC_5 which is formed in a surface region of the fourth region SC_4 and
25 has the second conductivity type (for example, p^+ -type), and

(f) the gate G which is formed, through an insulation layer, so as to bridge the first region SC_1 and the fourth region SC_4 , and so as to bridge the second
30 region SC_2 and the third region SC_3 , and is shared by the first transistor TR_1 and the second transistor TR_2 .

In the semiconductor memory cell shown in Fig. 128 and a semiconductor memory cell to be explained later with reference to Fig. 129, the first region SC_1
35 and the second region SC_2 are in contact with each other, and specifically, the second region SC_2 is formed in a surface region of the first region SC_1 . In the

-239-

semiconductor memory cell shown in Fig. 130 and a semiconductor memory cell to be explained later with reference to Fig. 131, the first region SC_1 is formed in a surface region of the second region SC_2 .

5 Concerning the first transistor TR_1 ,

(A-1) one source/drain region is formed of a surface region of the first region SC_1 ,

(A-2) the other source/drain region is formed of a surface region of the fourth region SC_4 , and

10 (A-3) the channel forming region CH_1 is formed of a surface region of the second region SC_2 which surface region is interposed between the surface region of the first region SC_1 and the surface region of the fourth region SC_4 .

15 Concerning the first transistor TR_1 ,

(A-1) one source/drain region is formed of a surface region of the first region SC_1 ,

(A-2) the other source/drain region is formed of a surface region of the fourth region SC_4 , and

20 (A-3) the channel forming region CH_1 is formed of a surface region of the second region SC_2 which surface region is interposed between the surface region of the first region SC_1 and the surface region of the fourth region SC_4 .

25 Concerning the junction-field-effect transistor JF_1 ,

(C-1) the gate regions are formed of the fifth region SC_5 and part of the second region SC_2 which part is opposed to the fifth region SC_5 ,

30 (C-2) the channel region CH_{J1} is formed of part of the fourth region SC_4 which part is interposed between the fifth region SC_5 and said part of the second region SC_2 ,

35 (C-3) one source/drain region is formed of the surface region of the fourth region SC_4 which surface region extends from one end of the channel region CH_{J1} of the junction-field-effect transistor JF_1 and

-240-

constitutes the other source/drain region of the first transistor TR_1 , and

(C-4) the other source/drain region is formed of a portion of the fourth region SC_4 which portion extends
5 from the other end of the channel region CH_{J1} of the junction-field-effect transistor JF_1 .

Concerning the MIS type diode DT,

(D-1) one end thereof is formed of the fifth region SC_5 , and

10 (D-2) an electrode constituting the other end thereof is formed to be opposed to the fifth region SC_5 which constitutes one end of the MIS type diode DT, through a wide gap thin film WG.

The wide gap thin film WG can be composed of
15 a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the fifth region SC_5 (corresponding to the extending portion of the channel forming region CH_1 of the first transistor TR_1) and the potential in the other
20 end (electrode EL) of the MIS type diode DT.

Specifically, it can be composed, for example, of an SiO_2 or $SiON$ film having a thickness of 5 nm or smaller, or an SiN film having a thickness of 9 nm or smaller.

The electrode EL constituting the other end
25 of the MIS type diode DT is connected to the line (third line) through a high-resistance element R having a resistance of approximately 10^9 to $10^{12} \Omega$. Specifically, the electrode EL constituting the other end of the MIS type diode DT and the high-resistance element R are
30 integrally formed and are composed of a polysilicon thin layer containing an impurity having the first conductivity type.

In the above semiconductor memory cell, further,

35 (E) the gate G is connected to a first line (for example, word line) for memory cell selection,

(F) the third region SC_3 is connected to a write-

-241-

in information setting line WISL,

(G) the portion of the fourth region SC_4 which portion constitutes the other source/drain region of the junction-field-effect transistor JF_1 is connected to a
5 second line,

(H) the fifth region SC_5 is connected to the second region SC_2 , and

(I) the electrode EL constituting the other end of the MIS type diode DT is connected to a third line
10 having a predetermined potential.

The first region SC_1 and the third region SC_3 constitute a pn junction diode D, and the first region SC_1 is connected to the write-in information setting line WISL through the third region SC_3 . In this case,
15 it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line WISL is used as a bit line as well and a second predetermined potential is applied to the second line.

20 The semiconductor memory cell (specifically, the first region SC_1) shown in Fig. 128 or shown in Fig. 129 is formed in a well structure which is formed, for example, in a p-type semiconductor substrate and has the first conductivity type (for example, n-type). Further,
25 when a first high-concentration-impurity-containing layer SC_{10} having the first conductivity type (for example, n^{++} -type) is formed below the second region SC_2 , the potential or charge to be stored in the channel forming region CH_1 of the first transistor TR_1 for
30 readout can be increased.

The semiconductor memory cell (specifically, the second region SC_2) shown in Fig. 130 or shown in Fig. 131 is formed in a well structure which is formed, for example, in a n-type semiconductor substrate and has the
35 second conductivity type (for example, p-type). Further, when a first high-concentration-impurity-containing layer SC_{10} having the first conductivity type (for

-242-

example, n^{++} -type) is formed below the second region SC_2 , the potential or charge to be stored in the channel forming region CH_1 of the first transistor TR_1 for readout can be increased.

5 The junction-field-effect transistor JF_1 is formed by

(X) optimizing the distance between the facing gate regions (the fifth region SC_5 and the part of the second region SC_2 which part is opposed to the fifth
10 region SC_5), that is, the thickness of the channel region CH_{J1} , and

(Y) optimizing the impurity concentration of each of the facing gate regions (the fifth region SC_5 and the part of the second region SC_2 which part is opposed to
15 the fifth region SC_5) and the impurity concentration of the channel region CH_{J1} .

In the semiconductor memory cell shown in Fig. 128, there may be employed an embodiment in which the formation of the pn junction diode D is omitted and
20 a second high-concentration-impurity-containing layer (not shown) which has the first conductivity type (for example, n^{++} -type) and works as a fifth line is formed below the first region SC_1 . In the semiconductor memory cell shown in Fig. 130, there may be employed an
25 embodiment in which the formation of the pn junction diode D is omitted and the first region SC_1 is connected to a fifth line (not shown). Fig. 126 shows the principle of these semiconductor memory cells. In these cases, it is preferred to employ a constitution in which
30 the second line is used as a bit line and a second predetermined potential is applied to the fifth line, or a constitution in which the fifth line is used as a bit line and a second predetermined potential is applied to the second line.

35 In the semiconductor memory cells shown in the principle drawing of Fig. 127B and the schematic partial cross-sectional views of Figs. 129 and 131,

-243-

there is further provided a diode-constituting region SC_D which is formed in a surface region of the first region SC_1 and is in contact with the first region SC_1 to form a rectifier junction together with the first region SC_1 , the diode-constituting region SC_D and the first region SC_1 constitute a majority carrier diode DS , and the first region SC_1 is connected to the write-in information setting line $WISL$ through the diode-constituting region SC_D . In this case, it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line $WISL$ is used as a bit line as well and a second predetermined potential is applied to the second line. In Fig. 129, the diode-constituting region SC_D is formed in the center of the third region SC_3 and is surrounded by the third region SC_3 , while the position of the diode-constituting region SC_D shall not be limited thereto.

Example 12

Example 12 is concerned with the semiconductor memory cell according to the seventh and nineteenth aspects of the present invention. The semiconductor memory cell of Example 12 differs from the semiconductor memory cell of Example 10 in that a third transistor TR_3 for current control is formed. That is, as is shown in the principle drawing of Fig. 133A, the semiconductor memory cell of Example 12 comprises;

(1) a first transistor TR_1 for readout, having a first conductivity type (for example, n-channel type), and having source/drain regions, a semi-conductive channel forming region CH_1 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_1 ,

(2) a second transistor TR_2 for switching, having a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive

-244-

channel forming region CH_2 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_2 ,

5 (3) a third transistor TR_3 for current control, having the second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_3 which is in contact with the source/drain regions and spaces out the
10 source/drain regions, and a gate G capacitively coupled with the channel forming region CH_3 ,

(4) a junction-field-effect transistor JF_1 for current control, having source/drain regions, a channel region CH_{J1} and gate regions, and

15 (5) an MIS type diode DT for retaining information.

In the semiconductor memory cell of Example
12,

one source/drain region of the first transistor TR_1 corresponds to the channel forming region CH_2 of the
20 second transistor TR_2 ,

the other source/drain region of the first transistor TR_1 corresponds to one source/drain region of the junction-field-effect transistor JF_1 ,

one source/drain region of the second transistor
25 TR_2 corresponds to the channel forming region CH_1 of the first transistor TR_1 , corresponds to one gate region of the junction-field-effect transistor JF_1 and corresponds to one source/drain region of the third transistor TR_3 ,

the other source/drain region of the third
30 transistor TR_3 corresponds to the other gate region of the junction-field-effect transistor JF_1 , and

one end of the MIS type diode DT is formed of an extending portion of the channel forming region CH_1 of the first transistor TR_1 , the other end of the MIS type
35 diode DT is formed of an electrode EL composed of a conductive material, and the electrode EL is connected to a line (third line) having a predetermined potential.

-245-

Further, the gate G of the first transistor TR_1 , the gate G of the second transistor TR_2 , and the gate G of the third transistor TR_3 are connected to a first line (for example, word line) for memory cell selection, the other source/drain regions of the first transistor TR_1 is connected to a second line through the junction-field-effect transistor JF_1 , one source/drain region of the first transistor TR_1 is connected to a write-in information setting line WISL through a diode D, the other source/drain region of the second transistor TR_2 is connected to the write-in information setting line WISL, and the other end of the MIS type diode DT is connected to a third line (corresponding to the above line) having a predetermined potential through a high-resistance element R. It is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line WISL is used as a bit line as well and a second predetermined potential is applied to the second line.

As shown in the schematic partial cross-sectional views of Figs. 134 and 136, the semiconductor memory cell of Example 12 comprises;

(1) a first transistor TR_1 for readout, having a first conductivity type (for example, n-channel type), and having source/drain regions, a semi-conductive channel forming region CH_1 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_1 ,

(2) a second transistor TR_2 for switching, having a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_2 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_2 ,

-246-

(3) a third transistor TR_3 for current control, having the second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_3 which is in
5 contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_3 ,

(4) a junction-field-effect transistor JF_1 for current control, having source/drain regions, a channel
10 region CH_{J1} and gate regions, and

(5) an MIS type diode DT for retaining information.
the semiconductor memory cell having;

(a) a semi-conductive first region SC_1 having a first conductivity type (for example, n-type),

15 (b) a semi-conductive second region SC_2 which is in contact with the first region SC_1 and has a second conductivity type (for example, p^+ -type),

(c) a third region SC_3 which is formed in a surface region of the first region SC_1 and is in contact
20 with the first region SC_1 so as to form a rectifier junction together with the first region SC_1 , the third region SC_3 being a region which is semi-conductive and has the second conductivity type (for example, p^+ -type) or which is conductive and is composed of a silicide, a
25 metal or a metal compound,

(d) a semi-conductive fourth region SC_4 which is formed in a surface region of the second region SC_2 and has the first conductivity type (for example, n^+ -type),

(e) a fifth region SC_5 which is formed in a
30 surface region of the fourth region SC_4 and is in contact with the fourth region SC_4 so as to form a rectifier junction together with the fourth region SC_4 , the fifth region SC_5 being a region which is semi-conductive and has the second conductivity type (for
35 example, p^+ -type) or which is conductive and is composed of a silicide, a metal or a metal compound, and

(f) the gate G which is formed, through an

-247-

insulation layer, so as to bridge the first region SC_1 and the fourth region SC_4 , so as to bridge the second region SC_2 and the third region SC_3 and so as to bridge the second region SC_2 and the fifth region SC_5 , and is
5 shared by the first transistor TR_1 , the second transistor TR_2 and the third transistor TR_3 .

In the semiconductor memory cell shown in Fig. 134 and a semiconductor memory cell to be explained later with reference to Fig. 135, the first region SC_1
10 and the second region SC_2 are in contact with each other, and specifically, the second region SC_2 is formed in a surface region of the first region SC_1 . In the semiconductor memory cell shown in Fig. 136 and a semiconductor memory cell to be explained later with
15 reference to Fig. 137, the first region SC_1 is formed in a surface region of the second region SC_2 .

Concerning the first transistor TR_1 ,

(A-1) one source/drain region is formed of a surface region of the first region SC_1 ,

20 (A-2) the other source/drain region is formed of a surface region of the fourth region SC_4 , and

(A-3) the channel forming region CH_1 is formed of a surface region of the second region SC_2 which surface region is interposed between the surface region of the first region SC_1 and the surface region of the fourth region SC_4 .
25

Concerning the second transistor TR_2 ,

(B-1) one source/drain region is formed of the surface region of the second region SC_2 ,

30 (B-2) the other source/drain region is formed of the third region SC_3 , and

(B-3) the channel forming region CH_2 is formed of the surface region of the first region SC_1 .

Concerning the third transistor TR_3 ,

35 (C-1) one source/drain region is formed of the surface region of the second region SC_2 ,

(C-2) the other source/drain region is formed of

-248-

the fifth region SC_5 , and

(C-3) the channel forming region CH_3 is formed of the surface region of the fourth region SC_4 .

Concerning the junction-field-effect

5 transistor JF_1 ,

(D-1) the gate regions are formed of the fifth region SC_5 and part of the second region SC_2 which part is opposed to the fifth region SC_5 ,

(D-2) the channel region CH_{J1} is formed of part of
10 the fourth region SC_4 which part is interposed between the fifth region SC_5 and said part of the second region SC_2 ,

(D-3) one source/drain region is formed of the surface region of the fourth region SC_4 which surface
15 region extends from one end of the channel region CH_{J1} of the junction-field-effect transistor JF_1 and constitutes the other source/drain region of the first transistor TR_1 and the channel forming region CH_3 of the third transistor TR_3 , and

(D-4) the other source/drain region is formed of a
20 portion of the fourth region SC_4 which portion extends from the other end of the channel region CH_{J1} of the junction-field-effect transistor JF_1 .

Concerning the MIS type diode DT ,

(E-1) one end thereof is formed of part SC_{2A} of the
25 second region SC_2 , and

(E-2) an electrode constituting the other end thereof is formed to be opposed to said part SC_{2A} of the second region SC_2 which part SC_{2A} constitutes one end of
30 the MIS type diode DT , through a wide gap thin film WG .

The wide gap thin film WG can be composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the second region SC_2 (the channel forming
35 region CH_1 of the first transistor TR_1) and the potential in the other end (electrode EL) of the MIS type diode DT . Specifically, it can be composed, for

-249-

example, of an SiO_2 or SiON film having a thickness of 5 nm or smaller, or an SiN film having a thickness of 9 nm or smaller.

The electrode EL constituting the other end
5 of the MIS type diode DT is connected to the line (third line) through a high-resistance element R having a resistance of approximately 10^9 to $10^{12} \Omega$. Specifically, the electrode EL constituting the other end of the MIS type diode DT and the high-resistance element R are
10 integrally formed and are composed of a polysilicon thin layer containing an impurity having the first conductivity type.

In the above semiconductor memory cell,
further,

15 (F) the gate G is connected to a first line (for example, word line) for memory cell selection,

(G) the third region SC_3 is connected to a write-in information setting line WISL,

(H) the portion of the fourth region SC_4 which
20 portion constitutes the other source/drain region of the junction-field-effect transistor JF_1 is connected to a second line, and

(I) the electrode EL constituting the other end of the MIS type diode DT is connected to a third line
25 having a predetermined potential.

The first region SC_1 and the third region SC_3 constitute a pn junction diode D, and the first region SC_1 is connected to the write-in information setting line WISL through the third region SC_3 . In this case,
30 it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line WISL is used as a bit line as well and a second predetermined potential is applied to the second line.

35 The junction-field-effect transistor JF_1 is formed by

(X) optimizing the distance between the facing

-250-

gate regions (the fifth region SC_5 and the part of the second region SC_2 which part is opposed to the fifth region SC_5), that is, the thickness of the channel region CH_{J1} , and

5 (Y) optimizing the impurity concentration of each of the facing gate regions (the fifth region SC_5 and the part of the second region SC_2 which part is opposed to the fifth region SC_5) and the impurity concentration of the channel region CH_{J1} .

10 The semiconductor memory cell (specifically, the first region SC_1) shown in Fig. 134 is formed in a well structure which is formed, for example, in an p-type semiconductor substrate and has the first conductivity type (for example, n-type). Further, when
 15 a first high-concentration-impurity-containing layer SC_{10} having the first conductivity type (for example, n^{++} -type) is formed below the second region SC_2 , the potential or charge to be stored in the channel forming region CH_1 of the first transistor TR_1 for readout can
 20 be increased. The semiconductor memory cell (specifically, the second region SC_2) shown in Fig. 136 is formed in a well structure which is formed, for example, in an n-type semiconductor substrate and has the second conductivity type (for example, p-type).
 25 Further, when a first high-concentration-impurity-containing layer SC_{10} having the first conductivity type (for example, n^{++} -type) is formed below the second region SC_2 , the potential or charge to be stored in the channel forming region CH_1 of the first transistor TR_1
 30 for readout can be increased.

In the semiconductor memory cell shown in Fig. 134 or Fig. 136, as is shown in the principle drawing of Fig. 132, there may be employed an embodiment in which the formation of the pn junction diode D is
 35 omitted and the first region SC_1 corresponding to one source/drain region of the first transistor TR_1 is connected to a fourth line (not shown in Fig. 134 or

-251-

136). That is, for example, in the semiconductor memory cell shown in Fig. 134, a second high-concentration-impurity-containing layer SC_{11} which has a first conductivity type (for example, n^{++} -type) and works as the fourth line can be formed below the first region SC_1 . In these cases, it is preferred to employ a constitution in which the second line is used as a bit line and a second predetermined potential is applied to the fourth line, or a constitution in which the fourth line is used as a bit line and a second predetermined potential is applied to the second line.

In the semiconductor memory cell shown in the schematic partial cross-sectional view of Fig. 135 or Fig. 137 and the principle drawing of Fig. 133B, there may be employed a constitution in which there is further provided a diode-constituting region SC_D which is formed in a surface region of the first region SC_1 and is in contact with the first region SC_1 to form a rectifier junction together with the first region SC_1 , the diode-constituting region SC_D and the first region SC_1 constitute a majority carrier diode DS , and the first region SC_1 is connected to the write-in information setting line $WISL$ through the diode-constituting region SC_D . In this case, it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line $WISL$ is used as a bit line as well and a second predetermined potential is applied to the second line.

30 Example 13

The Example 13 is concerned with the semiconductor memory cell according to the eighth and twentieth aspects of the present invention. The semiconductor memory cell of Example 13 differs from the semiconductor memory cell of Example 12 in that one end of the MIS type diode DT and the other gate region of the junction-field-effect transistor JF_1 are formed as a

-252-

common region.

That is, as is shown in the principle drawing of Fig. 139A, the semiconductor memory cell of Example 13 comprises;

5 (1) a first transistor TR_1 for readout, having a first conductivity type (for example, n-channel type), and having source/drain regions, a semi-conductive channel forming region CH_1 which is in contact with the source/drain regions and spaces out the source/drain
10 regions, and a gate G capacitively coupled with the channel forming region CH_1 ,

(2) a second transistor TR_2 for switching, having a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive
15 channel forming region CH_2 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_2 ,

(3) a third transistor TR_3 for current control,
20 having the second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_3 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled
25 with the channel forming region CH_3 ,

(4) a junction-field-effect transistor JF_1 for current control, having source/drain regions, a channel region CH_{J1} and gate regions, and

(5) an MIS type diode DT for retaining information.
30 In the semiconductor memory cell of Example 13,

one source/drain region of the first transistor TR_1 corresponds to the channel forming region CH_2 of the second transistor TR_2 ,

35 the other source/drain region of the first transistor TR_1 corresponds to one source/drain region of the junction-field-effect transistor JF_1 ,

-253-

one source/drain region of the second transistor TR_2 corresponds to the channel forming region CH_1 of the first transistor TR_1 , corresponds to one gate region of the junction-field-effect transistor JF_1 and corresponds
5 to one source/drain region of the third transistor TR_3 ,
the other source/drain region of the third transistor TR_3 corresponds to the other gate region of the junction-field-effect transistor JF_1 , and

one end of the MIS type diode DT corresponds to
10 the other source/drain region of the third transistor TR_3 , the other end of the MIS type diode DT is formed of an electrode EL composed of a conductive material, and the electrode EL is connected to a line (third line) having a predetermined potential.

15 Further, the gate G of the first transistor TR_1 , the gate G of the second transistor TR_2 and the gate of the third transistor TR_3 are connected to a first line (for example, word line) for memory cell selection, the other source/drain regions of the first
20 transistor TR_1 is connected to a second line through the junction-field-effect transistor JF_1 , one source/drain region of the first transistor TR_1 is connected to a write-in information setting line $WISL$ through a diode D , the other source/drain region of the second transistor
25 TR_2 is connected to the write-in information setting line $WISL$, and the other end of the MIS type diode DT is connected to a third line (corresponding to the above line) having a predetermined potential through a high-resistance element R . It is preferred to employ a
30 constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line $WISL$ is used as a bit line as well and a second predetermined potential is applied to the second line.

35 In another embodiment, as shown in the schematic partial cross-sectional views of Figs. 140 and 142, the semiconductor memory cell of Example 13

-254-

comprises;

(1) a first transistor TR_1 for readout, having a first conductivity type (for example, n-channel type), and having source/drain regions, a semi-conductive
5 channel forming region CH_1 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_1 ,

(2) a second transistor TR_2 for switching, having
10 a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_2 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the
15 channel forming region CH_2 ,

(3) a third transistor TR_3 for current control, having the second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_3 which is in
20 contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_3 ,

(4) a junction-field-effect transistor JF_1 for current control, having source/drain regions, a channel
25 region CH_{J1} and gate regions, and

(5) an MIS type diode DT for retaining information, the semiconductor memory cell having;

(a) a semi-conductive first region SC_1 having a first conductivity type (for example, n-type),

30 (b) a semi-conductive second region SC_2 which is in contact with the first region SC_1 and has a second conductivity type (for example, p^+ -type),

(c) a third region SC_3 which is formed in a surface region of the first region SC_1 and is in contact
35 with the first region SC_1 so as to form a rectifier junction together with the first region SC_1 , the third region SC_3 being a region which is semi-conductive and

-255-

has the second conductivity type (for example, p^+ -type) or which is conductive and is composed of a silicide, a metal or a metal compound,

(d) a semi-conductive fourth region SC_4 which is
5 formed in a surface region of the second region SC_2 and has the first conductivity type (for example, n^+ -type),

(e) a semi-conductive fifth region SC_5 which is formed in a surface region of the fourth region SC_4 and has the second conductivity type (for example, p^+ -type),
10 and

(f) the gate G which is formed, through an insulation layer, so as to bridge the first region SC_1 and the fourth region SC_4 , so as to bridge the second region SC_2 and the third region SC_3 and so as to bridge
15 the second region SC_2 and the fifth region SC_5 , and is shared by the first transistor TR_1 , the second transistor TR_2 and the third transistor TR_3 .

In the semiconductor memory cell shown in Fig. 140 and a semiconductor memory cell to be explained
20 later with reference to Fig. 141, the first region SC_1 and the second region SC_2 are in contact with each other, and specifically, the second region SC_2 is formed in a surface region of the first region SC_1 . In the semiconductor memory cell shown in Fig. 142 and a
25 semiconductor memory cell to be explained later with reference to Fig. 143, the first region SC_1 is formed in a surface region of the second region SC_2 .

Concerning the first transistor TR_1 ,

(A-1) one source/drain region is formed of a
30 surface region of the first region SC_1 ,

(A-2) the other source/drain region is formed of a surface region of the fourth region SC_4 , and

(A-3) the channel forming region CH_1 is formed of a surface region of the second region SC_2 which surface
35 region is interposed between the surface region of the first region SC_1 and the surface region of the fourth region SC_4 .

-256-

Concerning the second transistor TR_2 ,

(B-1) one source/drain region is formed of the surface region of the second region SC_2 ,

(B-2) the other source/drain region of the second transistor TR_2 is formed of the third region SC_3 , and

(B-3) the channel forming region CH_2 is formed of the surface region of the first region SC_1 .

Concerning the third transistor TR_3 ,

(C-1) one source/drain region is formed of the surface region of the second region SC_2 ,

(C-2) the other source/drain region of the third transistor TR_3 is formed of the fifth region SC_5 , and

(C-3) the channel forming region CH_3 is formed of the surface region of the fourth region SC_4 .

Concerning the junction-field-effect transistor JF_1 ,

(D-1) the gate regions are formed of the fifth region SC_5 and part of the second region SC_2 which part is opposed to the fifth region SC_5 ,

(D-2) the channel region CH_{J1} is formed of part of the fourth region SC_4 which part is interposed between the fifth region SC_5 and said part of the second region SC_2 ,

(D-3) one source/drain region is formed of the surface region of the fourth region SC_4 which surface region extends from one end of the channel region CH_{J1} of the junction-field-effect transistor JF_1 and constitutes the other source/drain region of the first transistor TR_1 and the channel forming region CH_3 of the third transistor TR_3 , and

(D-4) the other source/drain region is formed of a portion of the fourth region SC_4 which portion extends from the other end of the channel region CH_{J1} of the junction-field-effect transistor JF_1 .

Further, concerning the MIS type diode DT ,

(E-1) one end thereof is formed of the fifth region SC_5 , and

-257-

(E-2) an electrode constituting the other end thereof is formed to be opposed to the fifth region SC_5 , which constitutes one end of the MIS type diode DT, through a wide gap thin film WG.

5 The wide gap thin film WG can be composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the fifth region SC_5 (the other source/drain region of the third transistor TR_3) and the
10 potential in the other end (electrode EL) of the MIS type diode DT. Specifically, it can be composed, for example, of an SiO_2 or $SiON$ film having a thickness of 5 nm or smaller, or an SiN film having a thickness of 9 nm or smaller.

15 The electrode EL constituting the other end of the MIS type diode DT is connected to the line (third line) through a high-resistance element R having a resistance of approximately 10^9 to $10^{12} \Omega$. Specifically, the electrode EL constituting the other end of the MIS
20 type diode DT and the high-resistance element R are integrally formed and are composed of a polysilicon thin layer containing an impurity having the first conductivity type.

 In the semiconductor memory cell, further,
25 (F) the gate G is connected to a first line (for example, word line) for memory cell selection,

 (G) the third region SC_3 is connected to a write-in information setting line WISL,

 (H) the portion of the fourth region SC_4 which
30 portion constitutes the other source/drain region of the junction-field-effect transistor JF_1 is connected to a second line, and

 (I) the electrode EL constituting the other end of the MIS type diode DT is connected to a third line
35 having a predetermined potential.

 In the semiconductor memory cell of Example 13, an impurity-containing layer SC_{4A} having the second

-258-

conductivity type (for example, p^+ -type) is formed in the surface region of the fourth region SC_4 which surface region constitutes the channel forming region CH_3 of the third transistor TR_3 . Therefore, while
5 information is retained, and, for example, if the potential in the first line is turned to 0 volt, the third transistor TR_3 is brought into an on-state, and the MIS type diode DT and the channel forming region CH_1 of the first transistor TR_1 are put in a continuity.
10 The impurity concentration of the impurity-containing layer SC_{4A} is adjusted such that the third transistor TR_3 is brought into an off-state by the potential in the first line applied during the reading of information.

In the semiconductor memory cells shown in
15 Figs. 140 and 142, the first region SC_1 and the third region SC_3 constitute a pn junction diode D , and the first region SC_1 is connected to the write-in information setting line $WISL$ through the third region SC_3 . In this case, it is preferred to employ a
20 constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line $WISL$ is used as a bit line as well and a second predetermined potential is applied to the second line.

25 The junction-field-effect transistor JF_1 is formed by

(X) optimizing the distance between the facing gate regions (the fifth region SC_5 and the part of the second region SC_2 which part is opposed to the fifth
30 region SC_5), that is, the thickness of the channel region CH_{J1} , and

(Y) optimizing the impurity concentration of each of the facing gate regions (the fifth region SC_5 and the part of the second region SC_2 which part is opposed to
35 the fifth region SC_5) and the impurity concentration of the channel region CH_{J1} .

The semiconductor memory cell (specifically,

-259-

the first region SC_1) shown in Fig. 140 is formed in a well structure which is formed, for example, in an p-type semiconductor substrate and has the first conductivity type (for example, n-type). Further, when

5 a first high-concentration-impurity-containing layer SC_{10} having the first conductivity type (for example, n^{++} -type) is formed below the second region SC_2 , the potential or charge to be stored in the channel forming region CH_1 of the first transistor TR_1 for readout can

10 be increased. The semiconductor memory cell (specifically, the second region SC_2) shown in Fig. 142 is formed in a well structure which is formed, for example, in an n-type semiconductor substrate and has the second conductivity type (for example, p-type).

15 Further, when a first high-concentration-impurity-containing layer SC_{10} having the first conductivity type (for example, n^{++} -type) is formed below the second region SC_2 , the potential or charge to be stored in the channel forming region CH_1 of the first transistor TR_1

20 for readout can be increased.

In the semiconductor memory cell shown in Fig. 140 or Fig. 142, as is shown in the principle drawing of Fig. 138, there may be employed an embodiment in which the formation of the pn junction diode D is

25 omitted and the first region SC_1 corresponding to one source/drain region of the first transistor TR_1 is connected to the fourth line (not shown in Fig. 140 or 142). That is, for example, in the semiconductor memory cell shown in Fig. 140, a second high-concentration-

30 impurity-containing layer SC_{11} which has the first conductivity type (for example, n^{++} -type) and works as the fourth line can be formed below the first region SC_1 . In these cases, it is preferred to employ a constitution in which the second line is used as a bit line and a

35 second predetermined potential is applied to the fourth line, or a constitution in which the fourth line is used as a bit line and a second predetermined potential is

-260-

applied to the second line.

In the semiconductor memory cells shown in the schematic partial cross-sectional views of Figs. 141 and Fig. 143 and the principle drawing of Fig. 139B, there may be employed a constitution in which there is further provided a diode-constituting region SC_D which is formed in a surface region of the first region SC_1 and is in contact with the first region SC_1 to form a rectifier junction together with the first region SC_1 , the diode-constituting region SC_D and the first region SC_1 constitute a majority carrier diode DS , and the first region SC_1 is connected to the write-in information setting line $WISL$ through the diode-constituting region SC_D . In this case, it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line $WISL$ is used as a bit line as well and a second predetermined potential is applied to the second line.

20 Example 14

Example 14 is concerned with the semiconductor memory cell according to the ninth and twenty-first aspects of the present invention. The semiconductor memory cell of Example 14 differs from the semiconductor memory cell of Example 7 in that a second junction-field-effect transistor JF_2 is provided. That is, as is shown in the principle drawing of Fig. 145A, the semiconductor memory cell of Example 14 comprises;

(1) a first transistor TR_1 for readout, having a first conductivity type (for example, n-channel type), and having source/drain regions, a semi-conductive channel forming region CH_1 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_1 ,

(2) a second transistor TR_2 for switching, having a second conductivity type (for example, p-channel type),

-261-

and having source/drain regions, a semi-conductive channel forming region CH_2 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the

5 channel forming region CH_2 ,

(3) a first junction-field-effect transistor JF_1 for current control, having source/drain regions, a channel region CH_{J1} and gate regions,

(4) a second junction-field-effect transistor JF_2 for current control, having source/drain regions, a channel region CH_{J2} and gate regions, and

(5) an MIS type diode DT for retaining information.

In the semiconductor memory cell of Example 14,

15 one source/drain region of the first transistor TR_1 corresponds to the channel forming region CH_2 of the second transistor TR_2 and corresponds to one source/drain region of the first junction-field-effect transistor JF_1 ,

20 the other source/drain region of the first transistor TR_1 corresponds to one source/drain region of the second junction-field-effect transistor JF_2 ,

one source/drain region of the second transistor TR_2 corresponds to the channel forming region CH_1 of the first transistor TR_1 , corresponds to one gate region of the first junction-field-effect transistor JF_1 and corresponds to one gate region of the second junction-field-effect transistor JF_2 , and

30 one end of the MIS type diode DT is formed of an extending portion of the channel forming region CH_1 of the first transistor TR_1 , the other end of the MIS type diode DT is formed of an electrode EL composed of a conductive material, and the electrode EL is connected to a line (third line) having a predetermined potential.

35 In the semiconductor memory cell of Example 14,

the gate of the first transistor TR_1 and the gate of the

-262-

second transistor TR_2 are connected to a first line (for example, word line) for memory cell selection, the other source/drain region of the first transistor TR_1 is connected to a second line through the second junction-field-effect transistor JF_2 , the other gate region of the second junction-field-effect transistor JF_2 is connected to a fourth line, one source/drain region of the first transistor TR_1 is connected to a write-in information setting line WISL through the first junction-field-effect transistor JF_1 and a diode D, the other source/drain region of the second transistor TR_2 is connected to the write-in information setting line WISL, the other end of the MIS type diode DT is connected to a third line (corresponding to the above line) having a predetermined potential through a high-resistance element R. It is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line WISL is used as a bit line as well and a second predetermined potential is applied to the second line.

As shown in the schematic partial cross-sectional view of Fig. 148 or Fig. 152, the semiconductor memory cell of Example 14 comprises;

(1) a first transistor TR_1 for readout, having a first conductivity type (for example, n-channel type), and having source/drain regions, a semi-conductive channel forming region CH_1 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_1 ,

(2) a second transistor TR_2 for switching, having a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_2 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the

-263-

channel forming region CH_2 ,

(3) a first junction-field-effect transistor JF_1 for current control, having source/drain regions, a channel region CH_{J1} and gate regions,

5 (4) a second junction-field-effect transistor JF_2 for current control, having source/drain regions, a channel region CH_{J2} and gate regions, and

(5) an MIS type diode DT for retaining information, the semiconductor memory cell having;

10 (a) a semi-conductive first region SC_1 having a first conductivity type (for example, n-type),

(b) a semi-conductive second region SC_2 which is in contact with the first region SC_1 and has a second conductivity type (for example, p^+ -type),

15 (c) a third region SC_3 which is formed in a surface region of the first region SC_1 and is in contact with the first region SC_1 so as to form a rectifier junction together with the first region SC_1 , the third region SC_3 being a region which is semi-conductive and
20 has the second conductivity type (for example, p^+ -type) or which is conductive and is composed of a silicide, a metal or a metal compound,

(d) a semi-conductive fourth region SC_4 which is formed in a surface region of the second region SC_2 and
25 has the first conductivity type (for example, n^+ -type),

(e) a fifth region SC_5 which is formed in a surface region of the fourth region SC_4 and is in contact with the fourth region SC_4 so as to form a rectifier junction together with the fourth region SC_4 ,
30 the fifth region SC_5 being a region which is semi-conductive and has the second conductivity type (for example, p^+ -type) or which is conductive and is composed of a silicide, a metal or a metal compound, and

(f) the gate G which is formed, through an
35 insulation layer, so as to bridge the first region SC_1 and the fourth region SC_4 and so as to bridge the second region SC_2 and the third region SC_3 , and is shared by

-264-

the first transistor TR_1 and the second transistor TR_2 .

The first region SC_1 and the second region SC_2 are in contact with each other, and in the semiconductor memory cell shown in Fig. 148 and
5 semiconductor memory cells to be explained later with reference to Figs. 149 to 151, specifically, the second region SC_2 is formed in a surface region of the first region SC_1 . In the semiconductor memory cell shown in Fig. 152 and semiconductor memory cells to be explained
10 later with reference to Figs. 153 to 155, the first region SC_1 is formed in a surface region of the second region SC_2 .

Concerning the first transistor TR_1 ,

(A-1) one source/drain region is formed of a
15 surface region of the first region SC_1 ,

(A-2) the other source/drain region is formed of a surface region of the fourth region SC_4 , and

(A-3) the channel forming region CH_1 is formed of a surface region of the second region SC_2 which surface
20 region is interposed between the surface region of the first region SC_1 and the surface region of the fourth region SC_4 .

Concerning the second transistor TR_2 ,

(B-1) one source/drain region is formed of the
25 surface region of the second region SC_2 ,

(B-2) the other source/drain region is formed of the third region SC_3 , and

(B-3) the channel forming region CH_2 is formed of the surface region of the first region SC_1 .

30 Concerning the first junction-field-effect transistor JF_1 ,

(C-1) the gate regions are formed of the third region SC_3 and part of the second region SC_2 which part is opposed to the third region SC_3 ,

35 (C-2) the channel region CH_{J1} is formed of part of the first region SC_1 which part is interposed between the third region SC_3 and said part of the second region

-265-

SC₂,

(C-3) one source/drain region is formed of the surface region of the first region SC₁ which surface region extends from one end of the channel region CH_{J1} of the first junction-field-effect transistor JF₁ and constitutes one source/drain region of the first transistor TR₁, and

(C-4) the other source/drain region is formed of a portion of the first region SC₁ which portion extends from the other end of the channel region CH_{J1} of the first junction-field-effect transistor JF₁.

Concerning the second junction-field-effect transistor JF₂,

(D-1) the gate regions are formed of the fifth region SC₅ and part of the second region SC₂ which part is opposed to the fifth region SC₅,

(D-2) the channel region CH_{J2} is formed of part of the fourth region SC₄ which part is interposed between the fifth region SC₅ and said part of the second region SC₂,

(D-3) one source/drain region is formed of the surface region of the fourth region SC₄ which surface region extends from one end of the channel region CH_{J2} of the second junction-field-effect transistor JF₂ and constitutes the other source/drain region of the first transistor TR₁, and

(D-4) the other source/drain region is formed of a portion of the fourth region SC₄ which portion extends from the other end of the channel region CH_{J2} of the second junction-field-effect transistor JF₂.

Further, concerning the MIS type diode DT,

(E-1) one end thereof is formed of part SC_{2A} of the second region SC₂, and

(E-2) an electrode constituting the other end thereof is formed to be opposed to said part SC_{2A} of the second region SC₂ which part SC_{2A} constitutes one end of the MIS type diode DT, through a wide gap thin film WG.

-266-

The wide gap thin film WG can be composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the second region SC_2 (the channel forming region CH_1 of the first transistor TR_1) and the potential in the other end (electrode EL) of the MIS type diode DT. Specifically, it can be composed, for example, of an SiO_2 or $SiON$ film having a thickness of 5 nm or smaller, or an SiN film having a thickness of 9 nm or smaller.

The electrode EL constituting the other end of the MIS type diode DT is connected to the line (third line) through a high-resistance element R having a resistance of approximately 10^9 to $10^{12} \Omega$. Specifically, the electrode EL constituting the other end of the MIS type diode DT and the high-resistance element R are integrally formed and are composed of a polysilicon thin layer containing an impurity having the first conductivity type.

In the above semiconductor memory cell, further,

(F) the gate G is connected to a first line (for example, word line) for memory cell selection,

(G) the third region SC_3 is connected to a write-in information setting line WISL,

(H) the portion of the fourth region SC_4 constituting the other source/drain region of the second junction-field-effect transistor JF_2 is connected to a second line,

(I) the electrode EL constituting the other end of the MIS type diode DT is connected to a third line having a predetermined potential, and

(J) the fifth region SC_5 is connected to a fourth line.

Further, the first region SC_1 and the third region SC_3 constitute a pn junction diode D, and the first region SC_1 is connected to the write-in

-267-

information setting line WISL through the third region SC_3 . In this case, it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in

- 5 information setting line WISL is used as a bit line as well and a second predetermined potential is applied to the second line.

The semiconductor memory cell (specifically, the first region SC_1) shown in Fig. 148 is formed in a well structure which is formed, for example, in an p-type semiconductor substrate and has the first conductivity type (for example, n-type). Further, when a first high-concentration-impurity-containing layer SC_{10} having the first conductivity type (for example, n^{++} -type) is formed below the second region SC_2 , the potential or charge to be stored in the channel forming region CH_1 of the first transistor TR_1 for readout can be increased. The semiconductor memory cell (specifically, the second region SC_2) shown in Fig. 152 is formed in a well structure which is formed, for example, in an n-type semiconductor substrate and has the second conductivity type (for example, p-type). Further, when a first high-concentration-impurity-containing layer SC_{10} having the first conductivity type (for example, n^{++} -type) is formed below the second region SC_2 , the potential or charge to be stored in the channel forming region CH_1 of the first transistor TR_1 for readout can be increased.

The first junction-field-effect transistor JF_1 is formed by

- (X) optimizing the distance between the facing gate regions (the third region SC_3 and the part of the second region SC_2 which part is opposed to the third region SC_3), that is, the thickness of the channel region CH_{J1} , and

(Y) optimizing the impurity concentration of each of the facing gate regions (the third region SC_3 and the

-268-

part of the second region SC_2 which part is opposed to the third region SC_3) and the impurity concentration of the channel region CH_{J1} .

Further, the second junction-field-effect transistor JF_2 is formed by

(X) optimizing the distance between the facing gate regions (the fifth region SC_5 and part of the second region SC_2 which part is opposed to the fifth region SC_5), that is, the thickness of the channel region CH_{J2} , and

(Y) optimizing the impurity concentration of each of the facing gate regions (the fifth region SC_5 and the part of the second region SC_2 which part is opposed to the fifth region SC_5) and the impurity concentration of the channel region CH_{J2} .

In the semiconductor memory cells shown in Fig. 148 and Fig. 152, as is shown in the principle drawing of Fig. 144, there may be employed an embodiment in which the formation of the pn junction diode D is omitted and the first region SC_1 corresponding to one source/drain region of the first transistor TR_1 is connected to a fifth line (not shown in Fig. 148 and Fig. 152). In these cases, it is preferred to employ a constitution in which the second line is used as a bit line and a second predetermined potential is applied to the fifth line, or a constitution in which the fifth line is used as a bit line and a second predetermined potential is applied to the second line. In the semiconductor memory cell shown in Fig. 148, a second high-concentration-impurity-containing layer (not shown) which has the first conductivity type (for example, n^{++} -type) and works as the fifth line can be formed below the first region SC_1 .

In the semiconductor memory cells shown in the principle drawing of Fig. 145B and the schematic partial cross-sectional views of Fig. 149 and Fig. 153, there is further provided a diode-constituting region

-269-

SC_D which is formed in a surface region of the first region SC₁ and is in contact with the first region SC₁ to form a rectifier junction together with the first region SC₁, the diode-constituting region SC_D and the first region SC₁ constitute a majority carrier diode DS, and the first region SC₁ is connected to the write-in information setting line WISL through the diode-constituting region SC_D. In this case, it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line WISL is used as a bit line as well and a second predetermined potential is applied to the second line.

In semiconductor memory cells shown in the principle drawing of Fig. 147A and the schematic partial cross-sectional views of Fig. 150 and 154, the fifth region SC₅ corresponding to the other gate region of the second junction-field-effect transistor JF₂ is connected to the second region SC₂ corresponding to one gate region of the second junction-field-effect transistor JF₂ in place of being connected to the fourth line.

In the semiconductor memory cells shown in Fig. 150 and Fig. 154, as is shown in the principle drawing of Fig. 146, there may be employed an embodiment in which the formation of the pn junction diode D is omitted and the first region SC₁ corresponding to one source/drain region of the first transistor TR₁ is connected to a fifth line (not shown in Fig. 150 and Fig. 154). In these cases, it is preferred to employ a constitution in which the second line is used as a bit line and a second predetermined potential is applied to the fifth line, or a constitution in which the fifth line is used as a bit line and a second predetermined potential is applied to the second line. In the semiconductor memory cell shown in Fig. 150, the wiring structure of the semiconductor memory cell can be simplified by forming a second high-concentration-

-270-

impurity-containing layer (not shown) which has the first conductivity type (for example, n^{++} -type) and works as the fifth line, below the first region SC_1 .

In the semiconductor memory cells shown in the principle drawing of Fig. 147B and the schematic partial cross-sectional views of Fig. 151 and Fig. 155, there is further provided a diode-constituting region SC_D which is formed in a surface region of the first region SC_1 and is in contact with the first region SC_1 to form a rectifier junction together with the first region SC_1 , the diode-constituting region SC_D and the first region SC_1 constitute a majority carrier diode DS , and the first region SC_1 is connected to the write-in information setting line WISL through the diode-constituting region SC_D . In this case, it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line WISL is used as a bit line as well and a second predetermined potential is applied to the second line.

Example 15

Example 15 is concerned with the semiconductor memory cell according to the ninth and twenty-second aspects of the present invention. The semiconductor memory cell of Example 15 differs from the semiconductor memory cell of Example 14 in that one end of the MIS type diode DT and the other gate region of the second junction-field-effect transistor JF_2 are formed as a common region. Further, the fifth region SC_5 constituting the other gate region of the second junction-field-effect transistor JF_2 corresponds to an extending portion of the channel forming region CH_1 of the first transistor TR_1 .

That is, the semiconductor memory cell of Example 15 shown in the principle drawing of Fig. 157A and the schematic partial cross-sectional views of Fig. 158 and Fig. 160 comprises;

-271-

(1) a first transistor TR_1 for readout, having a first conductivity type (for example, n-channel type), and having source/drain regions, a semi-conductive channel forming region CH_1 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_1 ,

(2) a second transistor TR_2 for switching, having a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_2 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_2 ,

(3) a first junction-field-effect transistor JF_1 for current control, having source/drain regions, a channel region CH_{J1} and gate regions,

(4) a second junction-field-effect transistor JF_2 for current control, having source/drain regions, a channel region CH_{J2} and gate regions, and

(5) an MIS type diode DT for retaining information, the semiconductor memory cell having;

(a) a semi-conductive first region SC_1 having a first conductivity type (for example, n-type),

(b) a semi-conductive second region SC_2 which is in contact with the first region SC_1 and has a second conductivity type (for example, p^+ -type),

(c) a third region SC_3 which is formed in a surface region of the first region SC_1 and is in contact with the first region SC_1 so as to form a rectifier junction together with the first region SC_1 , the third region SC_3 being a region which is semi-conductive and has the second conductivity type (for example, p^+ -type) or which is conductive and is composed of a silicide, a metal or a metal compound,

(d) a semi-conductive fourth region SC_4 which is formed in a surface region of the second region SC_2 and

-272-

has the first conductivity type (for example, n^+ -type),

(e) a semi-conductive fifth region SC_5 which is formed in a surface region of the fourth region SC_4 and has the second conductivity type (for example, p^+ -type),

5 and

(f) the gate G which is formed, through an insulation layer, so as to bridge the first region SC_1 and the fourth region SC_4 and so as to bridge the second region SC_2 and the third region SC_3 , and is shared by
10 the first transistor TR_1 and the second transistor TR_2 .

While the first region SC_1 and the second region SC_2 are in contact with each other, specifically, in the semiconductor memory cell shown in Fig. 158 or a semiconductor memory cell to be explained later with
15 reference to Fig. 159, the second region SC_2 is formed in a surface region of the first region SC_1 . In the semiconductor memory cell shown in Fig. 160 or a semiconductor memory cell to be explained later with reference to Fig. 161, the first region SC_1 is formed in
20 a surface region of the second region SC_2 .

Concerning the first transistor TR_1 ,

(A-1) one source/drain region is formed of a surface region of the first region SC_1 ,

(A-2) the other source/drain region is formed of a
25 surface region of the fourth region SC_4 , and

(A-3) the channel forming region CH_1 is formed of a surface region of the second region SC_2 which surface region is interposed between the surface region of the first region SC_1 and the surface region of the fourth
30 region SC_4 .

Concerning the second transistor TR_2 ,

(B-1) one source/drain region is formed of the surface region of the second region SC_2 ,

(B-2) the other source/drain region is formed of
35 the third region SC_3 , and

(B-3) the channel forming region CH_2 is formed of the surface region of the first region SC_1 .

-273-

Concerning the first junction-field-effect transistor JF_1 ,

(C-1) the gate regions are formed of the third region SC_3 and part of the second region SC_2 which part is opposed to the third region SC_3 ,

(C-2) the channel region CH_{J1} is formed of part of the first region SC_1 which part is interposed between the third region SC_3 and said part of the second region SC_2 ,

(C-3) one source/drain region is formed of the surface region of the first region SC_1 which surface region extends from one end of the channel region CH_{J1} of the first junction-field-effect transistor JF_1 and constitutes one source/drain region of the first transistor TR_1 , and

(C-4) the other source/drain region is formed of a portion of the first region SC_1 which portion extends from the other end of the channel region CH_{J1} of the first junction-field-effect transistor JF_1 .

Concerning the second junction-field-effect transistor JF_2 ,

(D-1) the gate regions are formed of the fifth region SC_5 and part of the second region SC_2 which part is opposed to the fifth region SC_5 ,

(D-2) the channel region CH_{J2} is formed of part of the fourth region SC_4 which part is interposed between the fifth region SC_5 and said part of the second region SC_2 ,

(D-3) one source/drain region is formed of the surface region of the fourth region SC_4 which surface region extends from one end of the channel region CH_{J2} of the second junction-field-effect transistor JF_2 and constitutes the other source/drain region of the first transistor TR_1 , and

(D-4) the other source/drain region is formed of a portion of the fourth region SC_4 which portion extends from the other end of the channel region CH_{J2} of the

-274-

second junction-field-effect transistor JF_2 .

Further, concerning the MIS type diode DT,

(E-1) one end thereof is formed of the fifth region SC_5 , and

5 (E-2) an electrode constituting the other end thereof is formed to be opposed to the fifth region SC_5 which constitutes one end of the MIS type diode DT, through a wide gap thin film WG.

The wide gap thin film WG can be composed of
10 a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the fifth region SC_5 (corresponding to the extending portion of the channel forming region CH_1 of the first transistor TR_1) and the potential in the other
15 end (electrode EL) of the MIS type diode DT.

Specifically, it can be composed, for example, of an SiO_2 or $SiON$ film having a thickness of 5 nm or smaller, or an SiN film having a thickness of 9 nm or smaller.

The electrode EL constituting the other end
20 of the MIS type diode DT is connected to the line (third line) through a high-resistance element R having a resistance of approximately 10^9 to $10^{12} \Omega$. Specifically, the electrode EL constituting the other end of the MIS type diode DT and the high-resistance element R are
25 integrally formed and are composed of a polysilicon thin layer containing an impurity having the first conductivity type.

In the above semiconductor memory cell, further,

30 (F) the gate G is connected to a first line (for example, word line) for memory cell selection,

(G) the third region SC_3 is connected to a write-in information setting line WISL,

(H) the portion of the fourth region SC_4
35 constituting the other source/drain region of the second junction-field-effect transistor JF_2 is connected to a second line,

-275-

(I) the fifth region SC_5 is connected to the second region SC_2 , and

(J) the electrode EL constituting the other end of the MIS type diode DT is connected to a third line
5 having a predetermined potential.

Further, the first region SC_1 and the third region SC_3 constitute a pn junction diode D, and the first region SC_1 is connected to the write-in information setting line WISL through the third region
10 SC_3 . In this case, it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line WISL is used as a bit line as well and a second predetermined potential is applied to
15 the second line.

The semiconductor memory cell (specifically, the first region SC_1) shown in Fig. 158 is formed in a well structure which is formed, for example, in an p-type semiconductor substrate and has the first
20 conductivity type (for example, n-type). Further, when a first high-concentration-impurity-containing layer SC_{10} having the first conductivity type (for example, n^{++} -type) is formed below the second region SC_2 , the potential or charge to be stored in the channel forming region CH_1 of the first transistor TR_1 for readout can
25 be increased. The semiconductor memory cell (specifically, the second region SC_2) shown in Fig. 160 is formed in a well structure which is formed, for example, in an n-type semiconductor substrate and has
30 the second conductivity type (for example, p-type). Further, when a first high-concentration-impurity-containing layer SC_{10} having the first conductivity type (for example, n^{++} -type) is formed below the second region SC_2 , the potential or charge to be stored in the
35 channel forming region CH_1 of the first transistor TR_1 for readout can be increased.

The first junction-field-effect transistor

-276-

JF₁ is formed by

(X) optimizing the distance between the facing gate regions (the third region SC₃ and the part of the second region SC₂ which part is opposed to the third region SC₃), that is, the thickness of the channel region CH_{J1}, and

(Y) optimizing the impurity concentration of each of the facing gate regions (the third region SC₃ and the part of the second region SC₂ which part is opposed to the third region SC₃) and the impurity concentration of the channel region CH_{J1}.

Further, the second junction-field-effect transistor JF₂ is formed by

(X) optimizing the distance between the facing gate regions (the fifth region SC₅ and the part of the second region SC₂ which part is opposed to the fifth region SC₅), that is, the thickness of the channel region CH_{J2}, and

(Y) optimizing the impurity concentration of each of the facing gate regions (the fifth region SC₅ and the part of the second region SC₂ which part is opposed to the fifth region SC₅) and the impurity concentration of the channel region CH_{J2}.

In the semiconductor memory cells shown in Fig. 158 and Fig. 160, as is shown in the principle drawing of Fig. 156, there may be employed an embodiment in which the formation of the pn junction diode D is omitted and the first region SC₁ corresponding to one source/drain region of the first transistor TR₁ is connected to a fifth line (not shown in Fig. 158 and Fig. 160). In these cases, it is preferred to employ a constitution in which the second line is used as a bit line and a second predetermined potential is applied to the fifth line, or a constitution in which the fifth line is used as a bit line and a second predetermined potential is applied to the second line. In the semiconductor memory cell shown in Fig. 158, a second

-277-

high-concentration-impurity-containing layer (not shown) which has the first conductivity type (for example, n^{++} -type) and works as the fifth line can be formed below the first region SC_1 .

5 In the semiconductor memory cells shown in the principle drawing of Fig. 157B and the schematic partial cross-sectional views of Fig. 159 and Fig. 161, there is further provided a diode-constituting region SC_D which is formed in a surface region of the first
10 region SC_1 and is in contact with the first region SC_1 to form a rectifier junction together with the first region SC_1 , the diode-constituting region SC_D and the first region SC_1 constitute a majority carrier diode DS , and the first region SC_1 is connected to the write-in
15 information setting line $WISL$ through the diode-constituting region SC_D . In this case, it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line $WISL$ is used as a bit
20 line as well and a second predetermined potential is applied to the second line.

Example 16

Example 16 is concerned with the semiconductor memory cell according to the tenth and
25 twenty-third aspects of the present invention. The semiconductor memory cell of Example 16 differs from the semiconductor memory cell of Example 14 in that a third transistor TR_3 for current control is provided. That is, as is shown in the principle drawing of Fig. 163, the
30 semiconductor memory cell of Example 16 comprises;

(1) a first transistor TR_1 for readout, having a first conductivity type (for example, n -channel type), and having source/drain regions, a semi-conductive channel forming region CH_1 which is in contact with the
35 source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_1 ,

-278-

(2) a second transistor TR_2 for switching, having a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_2 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_2 ,

(3) a third transistor TR_3 for current control, having the second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_3 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_3 ,

(4) a first junction-field-effect transistor JF_1 for current control, having source/drain regions, a channel region CH_{J1} and gate regions,

(5) a second junction-field-effect transistor JF_2 for current control, having source/drain regions, a channel region CH_{J2} and gate regions, and

(6) an MIS type diode DT for retaining information, wherein:

one source/drain region of the first transistor TR_1 corresponds to the channel forming region CH_2 of the second transistor TR_2 and corresponds to one source/drain region of the first junction-field-effect transistor JF_1 ,

the other source/drain region of the first transistor TR_1 corresponds to one source/drain region of the second junction-field-effect transistor JF_2 ,

one source/drain region of the second transistor TR_2 corresponds to the channel forming region CH_1 of the first transistor TR_1 , corresponds to one gate region of the first junction-field-effect transistor JF_1 , corresponds to one gate region of the second junction-field-effect transistor JF_2 and corresponds to one source/drain region of the third transistor TR_3 ,

-279-

the other source/drain region of the third transistor TR_3 corresponds to the other gate region of the second junction-field-effect transistor JF_2 , and

one end of the MIS type diode DT is formed of an
5 extending portion of the channel forming region CH_1 of the first transistor TR_1 , the other end of the MIS type diode DT is formed of an electrode EL composed of a conductive material, and the electrode EL is connected to a line (third line) having a predetermined potential.

10 Further, the gate of the first transistor TR_1 , the gate of the second transistor TR_2 and the gate of the third transistor TR_3 are connected to a first line (for example, word line) for memory cell selection, the other source/drain region of the first transistor TR_1 is
15 connected to a second line through the second junction-field-effect transistor JF_2 , one source/drain region of the first transistor TR_1 is connected to a write-in information setting line WISL through the first junction-field-effect transistor JF_1 and a diode D, the
20 other source/drain region of the second transistor TR_2 is connected to the write-in information setting line WISL, the other gate region of the first junction-field-effect transistor JF_1 is connected to the write-in information setting line WISL, and the other end of the
25 MIS type diode DT is connected to the above line (third line) having a predetermined potential through a high-resistance element R. It is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in
30 information setting line WISL is used as a bit line as well and a second predetermined potential is applied to the second line.

As is shown in the schematic partial cross-sectional views of Figs. 165 and 167, the semiconductor
35 memory cell of Example 16 comprises;

(1) a first transistor TR_1 for readout, having a first conductivity type (for example, n-channel type),

-280-

and having source/drain regions, a semi-conductive channel forming region CH_1 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the
5 channel forming region CH_1 ,

(2) a second transistor TR_2 for switching, having a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_2 which is in contact with the
10 source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_2 ,

(3) a third transistor TR_3 for current control, having the second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_3 which is in
15 contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_3 ,

(4) a first junction-field-effect transistor JF_1 for current control, having source/drain regions, a channel region CH_{J1} and gate regions,
20

(5) a second junction-field-effect transistor JF_2 for current control, having source/drain regions, a
25 channel region CH_{J1} and gate regions, and

(6) an MIS type diode DT for retaining information, the semiconductor memory cell having;

(a) a semi-conductive first region SC_1 having a first conductivity type (for example, n-type),

(b) a semi-conductive second region SC_2 which is
30 in contact with the first region SC_1 and has a second conductivity type (for example, p^+ -type),

(c) a third region SC_3 which is formed in a surface region of the first region SC_1 and is in contact
35 with the first region SC_1 so as to form a rectifier junction together with the first region SC_1 , the third region SC_3 being a region which is semi-conductive and

-281-

has the second conductivity type (for example, p^+ -type) or which is conductive and is composed of a silicide, a metal or a metal compound,

(d) a semi-conductive fourth region SC_4 which is
5 formed in a surface region of the second region SC_2 and has the first conductivity type (for example, n^+ -type),

(e) a fifth region SC_5 which is formed in a surface region of the fourth region SC_4 and is in contact with the fourth region SC_4 so as to form a
10 rectifier junction together with the fourth region SC_4 , the fifth region SC_5 being a region which is semi-conductive and has the second conductivity type (for example, p^+ -type) or which is conductive and is composed of a silicide, a metal or a metal compound, and

(f) the gate G which is formed, through an
15 insulation layer, so as to bridge the first region SC_1 and the fourth region SC_4 , so as to bridge the second region SC_2 and the third region SC_3 and so as to bridge the second region SC_2 and the fifth region SC_5 , and is
20 shared by the first transistor TR_1 , the second transistor TR_2 and the third transistor TR_3 .

While the first region SC_1 and the second region SC_2 are in contact with each other, specifically, in the semiconductor memory cell shown in Fig. 165 or a
25 semiconductor memory cell to be explained later with reference to Fig. 166, the second region SC_2 is formed in a surface region of the first region SC_1 . In the semiconductor memory cell shown in Fig. 167 or a semiconductor memory cell to be explained later with
30 reference to Fig. 168, the first region SC_1 is formed in a surface region of the second region SC_2 .

Concerning the first transistor TR_1 ,

(A-1) one source/drain region is formed of a surface region of the first region SC_1 ,

35 (A-2) the other source/drain region is formed of a surface region of the fourth region SC_4 , and

(A-3) the channel forming region CH_1 is formed of

-282-

a surface region of the second region SC_2 which surface region is interposed between the surface region of the first region SC_1 and the surface region of the fourth region SC_4 .

5 Concerning the second transistor TR_2 ,

(B-1) one source/drain region is formed of the surface region of the second region SC_2 ,

(B-2) the other source/drain region is formed of the third region SC_3 , and

10 (B-3) the channel forming region CH_2 is formed of the surface region of the first region SC_1 .

 Concerning the third transistor TR_3 ,

(C-1) one source/drain region is formed of the surface region of the second region SC_2 ,

15 (C-2) the other source/drain region is formed of the fifth region SC_5 , and

(C-3) the channel forming region CH_3 is formed of the surface region of the fourth region SC_4 .

 Concerning the first junction-field-effect
20 transistor JF_1 ,

(D-1) the gate regions are formed of the third region SC_3 and part of the second region SC_2 which part is opposed to the third region SC_3 ,

(D-2) the channel region CH_{J1} is formed of part of
25 the first region SC_1 which part is interposed between the third region SC_3 and said part of the second region SC_2 ,

(D-3) one source/drain region is formed of the surface region of the first region SC_1 which surface
30 region extends from one end of the channel region CH_{J1} of the first junction-field-effect transistor JF_1 and constitutes one source/drain region of the first transistor TR_1 , and

(D-4) the other source/drain region is formed of a
35 portion of the first region SC_1 which portion extends from the other end of the channel region CH_{J1} of the first junction-field-effect transistor JF_1 .

-283-

Concerning the second junction-field-effect transistor JF_2 ,

(E-1) the gate regions are formed of the fifth region SC_5 and part of the second region SC_2 which part is opposed to the fifth region SC_5 ,

(E-2) the channel region CH_{J2} is formed of part of the fourth region SC_4 which part is interposed between the fifth region SC_5 and said part of the second region SC_2 ,

(E-3) one source/drain region is formed of the surface region of the fourth region SC_4 which surface region extends from one end of the channel region CH_{J2} of the second junction-field-effect transistor JF_2 and constitutes the other source/drain region of the first transistor TR_1 and the channel forming region CH_3 of the third transistor TR_3 , and

(E-4) the other source/drain region is formed of a portion of the fourth region SC_4 which portion extends from the other end of the channel region CH_{J2} of the second junction-field-effect transistor JF_2 .

Further, concerning the MIS type diode DT ,

(F-1) one end thereof is formed of part SC_{2A} of the second region SC_2 , and

(F-2) an electrode constituting the other end thereof is formed to be opposed to said part SC_{2A} of the second region SC_2 which part constitutes one end of the MIS type diode DT , through a wide gap thin film WG .

The wide gap thin film WG can be composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the second region SC_2 (the channel forming region CH_1 of the first transistor TR_1) and the potential in the other end (electrode EL) of the MIS type diode DT . Specifically, it can be composed, for example, of an SiO_2 or $SiON$ film having a thickness of 5 nm or smaller, or an SiN film having a thickness of 9 nm or smaller.

-284-

The electrode EL constituting the other end of the MIS type diode DT is connected to the line (third line) through a high-resistance element R having a resistance of approximately 10^9 to $10^{12} \Omega$. Specifically, the electrode EL constituting the other end of the MIS type diode DT and the high-resistance element R are integrally formed and are composed of a polysilicon thin layer containing an impurity having the first conductivity type.

10 In the above semiconductor memory cell, further,

(G) the gate G is connected to a first line (for example, word line) for memory cell selection,

(H) the third region SC_3 is connected to a write-in information setting line WISL,

(I) the portion of the fourth region SC_4 constituting the other source/drain region of the second junction-field-effect transistor JF_2 is connected to a second line, and

20 (J) the electrode EL constituting the other end of the MIS type diode DT is connected to a third line having a predetermined potential.

Further, the first region SC_1 and the third region SC_3 constitute a pn junction diode D, and the first region SC_1 is connected to the write-in information setting line WISL through the third region SC_3 . In this case, it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line WISL is used as a bit line as well and a second predetermined potential is applied to the second line.

The semiconductor memory cell (specifically, the first region SC_1) shown in Fig. 165 is formed in a well structure which is formed, for example, in an p-type semiconductor substrate and has the first conductivity type (for example, n-type). Further, when

-285-

a first high-concentration-impurity-containing layer SC_{10} having the first conductivity type (for example, n^{++} -type) is formed below the second region SC_2 , the potential or charge to be stored in the channel forming region CH_1 of the first transistor TR_1 for readout can be increased. The semiconductor memory cell (specifically, the second region SC_2) shown in Fig. 167 is formed in a well structure which is formed, for example, in an n-type semiconductor substrate and has the second conductivity type (for example, p-type). Further, when a first high-concentration-impurity-containing layer SC_{10} having the first conductivity type (for example, n^{++} -type) is formed below the second region SC_2 , the potential or charge to be stored in the channel forming region CH_1 of the first transistor TR_1 for readout can be increased.

The first junction-field-effect transistor JF_1 is formed by

(X) optimizing the distance between the facing gate regions (the third region SC_3 and the part of the second region SC_2 which part is opposed to the third region SC_3), that is, the thickness of the channel region CH_{J1} , and

(Y) optimizing the impurity concentration of each of the facing gate regions (the third region SC_3 and the part of the second region SC_2 which part is opposed to the third region SC_3) and the impurity concentration of the channel region CH_{J1} .

Further, the second junction-field-effect transistor JF_2 is formed by

(X) optimizing the distance between the facing gate regions (the fifth region SC_5 and the part of the second region SC_2 which part is opposed to the fifth region SC_5), that is, the thickness of the channel region CH_{J2} , and

(Y) optimizing the impurity concentration of each of the facing gate regions (the fifth region SC_5 and the

-286-

part of the second region SC_2 which part is opposed to the fifth region SC_5) and the impurity concentration of the channel region CH_{J2} .

In the semiconductor memory cells shown in Fig. 165 and Fig. 167, as is shown in the principle drawing of Fig. 162, there may be employed an embodiment in which the formation of the pn junction diode D is omitted and the first region SC_1 corresponding to one source/drain region of the first transistor TR_1 is connected to a fourth line (not shown in Fig. 165 and Fig. 167). In these cases, it is preferred to employ a constitution in which the second line is used as a bit line and a second predetermined potential is applied to the fourth line, or a constitution in which the fourth line is used as a bit line and a second predetermined potential is applied to the second line. In the semiconductor memory cell shown in Fig. 165, the wiring structure thereof can be simplified by forming a second high-concentration-impurity-containing layer (not shown) which has the first conductivity type (for example, n^{++} -type) and works as the fourth line, below the first region SC_1 .

In semiconductor memory cells shown in the principle drawing of Fig. 164 and the schematic partial cross-sectional views of Fig. 166 and Fig. 168, there is further provided a diode-constituting region SC_D which is formed in a surface region of the first region SC_1 and is in contact with the first region SC_1 to form a rectifier junction together with the first region SC_1 , the diode-constituting region SC_D and the first region SC_1 constitute a majority carrier diode DS, and the first region SC_1 is connected to the write-in information setting line WISL through the diode-constituting region SC_D . In this case, it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line WISL is used as a bit

-287-

line as well and a second predetermined potential is applied to the second line.

Example 17

Example 17 is concerned with the
5 semiconductor memory cell according to the eleventh and twenty-fourth aspects of the present invention. The semiconductor memory cell of Example 17 differs from the semiconductor memory cell of Example 16 in that one end of the MIS type diode DT and the other gate region of
10 the second junction-field-effect transistor JF₂ are formed as a common region.

That is, as is shown in the principle drawing of Fig. 170, the semiconductor memory cell of Example 17 comprises;

15 (1) a first transistor TR₁ for readout, having a first conductivity type (for example, n-channel type), and having source/drain regions, a semi-conductive channel forming region CH₁ which is in contact with the source/drain regions and spaces out the source/drain
20 regions, and a gate G capacitively coupled with the channel forming region CH₁,

(2) a second transistor TR₂ for switching, having a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive
25 channel forming region CH₂ which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH₂,

(3) a third transistor TR₃ for current control,
30 having the second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH₃ which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled
35 with the channel forming region CH₃,

(4) a first junction-field-effect transistor JF₁ for current control, having source/drain regions, a

-288-

channel region CH_{J1} and gate regions,

(5) a second junction-field-effect transistor JF_2 for current control, having source/drain regions, a channel region CH_{J2} and gate regions, and

5 (6) an MIS type diode DT for retaining information, wherein:

one source/drain region of the first transistor TR_1 corresponds to the channel forming region CH_2 of the second transistor TR_2 and corresponds to one

10 source/drain region of the first junction-field-effect transistor JF_1 ,

the other source/drain region of the first transistor TR_1 corresponds to one source/drain region of the second junction-field-effect transistor JF_2 ,

15 one source/drain region of the second transistor TR_2 corresponds to channel forming region CH_1 of the first transistor TR_1 , corresponds to one gate region of the first junction-field-effect transistor JF_1 , corresponds to one gate region of the second junction-field-effect transistor JF_2 and corresponds to one
20 source/drain region of the third transistor TR_3 ,

the other source/drain region of the third transistor TR_3 corresponds to the other gate region of the second junction-field-effect transistor JF_2 , and

25 one end of the MIS type diode DT corresponds to the other source/drain region of the third transistor TR_3 , the other end of the MIS type diode DT is formed of an electrode EL composed of a conductive material, and the electrode EL is connected to a line (third line)
30 having a predetermined potential.

Further, the gate of the first transistor TR_1 , the gate of the second transistor TR_2 and the gate of third transistor TR_3 are connected to a first line (for example, word line) for memory cell selection, the other
35 source/drain region of the first transistor TR_1 is connected to a second line through the second junction-field-effect transistor JF_2 , one source/drain region of

-289-

the first transistor TR_1 is connected to a write-in information setting line WISL through the first junction-field-effect transistor JF_1 and a diode D , the other source/drain region of the second transistor TR_2 is connected to the write-in information setting line WISL, the other gate region of the first junction-field-effect transistor JF_1 is connected to the write-in information setting line WISL, and the other end of the MIS type diode DT is connected to the above line (third line) having a predetermined potential through a high-resistance element R . It is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line WISL is used as a bit line as well and a second predetermined potential is applied to the second line.

As is shown in the schematic partial cross-sectional views of Figs. 172 and 174, the semiconductor memory cell of Example 17 comprises;

(1) a first transistor TR_1 for readout, having a first conductivity type (for example, n-channel type), and having source/drain regions, a semi-conductive channel forming region CH_1 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_1 ,

(2) a second transistor TR_2 for switching, having a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_2 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH_2 ,

(3) a third transistor TR_3 for current control, having the second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_3 which is in

-290-

contact with the source/drain regions and spaces out the source/drain regions, and a gate G capacitively coupled with the channel forming region CH₃,

(4) a first junction-field-effect transistor JF₁
5 for current control, having source/drain regions, a channel region CH_{J1} and gate regions,

(5) a second junction-field-effect transistor JF₂ for current control, having source/drain regions, a channel region CH_{J2} and gate regions, and

10 (6) an MIS type diode DT for retaining information, the semiconductor memory cell having;

(a) a semi-conductive first region SC₁ having a first conductivity type (for example, n-type),

(b) a semi-conductive second region SC₂ which is
15 in contact with the first region SC₁ and has a second conductivity type (for example, p⁺-type),

(c) a third region SC₃ which is formed in a surface region of the first region SC₁ and is in contact with the first region SC₁ so as to form a rectifier
20 junction together with the first region SC₁, the third region SC₃ being a region which is semi-conductive and has the second conductivity type (for example, p⁺-type) or which is conductive and is composed of a silicide, a metal or a metal compound,

25 (d) a semi-conductive fourth region SC₄ which is formed in a surface region of the second region SC₂ and has the first conductivity type (for example, n⁺-type),

(e) a semi-conductive fifth region SC₅ which is formed in a surface region of the fourth region SC₄ and
30 has the second conductivity type (for example, p⁺-type), and

(f) the gate G which is formed, through an insulation layer, so as to bridge the first region SC₁ and the fourth region SC₄, so as to bridge the second
35 region SC₂ and the third region SC₃ and so as to bridge the second region SC₂ and the fifth region SC₅, and is shared by the first transistor TR₁, the second

-291-

transistor TR_2 and the third transistor TR_3 .

While the first region SC_1 and the second region SC_2 are in contact with each other, specifically, in the semiconductor memory cell shown in Fig. 172 or a semiconductor memory cell to be explained later with reference to Fig. 173, the second region SC_2 is formed in a surface region of the first region SC_1 . In the semiconductor memory cell shown in Fig. 174 or a semiconductor memory cell to be explained later with reference to Fig. 175, the first region SC_1 is formed in a surface region of the second region SC_2 .

Concerning the first transistor TR_1 ,

(A-1) one source/drain region is formed of a surface region of the first region SC_1 ,

(A-2) the other source/drain region is formed of a surface region of the fourth region SC_4 , and

(A-3) the channel forming region CH_1 is formed of a surface region of the second region SC_2 which surface region is interposed between the surface region of the first region SC_1 and the surface region of the fourth region SC_4 .

Concerning the second transistor TR_2 ,

(B-1) one source/drain region is formed of the surface region of the second region SC_2 ,

(B-2) the other source/drain region is formed of the third region SC_3 , and

(B-3) the channel forming region CH_2 is formed of the surface region of the first region SC_1 .

Concerning the third transistor TR_3 ,

(C-1) one source/drain region is formed of the surface region of the second region SC_2 ,

(C-2) the other source/drain region is formed of the fifth region SC_5 , and

(C-3) the channel forming region CH_3 is formed of the surface region of the fourth region SC_4 .

Concerning the first junction-field-effect transistor JF_1 ,

-292-

(D-1) the gate regions are formed of the third region SC_3 and part of the second region SC_2 which part is opposed to the third region SC_3 ,

(D-2) the channel region CH_{J1} is formed of part of
5 the first region SC_1 which part is interposed between the third region SC_3 and said part of the second region SC_2 ,

(D-3) one source/drain region is formed of the surface region of the first region SC_1 which surface
10 region extends from one end of the channel region CH_{J1} of the first junction-field-effect transistor JF_1 and constitutes one source/drain region of the first transistor TR_1 , and

(D-4) the other source/drain region is formed of a
15 portion of the first region SC_1 which portion extends from the other end of the channel region CH_{J1} of the first junction-field-effect transistor JF_1 .

Concerning the second junction-field-effect transistor JF_2 ,

(E-1) the gate regions are formed of the fifth
20 region SC_5 and part of the second region SC_2 which part is opposed to the fifth region SC_5 ,

(E-2) the channel region CH_{J2} is formed of part of
the fourth region SC_4 which part is interposed between
25 the fifth region SC_5 and said part of the second region SC_2 ,

(E-3) one source/drain region is formed of the surface region of the fourth region SC_4 which surface
region extends from one end of the channel region CH_{J2}
30 of the second junction-field-effect transistor JF_2 and constitutes the other source/drain region of the first transistor TR_1 and the channel forming region CH_3 of the third transistor TR_3 , and

(E-4) the other source/drain region is formed of a
35 portion of the fourth region SC_4 which portion extends from the other end of the channel region CH_{J2} of the second junction-field-effect transistor JF_2 .

-293-

Further, concerning the MIS type diode DT,
(E-1) one end thereof is formed of the fifth
region SC₅, and

(E-2) an electrode constituting the other end
5 thereof is formed to be opposed to the fifth region SC₅
which constitutes one end of the MIS type diode DT,
through a wide gap thin film WG.

The wide gap thin film WG can be composed of
a material in which the tunnel transition of carriers is
10 caused depending upon a potential difference between the
potential in the fifth region SC₅ (the other
source/drain region of the third transistor TR₃) and the
potential in the other end (electrode EL) of the MIS
type diode DT. Specifically, it can be composed, for
15 example, of an SiO₂ or SiON film having a thickness of 5
nm or smaller, or an SiN film having a thickness of 9 nm
or smaller.

The electrode EL constituting the other end
of the MIS type diode DT is connected to the line (third
20 line) through a high-resistance element R having a
resistance of approximately 10^9 to 10^{12} Ω . Specifically,
the electrode EL constituting the other end of the MIS
type diode DT and the high-resistance element R are
integrally formed and are composed of a polysilicon thin
25 layer containing an impurity having the first
conductivity type.

In the above semiconductor memory cell,
further,

(G) the gate G is connected to a first line (for
30 example, word line) for memory cell selection,

(H) the third region SC₃ is connected to a write-
in information setting line WISL,

(I) the portion of the fourth region SC₄
constituting the other source/drain region of the second
35 junction-field-effect transistor JF₂ is connected to a
second line,

(J) the fifth region SC₅ is connected to the

-294-

second region SC_2 , and

(K) the electrode EL constituting the other end of the MIS type diode DT is connected to a third line having a predetermined potential.

5 In the semiconductor memory cell of Example 17, an impurity-containing layer SC_{4A} having the second conductivity type (for example, p^{++} -type) is formed in the surface region of the fourth region SC_4 which surface region constitutes the channel forming region
10 CH_3 of the third transistor TR_3 . Therefore, while information is retained, and, for example, if the potential in the first line is turned to 0 volt, the third transistor TR_3 is brought into an on-state, and the MIS type diode DT and the channel forming region CH_1
15 of the first transistor TR_1 are put in a continuity. The impurity concentration of the impurity-containing layer SC_{4A} is adjusted such that the third transistor TR_3 is brought into an off-state by the potential in the first line applied during the reading of information.

20 Further, the first region SC_1 and the third region SC_3 constitute a pn junction diode D, and the first region SC_1 is connected to the write-in information setting line WISL through the third region SC_3 . In this case, it is preferred to employ a
25 constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line WISL is used as a bit line as well and a second predetermined potential is applied to the second line.

30 The semiconductor memory cell (specifically, the first region SC_1) shown in Fig. 172 is formed in a well structure which is formed, for example, in an p-type semiconductor substrate and has the first conductivity type (for example, n-type). Further, when
35 a first high-concentration-impurity-containing layer SC_{10} having the first conductivity type (for example, n^{++} -type) is formed below the second region SC_2 , the

-295-

potential or charge to be stored in the channel forming region CH_1 of the first transistor TR_1 for readout can be increased. The semiconductor memory cell (specifically, the second region SC_2) shown in Fig. 174

5 is formed in a well structure which is formed, for example, in an n-type semiconductor substrate and has the second conductivity type (for example, p-type). Further, when a first high-concentration-impurity-containing layer SC_{10} having the first conductivity type

10 (for example, n^{++} -type) is formed below the second region SC_2 , the potential or charge to be stored in the channel forming region CH_1 of the first transistor TR_1 for readout can be increased.

The first junction-field-effect transistor

15 JF_1 is formed by

(X) optimizing the distance between the facing gate regions (the third region SC_3 and the part of the second region SC_2 which part is opposed to the third region SC_3), that is, the thickness of the channel

20 region CH_{J1} , and

(Y) optimizing the impurity concentration of each of the facing gate regions (the third region SC_3 and the part of the second region SC_2 which part is opposed to the third region SC_3) and the impurity concentration of

25 the channel region CH_{J1} .

Further, the second junction-field-effect transistor JF_2 is formed by

(X) optimizing the distance between the facing gate regions (the fifth region SC_5 and the part of the second region SC_2 which part is opposed to the fifth region SC_5), that is, the thickness of the channel

30 region CH_{J2} , and

(Y) optimizing the impurity concentration of each of the facing gate regions (the fifth region SC_5 and the part of the second region SC_2 which part is opposed to the fifth region SC_5) and the impurity concentration of

35 the channel region CH_{J2} .

-296-

In the semiconductor memory cells shown in Fig. 172 and Fig. 174, as is shown in the principle drawing of Fig. 169, there may be employed an embodiment in which the formation of the pn junction diode D is omitted and the first region SC_1 corresponding to one source/drain region of the first transistor TR_1 is connected to a fourth line (not shown in Fig. 172 and Fig. 174). In these cases, it is preferred to employ a constitution in which the second line is used as a bit line and a second predetermined potential is applied to the fourth line, or a constitution in which the fourth line is used as a bit line and a second predetermined potential is applied to the second line. In the semiconductor memory cell shown in Fig. 172, the wiring structure thereof can be simplified by forming a second high-concentration-impurity-containing layer (not shown) which has the first conductivity type (for example, n^{++} -type) and works as the fourth line, below the first region SC_1 .

In semiconductor memory cells shown in the principle drawing of Fig. 171 and the schematic partial cross-sectional views of Fig. 173 and Fig. 175, there is further provided a diode-constituting region SC_D which is formed in a surface region of the first region SC_1 and is in contact with the first region SC_1 to form a rectifier junction together with the first region SC_1 , the diode-constituting region SC_D and the first region SC_1 constitute a majority carrier diode DS, and the first region SC_1 is connected to the write-in information setting line WISL through the diode-constituting region SC_D . In this case, it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line WISL is used as a bit line as well and a second predetermined potential is applied to the second line.

As an example of the process for

-297-

manufacturing the semiconductor memory cell of the present invention, the process for manufacturing the semiconductor memory cell of Example 7 shown in Fig. 69 will be explained with reference to Figs. 176A, 176B, 177A, 177B, 178A and 178B hereinafter.

[Step-300]

First, a device separation region (not shown), the well of the first conductivity type (for example, n-type well), the semi-conductive first region SC_1 of the first conductivity type (for example, n^{++} -type), the first high-concentration-impurity-containing layer SC_{10} of the first conductivity type (for example, n^{++} -type) (not shown) and a gate insulation layer 12 corresponding to the insulation layer are formed in a p-type silicon semiconductor substrate 10 according to known methods. Then, gate G ($G_1 + G_2$) is formed, for example, from a polysilicon containing an impurity or a polyside or polymetal structure. In this manner, a structure shown in Fig. 176A can be obtained. The n-type first region SC_1 had an impurity concentration of $1.0 \times 10^{17}/\text{cm}^3$, and the gate G ($G_1 + G_2$) had a length of $0.28 \mu\text{m}$.

[Step-310]

Then, an ion-implanting mask 20 is formed from a resist material, and an impurity having the second conductivity type (for example, p-type) is ion-implanted to form the semi-conductive third region SC_3 which is formed in a surface region of the first region SC_1 and has the second conductivity type (see Fig. 176B). The ion implantation can be carried out, for example, under the same conditions as those shown in Table 1.

[Step-320]

Then, the ion-implanting mask 20 is removed, an ion-implanting mask 21 is formed from a resist material, and an impurity having the second conductivity type (for example, p-type) is ion-implanted by an oblique ion implanting method, to form the semi-

-298-

conductive second region SC_2 which is in contact with the first region SC_1 (specifically, formed in a surface region of the first region SC_1), is spaced from the third region SC_3 and has the second conductivity type (for example, p^+ -type). Since the ion implantation is carried out by the oblique ion implanting method, the second region SC_2 is formed below the gates ($G_1 + G_2$) as well (see Fig. 177A). The ion implantation is carried out twice under the same conditions as those shown in Table 2, and the ion incidence angle during one ion-implantation is arranged to differ from that during the other ion-implantation. Particularly, when the ion incidence angle during the first ion-implantation is set at 60 degrees, the impurity concentration of the semi-conductive second region SC_2 below the gate G ($G_1 + G_2$) can be highly accurately controlled.

[Step-330]

Then, an impurity having the first conductivity type (for example, n -type) is ion-implanted to form the fourth region SC_4 which is formed in a surface region of the second region SC_2 and is in contact with the second region SC_2 to form a rectifier junction together with the second region SC_2 (see Fig. 177B). The ion-implantation can be carried out under the same conditions as those shown in Table 3.

[Step-340]

Then, the ion-implanting mask 21 is removed, an SiO_2 layer is formed on the entire surface by a CVD method, and the SiO_2 layer is etched back to form a side-wall 30 on the side wall of the gate G ($G_1 + G_2$).

[Step-350]

Then, an ion-implanting mask 22 is formed from a resist material, and an impurity having the first conductivity type (for example, n -type) is ion-implanted to increase the impurity concentration of the fourth region SC_4 up to approximately 10^{18} to 10^{20} cm^{-3} , whereby the resistance of the fourth region SC_4 is

-299-

decreased (see Fig. 178A). The ion implantation can be carried out under the same conditions as those shown in Table 4.

[Step-360]

5 Then, the ion-implanting mask 22 is removed, an ion-implanting mask 23 is formed from a resist material, and an impurity having the second conductivity type (for example, p-type) is ion-implanted to increase the impurity concentration of the third region SC₃ up to
10 approximately 10^{18} to 10^{20} cm⁻³, whereby the resistance of the third region SC₃ is decreased (see Fig. 178B). The ion implantation can be carried out under the same conditions as those shown in Table 5.

Under the above ion-implanting conditions,
15 the gate regions (second region SC₂ and third region SC₃) of the junction-field-effect transistor JF₁ and the channel region CH_{J1} had impurity concentrations shown in the following Table 7. Further, the channel region CH_{J1} of the junction-field-effect transistor JF₁ had a
20 thickness of 0.1 μm.

Table 7

Second region SC ₂	1.5×10^{18} cm ⁻³
Third region SC ₃	2.1×10^{19} cm ⁻³
Channel region CH _{J1}	5.0×10^{17} cm ⁻³

25 [Step-370]

Then, an insulating interlayer is formed on the entire surface, and the insulating interlayer is patterned using a patterned resist layer as a mask, to expose part of the second region SC₂. A silicon oxide
30 layer (SiO₂ layer) as a wide gap thin film WG is formed on the exposed surface of the second region SC₂. Then, a polysilicon thin layer containing an impurity having the first conductivity type (for example, n-type) is formed on the entire surface, and the polysilicon thin

-300-

layer is patterned to form the electrode EL constituting the other end of a MIS type diode DT connected to the wide gap thin film WG and also to form the high-resistance element R extending from the above electrode EL.

[Step-380]

Then, the write-in information setting line, the second line (bit line), the fourth line, etc., are formed according to known methods.

The steps of manufacturing the semiconductor memory cell shall not be limited to the above process. For example, [Step-310] may be omitted. [Step-320], [Step-330] and [Step-350] may be carried out in any order. The formation of the gate and the formation of the device separation region may be carried out after [Step-370]. The above-described ion-implantation conditions are given for explanation purposes and may be modified as required.

When the MIS-type-diode constituting region SC_{DT} having the second conductivity type (for example, p^+ -type) is formed in the form of a buried plug, it can be formed in [Step-370] by a method in which an insulating interlayer is formed, then, the MIS-type-diode constituting region SC_{DT} is formed by ion implantation using a patterned resist material as a mask, and then the MIS type diode DT is formed.

Example 18

Example 18 is concerned with the semiconductor memory cell according to the fifth and twenty-fifth aspects of the present invention. As is shown in the principle drawing of Fig. 179A and the schematic partial cross-sectional view of Fig. 180A, the semiconductor memory cell of Example 18 has a semiconductor layer having two main surfaces opposed to each other, the main surfaces being a first main surface A_1 and a second main surface A_2 , and the semiconductor memory cell comprises;

-301-

(1) a first transistor TR_1 for readout, having a first conductivity type (for example, n-channel type), and having source/drain regions, a semi-conductive channel forming region CH_1 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G_1 capacitively coupled with the channel forming region CH_1 ,

(2) a second transistor TR_2 for switching, having a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_2 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G_2 capacitively coupled with the channel forming region CH_2 ,

(3) a junction-field-effect transistor JF_1 for current control, having source/drain regions, a channel region CH_{J1} and gate regions, and

(4) an MIS type diode DT for retaining information.

In the semiconductor memory cell of Example 18 shown in Fig. 180A, the gate G_1 of the first transistor TR_1 and the gate G_2 of the second transistor TR_2 are respectively formed on the first main surface A_1 and the second main surface A_2 so as to be opposite to each other thorough the semiconductor layer, and positions of these gates are deviated to some extent with regard to the perpendicular direction. Further, the semiconductor memory cell has a so-called SOI structure in which it is surrounded by an insulation material layer IL_0 formed on a supporting substrate SPS. In the semiconductor memory cell of Example 18 shown in Fig. 180A, the supporting substrate SPS, an insulating interlayer IL_1 , the gate G_2 of the second transistor TR_2 and the gate G_1 of the first transistor TR_1 are arranged in this order from below.

The semiconductor memory cell of Example 18 has;

(a) a semi-conductive first region SC_1 which is

-302-

formed in the semiconductor layer to extend over from the first main surface A_1 to the second main surface A_2 and has a first conductivity type (for example, n-type),

(b) a semi-conductive second region SC_2 which is
5 formed in the semiconductor layer to extend over from the first main surface A_1 to the second main surface A_2 , is in contact with the first region SC_1 and has a second conductivity type (for example, p^+ -type),

(c) a third region SC_3 which is formed in a
10 surface region including the second main surface A_2 of the first region SC_1 to be spaced from the second region SC_2 and is in contact with the first region SC_1 so as to form a rectifier junction together with the first region SC_1 , the third region SC_3 being a region which is semi-
15 conductive and has the second conductivity type (for example, p^+ -type) or which is conductive and is composed of a silicide, a metal or a metal compound,

(d) a fourth region SC_4 which is formed in a surface region including the first main surface A_1 of
20 the second region SC_2 to be spaced from the first region SC_1 and is in contact with the second region SC_2 so as to form a rectifier junction together with the second region SC_2 , the fourth region SC_4 being a region which is semi-conductive and has the second conductivity type
25 (for example, n^+ -type) or which is conductive and is composed of a silicide, a metal or a metal compound,

(e) a fifth region SC_5 which is formed in a surface region including the first main surface A_1 of the first region SC_1 to be spaced from the second region
30 SC_2 and is in contact with the first region SC_1 so as to form a rectifier junction together with the first region SC_1 , the fifth region SC_5 being a region which is semi-conductive and has the second conductivity type (for example, p^+ -type) or which is conductive and is composed
35 of a silicide, a metal or a metal compound,

(f) the gate G_1 of the first transistor TR_1 formed on a first insulation layer formed on the first main

-303-

surface A_1 so as to bridge the first region SC_1 and the fourth region SC_4 , and

(g) the gate G_2 of the second transistor TR_2 formed on a second insulation layer formed on the second main surface A_2 so as to bridge the second region SC_2 and the third region SC_3 .

Concerning the first transistor TR_1 ,

(A-1) one source/drain region is formed of a surface region including the first main surface A_1 of the first region SC_1 ,

(A-2) the other source/drain region is formed of the fourth region SC_4 , and

(A-3) the channel forming region CH_1 is formed of a surface region including the first main surface A_1 of the second region SC_2 which surface region is interposed between the surface region including the first main surface A_1 of the first region SC_1 and the fourth region SC_4 .

Concerning the second transistor TR_2 ,

(B-1) one source/drain region is formed of a surface region including the second main surface A_2 of the second region SC_2 ,

(B-2) the other source/drain region is formed of the third region SC_3 , and

(B-3) the channel forming region CH_2 is formed of a surface region including the second main surface A_2 of the first region SC_1 which surface region is interposed between the surface region including the second main surface A_2 of the second region SC_2 and the third region SC_3 .

Concerning the junction-field-effect transistor JF_1 ,

(C-1) the gate regions of are formed of the fifth region SC_5 and the third region SC_3 which is opposed to the fifth region SC_5 ,

(C-2) the channel region CH_{J1} is formed of part of the first region SC_1 which part is interposed between

-304-

the fifth region SC_5 and the third region SC_3 ,

(C-3) one source/drain region is formed of a portion of the first region SC_1 which portion extends from one end of the channel region CH_{J1} of the junction-field-effect transistor JF_1 and constitutes one source/drain region of the first transistor TR_1 and the channel forming region CH_2 of the second transistor TR_2 , and

(C-4) the other source/drain region is formed of a portion of the first region SC_1 which portion extends from the other end of the channel region CH_{J1} of the junction-field-effect transistor JF_1 .

Concerning the MIS type diode DT ,

(D-1) one end thereof is formed of part of the second region SC_2 , and

(D-2) an electrode EL constituting the other end thereof is formed to be opposed to said part of the second region SC_2 constituting one end of the MIS type diode DT , through a wide gap thin film.

The junction-field-effect transistor JF_1 is formed by

(X) optimizing the distance between the facing gate regions (the fifth region SC_5 and the third region SC_3 which is opposed to the fifth region SC_5), that is, the thickness of the channel region CH_{J1} , and

(Y) optimizing the impurity concentration of each of the facing gate regions (the fifth region SC_5 and the third region SC_3 which is opposed to the fifth region SC_5) and the impurity concentration of the channel region CH_{J1} (specifically, the first region SC_1).

The gate G_1 of the first transistor TR_1 and the gate G_2 of the second transistor TR_2 are connected to a first line (word line) for memory cell selection, and the third region SC_3 is connected to the write-in information setting line $WISL$. Further, the fourth region SC_4 is connected to a second line, the electrode EL constituting the other end of the MIS type diode DT

-305-

is connected to a third line having a predetermined potential, the fifth region SC_5 is connected to a fourth line, and the portion of the first region SC_1 which portion constitutes the other source/drain region of the junction-field-effect transistor JF_1 is connected to a fifth line. The electrode EL constituting the other end of the MIS type diode DT is connected to the third line through a high-resistance element R having a resistance of approximately 10^9 to $10^{12} \Omega$. In this case, there may be employed an embodiment in which the second line to which the fourth region SC_4 is connected is used as a bit line and a second predetermined potential is applied to the fifth line to which the first region SC_1 is connected, or an embodiment in which a second predetermined potential is applied to the second line and the fifth line is used as a bit line.

Figs. 180B, 181A and 181B show schematic partial cross-sectional views of variants of the semiconductor memory cell of Example 18. In the variant shown in Fig. 180B, positions of the gate G_1 of the first transistor TR_1 and the gate G_2 of the second transistor TR_2 are nearly aligned with regard to the perpendicular direction, differing from their positional relationship in Fig. 180A. Forming such a structure serves to decrease the area of the semiconductor memory cell. In the variants shown in Figs. 181A and 181B, the supporting substrate SPS, the insulating interlayer IL_1 , the gate G_1 of the first transistor TR_1 and the gate G_2 of the second transistor TR_2 are arranged in this order from below. The positional relationship of these regions with regard to the perpendicular direction is reverse to the positional relationship of the regions of the semiconductor memory cells shown in Figs. 180A and 180B. In the variant shown in Fig. 181B, positions of the gate G_1 of the first transistor TR_1 and the gate G_2 of the second transistor TR_2 are nearly aligned with regard to the perpendicular direction, differing from

-306-

their positional relationship in Fig. 181A.

Further, Figs. 182A, 182B, 183A, 183B, 184A, 184B, 185A and 185B show schematic partial cross-sectional views of variants of the semiconductor memory cell of Example 18. The principle drawing of the semiconductor memory cells shown in these Figures is as shown in Fig. 179B. The semiconductor memory cells shown in Figs. 182A, 182B 184A and 184B are variants of the semiconductor memory cells shown in Figs. 180A and 180B, and the semiconductor memory cells shown in Figs. 183A, 183B, 185A and 185B are variants of the semiconductor memory cells shown in Figs. 181A and 181B.

In these semiconductor memory cells, the fifth region SC_5 is connected to the write-in information setting line WISL in place of being connected to the fourth line. Being connected to the write-in information setting line WISL is equivalent to being connected to the third region SC_3 . Specifically, the fifth region SC_5 and the third region SC_3 can be connected to each other, for example, by forming a structure in which a portion of the third region SC_3 is extended up to the first main surface A_1 of the semiconductor layer and the fifth region SC_5 and the extending portion of the third region SC_3 are in contact with each other outside the first region SC_1 . The wiring structure of the semiconductor memory cell can be simplified by structuring the semiconductor memory cell as described above. In these cases, it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line WISL is used as a bit line as well and a second predetermined potential is applied to the second line.

The semiconductor memory cell of Example 18 can be manufactured substantially by the same process as that explained in Example 3, so that the detailed explanation thereof is omitted. The junction-field-

-307-

effect transistor JF_1 can be formed by optimizing the distance between the fifth region SC_5 and the third region SC_3 which is opposed to the fifth region SC_5 , that is, the thickness of the channel region CH_{J1} , and
5 by optimizing the impurity concentration of each of the fifth region SC_5 and the third region SC_3 which is opposed to the fifth region SC_5 and the impurity concentration of the first region SC_1 (corresponding to the channel region CH_{J1}). Further, the process for
10 manufacturing semiconductor memory cells of Examples to be explained hereinafter can be also manufactured substantially by the same process as that explained in Example 3 except for differences, for example, in the formation of the fifth region SC_5 and/or the sixth
15 region SC_6 and the formation of a common gate ($G_1 + G_3$), so that the detailed explanations thereof will be omitted.

When each of the semiconductor memory cells of Example 18 and Examples 19 to 22 to be explained
20 later is produced, the order of the formation of gate G_1 of the first transistor TR_1 and formation of gate G_2 of the second transistor TR_2 can be determined depending upon structures of the semiconductor memory cells to be manufactured. Further, the gate G_1 of the first
25 transistor TR_1 , the gate G_2 of the second transistor TR_2 , the facing gate regions of the junction-field-effect transistor JF_1 and the channel region CH_{J1} can be formed in an order required depending upon structures of semiconductor memory cells to be manufactured.

30 Example 19

Example 19 is concerned with the semiconductor memory cell according to the sixth and twenty-sixth aspects of the present invention. As is shown in the principle drawing of Fig. 108, the
35 schematic partial cross-sectional view of Fig. 186A and a schematic layout of gates and regions in Fig. 189A, the semiconductor memory cell of Example 19 has a

-308-

semiconductor layer having two main surfaces opposed to each other, the main surfaces being a first main surface A_1 and a second main surface A_2 , and the semiconductor memory cell comprises;

- 5 (1) a first transistor TR_1 for readout, having a first conductivity type (for example, n-channel type), and having source/drain regions, a semi-conductive channel forming region CH_1 which is in contact with the source/drain regions and spaces out the source/drain
10 regions, and a gate G_1 capacitively coupled with the channel forming region CH_1 ,
- (2) a second transistor TR_2 for switching, having a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive
15 channel forming region CH_2 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G_2 capacitively coupled with the channel forming region CH_2 ,
- (3) a junction-field-effect transistor JF_1 for
20 current control, having source/drain regions, a channel region CH_{J1} and gate regions, and
- (4) an MIS type diode DT for retaining information.

In the semiconductor memory cell of Example 19 shown in Fig. 186A, the gate G_1 of the first
25 transistor TR_1 and the gate G_2 of the second transistor TR_2 are respectively formed on the first main surface A_1 and the second main surface A_2 so as to be opposite to each other thorough the semiconductor layer, and positions of these gates are deviated to some extent
30 with regard to the perpendicular direction. Further, the semiconductor memory cell has a so-called SOI structure in which it is surrounded by an insulation material layer IL_0 formed on a supporting substrate SPS. In the semiconductor memory cell of Example 19 shown in
35 Fig. 186A, the supporting substrate SPS, an insulating interlayer IL_1 , the gate G_2 of the second transistor TR_2 and the gate G_1 of the first transistor TR_1 are arranged

-309-

in this order from below. In Fig. 189A, showing of the gate G_2 and the third region SC_3 is omitted.

The semiconductor memory cell of Example 19 has;

- 5 (a) a semi-conductive first region SC_1 which is formed in the semiconductor layer to extend over from the first main surface A_1 to the second main surface A_2 and has a first conductivity type (for example, n-type),
- (b) a semi-conductive second region SC_2 which is
10 formed in the semiconductor layer to extend over from the first main surface A_1 to the second main surface A_2 , is in contact with the first region SC_1 and has a second conductivity type (for example, p^+ -type),
- (c) a third region SC_3 which is formed in a
15 surface region including the second main surface A_2 of the first region SC_1 to be spaced from the second region SC_2 and is in contact with the first region SC_1 so as to form a rectifier junction together with the first region SC_1 , the third region SC_3 being a region which is semi-
20 conductive and has the second conductivity type (for example, p^+ -type) or which is conductive and is composed of a silicide, a metal or a metal compound,
- (d) a fourth region SC_4 which is formed in a
25 surface region including the first main surface A_1 of the second region SC_2 to be spaced from the first region SC_1 and is in contact with the second region SC_2 so as to form a rectifier junction together with the second region SC_2 , the fourth region SC_4 being a region which is semi-conductive and has the second conductivity type
30 (for example, n^+ -type) or which is conductive and is composed of a silicide, a metal or a metal compound,
- (e) a fifth region SC_5 which is formed in a
35 surface region of the fourth region SC_4 and is in contact with the fourth region SC_4 so as to form a rectifier junction together with the fourth region SC_4 , the fifth region SC_5 being a region which is semi-conductive and has the second conductivity type (for

-310-

example, p^+ -type) or which is conductive and is composed of a silicide, a metal or a metal compound,

(f) the gate G_1 of the first transistor TR_1 formed on a first insulation layer formed on the first main surface A_1 so as to bridge the first region SC_1 and the fourth region SC_4 , and

(g) the gate G_2 of the second transistor TR_2 formed on a second insulation layer formed on the second main surface A_2 so as to bridge the second region SC_2 and the third region SC_3 .

Concerning the first transistor TR_1 ,

(A-1) one source/drain region is formed of a surface region including the first main surface A_1 of the first region SC_1 ,

(A-2) the other source/drain region is formed of the fourth region SC_4 , and

(A-3) the channel forming region CH_1 is formed of a surface region including the first main surface A_1 of the second region SC_2 which surface region is interposed between the surface region including the first main surface A_1 of the first region SC_1 and the fourth region SC_4 .

Concerning the second transistor TR_2 ,

(B-1) one source/drain region is formed of a surface region including the second main surface A_2 of the second region SC_2 ,

(B-2) the other source/drain region is formed of the third region SC_3 , and

(B-3) the channel forming region CH_2 is formed of a surface region including the second main surface A_2 of the first region SC_1 which surface region is interposed between the surface region including the second main surface A_2 of the second region SC_2 and the third region SC_3 .

Concerning the junction-field-effect transistor JF_1 ,

(C-1) the gate regions are formed of the fifth

-311-

region SC_5 and part of the second region SC_2 which part is opposed to the fifth region SC_5 ,

(C-2) the channel region CH_{J1} is formed of part of the fourth region SC_4 which part is interposed between
5 the fifth region SC_5 and said part of the second region SC_2 ,

(C-3) one source/drain region is formed of a portion of the fourth region SC_4 which portion extends from one end of the channel region CH_{J1} of the junction-
10 field-effect transistor JF_1 and constitutes the other source/drain region of the first transistor TR_1 , and

(C-4) the other source/drain region is formed of a portion of the fourth region SC_4 which portion extends from the other end of the channel region CH_{J1} of the
15 junction-field-effect transistor JF_1 .

The junction-field-effect transistor JF_1 is formed by

(X) optimizing the distance between the facing gate regions (the fifth region SC_5 and the part of the
20 second region SC_2 which part is opposed to the fifth region SC_5), that is, the thickness of the channel region CH_{J1} , and

(Y) optimizing the impurity concentration of each of the facing gate regions (the fifth region SC_5 and the
25 part of the second region SC_2 which part is opposed to the fifth region SC_5) and the impurity concentration of the channel region CH_{J1} (fourth region SC_4).

Concerning the MIS type diode DT ,

(D-1) one end thereof is formed of part of the
30 second region SC_2 , and

(D-2) an electrode EL constituting the other end thereof is formed to be opposed to said part of the second region SC_2 constituting one end of the MIS type diode DT , through a wide gap thin film.

35 The gate G_1 of the first transistor TR_1 and the gate G_2 of the second transistor TR_2 are connected to a first line (word line) for memory cell selection,

-312-

and the portion of the fourth region SC_4 which portion constitutes the other source/drain region of the junction-field-effect transistor JF_1 is connected to a second line, the electrode EL constituting the other end of the MIS type diode DT is connected to a third line having a predetermined potential, and the third region SC_3 is connected to the write-in information setting line WISL. Further, the fifth region SC_5 is connected to a fourth line, and the first region SC_1 is connected to a fifth line. The electrode EL constituting the other end of the MIS type diode DT is connected to the third line through a high-resistance element R having a resistance of approximately 10^9 to $10^{12} \Omega$. In this case, there may be employed an embodiment in which the second line to which the fourth region SC_4 is connected is used as a bit line and a second predetermined potential is applied to the fifth line to which the first region SC_1 is connected, or an embodiment in which a second predetermined potential is applied to the second line to which the fourth region SC_4 is connected and the fifth line to which the first region SC_1 is connected is used as a bit line.

Fig. 186B, 187A and 187B show schematic partial cross-sectional views of variants of the semiconductor memory cell of Example 19. In the variant shown in Fig. 186B, positions of the gate G_1 of the first transistor TR_1 and the gate G_2 of the second transistor TR_2 are nearly aligned with regard to the perpendicular direction, differing from their positional relationship in Fig. 186A. Forming such a structure serves to decrease the area of the semiconductor memory cell. In the variants shown in Figs. 187A and 187B, the supporting substrate SPS, the insulating interlayer IL_1 , the gate G_1 of the first transistor TR_1 and the gate G_2 of the second transistor TR_2 are arranged in this order from below. The positional relationship of these regions with regard to the perpendicular direction is

-313-

reverse to the positional relationship of the regions of the semiconductor memory cells shown in Figs. 186A and 186B. In the variant shown in Fig. 187B, positions of the gate G_1 of the first transistor TR_1 and the gate G_2 of the second transistor TR_2 are nearly aligned with regard to the perpendicular direction, differing from their positional relationship in Fig. 187A.

Further, Figs. 188A, 188B, 190A and 190B show schematic partial cross-sectional views of variants of the semiconductor memory cell of Example 19. Fig. 189B shows a schematic layout of gates and regions in the semiconductor memory cell shown in Fig. 188A. In Fig. 189B, showing of the gate G_2 and the third region SC_3 is omitted. The principle drawing of the semiconductor memory cells shown in these Figures is as shown in Fig. 112. That is, in these semiconductor memory cells, the fifth region SC_5 is connected to the second region SC_2 in place of being connected to the fourth line. Specifically, the fifth region SC_5 and the second region SC_2 can be connected to each other, for example, by forming a structure in which a portion of the second region SC_2 is extended up to the first main surface A_1 of the semiconductor layer and the fifth region SC_5 and the extending portion of the second region SC_2 are in contact with each other outside the fourth region SC_4 . The wiring structure of the semiconductor memory cell can be simplified by structuring the semiconductor memory cell as described above. The semiconductor memory cells shown in Figs. 188A and 188B are variants of the semiconductor memory cells shown in Figs. 186A and 186B, and the semiconductor memory cells shown in Figs. 190A and 190B are variants of the semiconductor memory cells shown in Figs. 187A and 187B. In these cases, it is preferred to employ a constitution in which the second line is used as a bit line, or a constitution in which the write-in information setting line WISL is used as a bit line as

-314-

well and a second predetermined potential is applied to the second line.

Example 20

Example 20 is concerned with the
5 semiconductor memory cell according to the twenty-seventh aspect of the present invention. As is shown in the principle drawing of Fig. 191 and the schematic partial cross-sectional view of Fig. 192A, the semiconductor memory cell of Example 20 has a
10 semiconductor layer having two main surfaces opposed to each other, the main surfaces being a first main surface A_1 and a second main surface A_2 , and the semiconductor memory cell comprises;

(1) a first transistor TR_1 for readout, having a
15 first conductivity type (for example, n-channel type), and having source/drain regions, a semi-conductive channel forming region CH_1 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G_1 capacitively coupled with the
20 channel forming region CH_1 ,

(2) a second transistor TR_2 for switching, having a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_2 which is in contact with the
25 source/drain regions and spaces out the source/drain regions, and a gate G_2 capacitively coupled with the channel forming region CH_2 ,

(3) a first junction-field-effect transistor JF_1 for current control, having source/drain regions, a
30 channel region CH_{J1} and gate regions,

(4) a second junction-field-effect transistor JF_2 for current control, having source/drain regions, a channel region CH_{J2} and gate regions, and

(5) an MIS type diode DT for retaining information.
35 That is, the semiconductor memory cell of Example 20 has a structure in which the structure of the semiconductor memory cell according to the twenty-sixth

-315-

aspect of the present invention, explained in Example 19, is modified by forming a semi-conductive or conductive sixth region SC_6 and adding a second junction-field-effect transistor JF_2 for current control. Specifically, in Example 20, there is provided the semi-conductive or conductive sixth region SC_6 which is formed in the surface region of the fourth region SC_4 and is in contact with the fourth region SC_4 to form a rectifier junction together with the fourth region SC_4 .

10 In the semiconductor memory cell shown in Fig. 192A, positions of the gate G_1 of the first transistor TR_1 and the gate G_2 of the second transistor TR_2 are deviated to some extent with regard to the perpendicular direction. Further, the semiconductor memory cell has a so-called SOI structure in which it is surrounded by an insulation material layer IL_0 formed on a supporting substrate SPS. In the semiconductor memory cell of Example 20 shown in Fig. 192A, the supporting substrate SPS, an insulating interlayer IL_1 , the gate G_2 of the second transistor TR_2 and the gate G_1 of the first transistor TR_1 are arranged in this order from below.

The semiconductor memory cell of Example 20 has;

- 25 (a) a semi-conductive first region SC_1 which is formed in the semiconductor layer to extend over from the first main surface A_1 to the second main surface A_2 and has a first conductivity type (for example, n-type),
- (b) a semi-conductive second region SC_2 which is formed in the semiconductor layer to extend over from the first main surface A_1 to the second main surface A_2 , is in contact with the first region SC_1 and has a second conductivity type (for example, p^+ -type),
- 30 (c) a third region SC_3 which is formed in a surface region including the second main surface A_2 of the first region SC_1 to be spaced from the second region SC_2 and is in contact with the first region SC_1 so as to
- 35

-316-

form a rectifier junction together with the first region SC_1 , the third region SC_3 being a region which is semi-conductive and has the second conductivity type (for example, p^+ -type) or which is conductive and is composed
5 of a silicide, a metal or a metal compound,

(d) a fourth region SC_4 which is formed in a surface region including the first main surface A_1 of the second region SC_2 to be spaced from the first region SC_1 and is in contact with the second region SC_2 so as
10 to form a rectifier junction together with the second region SC_2 , the fourth region SC_4 being a region which is semi-conductive and has the second conductivity type (for example, n^+ -type) or which is conductive and is composed of a silicide, a metal or a metal compound,

(e) a fifth region SC_5 which is formed in a surface region including the first main surface A_1 of the first region SC_1 to be spaced from the second region SC_2 and is in contact with the first region SC_1 so as to form a rectifier junction together with the first region
15 SC_1 , the fifth region SC_5 being a region which is semi-conductive and has the second conductivity type (for example, p^+ -type) or which is conductive and is composed of a silicide, a metal or a metal compound,

(f) a sixth region SC_6 which is formed in a surface region of the fourth region SC_4 and is in contact with the fourth region SC_4 so as to form a rectifier junction together with the fourth region SC_4 ,
25 the sixth region SC_6 being a region which is semi-conductive and has the second conductivity type (for example, p^+ -type) or which is conductive and is composed of a silicide, a metal or a metal compound,

(g) the gate G_1 of the first transistor TR_1 formed on a first insulation layer formed on the first main surface A_1 so as to bridge the first region SC_1 and the
35 fourth region SC_4 , and

(h) the gate G_2 of the second transistor TR_2 formed on a second insulation layer formed on the second main

-317-

surface A_2 so as to bridge the second region SC_2 and the third region SC_3 .

Concerning the first transistor TR_1 ,

(A-1) one source/drain region is formed of a
5 surface region including the first main surface A_1 of the first region SC_1 ,

(A-2) the other source/drain region is formed of the fourth region SC_4 , and

(A-3) the channel forming region CH_1 is formed of
10 a surface region including the first main surface A_1 of the second region SC_2 which surface region is interposed between the surface region including the first main surface A_1 of the first region SC_1 and the fourth region SC_4 .

15 Concerning the second transistor TR_2 ,

(B-1) one source/drain region is formed of a surface region including the second main surface A_2 of the second region SC_2 ,

(B-2) the other source/drain region is formed of
20 the third region SC_3 , and

(B-3) the channel forming region CH_2 is formed of a surface region including the second main surface A_2 of the first region SC_1 which surface region is interposed between the surface region including the second main
25 surface A_2 of the second region SC_2 and the third region SC_3 .

Concerning the first junction-field-effect transistor JF_1 ,

(C-1) the gate regions are formed of the fifth
30 region SC_5 and the third region SC_3 which is opposed to the fifth region SC_5 ,

(C-2) the channel region CH_{J1} is formed of part of the first region SC_1 which part is interposed between the fifth region SC_5 and the third region SC_3 ,

35 (C-3) one source/drain region is formed of a portion of the first region SC_1 which portion extends from one end of the channel CH_{J1} region of the first

-318-

junction-field-effect transistor JF_1 and constitutes one source/drain region of the first transistor TR_1 and the channel forming region CH_2 of the second transistor TR_2 , and

- 5 (C-4) the other source/drain region is formed of a portion of the first region SC_1 which portion extends from the other end of the channel region CH_{J1} of the first junction-field-effect transistor JF_1 .

Concerning the second junction-field-effect transistor JF_2 ,

(D-1) the gate regions are formed of the sixth region SC_6 and part of the second region SC_2 which part is opposed to the sixth region SC_6 ,

- 15 (D-2) the channel region CH_{J2} is formed of part of the fourth region SC_4 which part is interposed between the sixth region SC_6 and said part of the second region SC_2 ,

(D-3) one source/drain region is formed of a portion of the fourth region SC_4 which portion extends from one end of the channel region CH_{J2} of the second junction-field-effect transistor JF_2 and constitutes the other source/drain region of the first transistor TR_1 , and

- 25 (D-4) the other source/drain region is formed of a portion of the fourth region SC_4 which portion extends from the other end of the channel region CH_{J2} of the second junction-field-effect transistor JF_2 .

The junction-field-effect transistors JF_1 and JF_2 are formed by

- 30 (X) optimizing the distance between the facing gate regions (the fifth region SC_5 and the third region SC_3 which is opposed to the fifth region SC_5 , that is, the thickness of the channel region CH_{J1} , and optimizing the distance between the sixth region SC_6 and the part of the second region SC_2 which part is opposed to the sixth region SC_6 , that is, the thickness of the channel region CH_{J2} , and (Y) optimizing the impurity

-319-

concentration of each of the facing gate regions (the fifth region SC_5 and the third region SC_3 which is opposed to the fifth region SC_5 , and the sixth region SC_6 and the part of the second region SC_2 which part is
5 opposed to the sixth region SC_6) and the impurity concentrations of the channel regions CH_{J1} and CH_{J2} (first region SC_1 and fourth region SC_4).

Concerning the MIS type diode DT,

(E-1) one end thereof is formed of part of the
10 second region SC_2 , and

(E-2) an electrode EL constituting the other end thereof is formed to be opposed to said part of the second region SC_2 constituting one end of the MIS type diode DT, through a wide gap thin film.

15 The gate G_1 of the first transistor TR_1 and the gate G_2 of the second transistor TR_2 are connected to a first line (word line) for memory cell selection, and the third region SC_3 is connected to a write-in information setting line WISL. Further, the portion of
20 the fourth region SC_4 which portion constitutes the other source/drain region of the second junction-field-effect transistor JF_2 is connected to a second line, the electrode EL constituting the other end of the MIS type diode DT is connected to a third line having a
25 predetermined potential, the fifth region SC_5 and the sixth region SC_6 are connected to a fifth line, and the portion of the first region SC_1 which constitutes the other source/drain region of the first junction-field-effect transistor JF_1 is connected to a fifth line. The
30 electrode EL constituting the other end of the MIS type diode DT is connected to the third line through a high-resistance element R having a resistance of approximately 10^9 to $10^{12} \Omega$. In this case, there may be employed an embodiment in which the second line to which
35 the fourth region SC_4 is connected is used as a bit line and a second predetermined potential is applied to the second line to which the fourth region SC_4 is connected,

-320-

or an embodiment in which a second predetermined potential is applied to the second line to which the fourth region SC_4 is connected and the fifth line to which the first region SC_1 is connected is used as a bit line.

Figs. 192B, 193A and 193B show schematic partial cross-sectional views of variants of the semiconductor memory cell of Example 20. In the variant shown in Fig. 192B, positions of the gate G_1 of the first transistor TR_1 and the gate G_2 of the second transistor TR_2 are nearly aligned with regard to the perpendicular direction, differing from their positional relationship in Fig. 192A. Forming such a structure serves to decrease the area of the semiconductor memory cell. In the variants shown in Figs. 193A and 193B, the supporting substrate SPS, the insulating interlayer IL_1 , the gate G_1 of the first transistor TR_1 and the gate G_2 of the second transistor TR_2 are arranged in this order from below. The positional relationship of these regions with regard to the perpendicular direction is reverse to the positional relationship of the regions of the semiconductor memory cells shown in Figs. 192A and 192B. In the variant shown in Fig. 193B, positions of the gate G_1 of the first transistor TR_1 and the gate G_2 of the second transistor TR_2 are nearly aligned with regard to the perpendicular direction, differing from their positional relationship in Fig. 193A.

Figs. 195A, 195B, 196A, 196B, 197A, 197B, 198A and 198B show schematic partial cross-sectional views of variants of the semiconductor memory cell of Example 20, and Fig. 194 shows the principle of these semiconductor memory cells. In these semiconductor memory cells, the fifth region SC_5 is connected to the write-in information setting line WISL in place of being connected to the fourth line, and the sixth region SC_6 is connected to the second region SC_2 in place of being connected to the fourth line. Being connected to the

-321-

write-in information setting line WISL is equivalent to being connected to the third region SC_3 . The fifth region SC_5 and the write-in information setting line WISL can be connected (the fifth region SC_5 and the third region SC_3 can be connected) to each other according to the method explained in Example 18. Further, the sixth region SC_6 and the second region SC_2 can be connected to each other in the same manner as in the connection of the fifth region SC_5 and the second region SC_2 explained in Example 19. The semiconductor memory cells shown in Figs. 195A, 195B, 196A and 196B are, in principle, structurally the same as the semiconductor memory cells shown in Figs. 192A and 192B, and the semiconductor memory cells shown in Figs. 197A, 197B, 198A and 198B are, in principle, structurally the same as the semiconductor memory cells shown in Figs. 193A and 193B, so that detailed explanations thereof are omitted. There may be employed an embodiment in which the second line to which the fourth region SC_4 is connected is used as a bit line and a second predetermined potential is applied to the fifth line to which the first region SC_1 is connected, or an embodiment in which the a second predetermined potential is applied to the second line to which the fourth region SC_4 is connected and the fifth line to which the first region SC_1 is connected is used as a bit line.

Example 21

Example 21 is concerned with the semiconductor memory cell according to the twenty-eighth aspect of the present invention. Fig. 132 shows the principle, Fig. 199A shows a partial schematic cross-sectional view of one example of the semiconductor memory cell of Example 21, and Fig. 199B shows a schematic layout of regions thereof. The semiconductor memory cell of Example 21 has a semiconductor layer having two main surfaces opposed to each other, the main surfaces being a first main surface A_1 and a second main

-322-

surface A_2 , and comprises;

(1) a first transistor TR_1 for readout, having a first conductivity type (for example, n-channel type), and having source/drain regions, a semi-conductive channel forming region CH_1 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G_1 capacitively coupled with the channel forming region CH_1 ,

(2) a second transistor TR_2 for switching, having a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_2 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G_2 capacitively coupled with the channel forming region CH_2 ,

(3) a third transistor TR_3 for current control, having the second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_3 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G_3 capacitively coupled with the channel forming region CH_3 ,

(4) a junction-field-effect transistor JF_1 for current control, having source/drain regions, a channel region CH_{J1} and gate regions, and

(5) an MIS type diode DT for retaining information.

That is, the semiconductor memory cell of Example 21 has a structure similar to the semiconductor memory cell according to the twenty-sixth aspect of the present invention explained in Example 19 in which the third transistor TR_3 for current control having the second conductivity type is added. In Fig. 199B, the gate G_2 and the third region SC_3 are omitted.

In the semiconductor memory cell of Example 21 shown in Fig. 199A, positions of the gate ($G_1 + G_3$) common to the first transistor TR_1 and the third transistor TR_3 (to be sometimes referred to as "common

-323-

gate ($G_1 + G_3$)" hereinafter) and the gate G_2 of the second transistor TR_2 are deviated to some extent with regard to the perpendicular direction. Further, the semiconductor memory cell has a so-called SOI structure in which it is surrounded by an insulation material layer IL_0 formed on a supporting substrate SPS. In the semiconductor memory cell of Example 21 shown in Fig. 199A, the supporting substrate SPS, an insulating interlayer IL_1 , the gate G_2 of the second transistor TR_2 and the common gate ($G_1 + G_3$) are arranged in this order from below.

In a semiconductor memory cell of Example 21, the layout of the first region SC_1 , the second region SC_2 , the third region SC_3 , the fourth region SC_4 and the fifth region SC_5 is the same as that of the semiconductor memory cell of Example 19.

The structures of the first transistor TR_1 , the second transistor TR_2 and the junction-field-effect transistor JF_1 are the same as those of the semiconductor memory cell of Example 19. The semiconductor memory cell of Example 21 differs from the semiconductor memory cell of Example 19 in that the common gate ($G_1 + G_3$) is formed on the first insulation layer formed on the first main surface A_1 so as to bridge the first region SC_1 and the fourth region SC_4 and so as to bridge the second region SC_2 and the fifth region SC_5 and is shared by the first transistor TR_1 and the third transistor TR_3 . The semiconductor memory cell of Example 21 has a constitution in which the common gate ($G_1 + G_3$) extends to an end portion of the surface region of the fourth region SC_4 . In the semiconductor memory cell of Example 21, the fifth region SC_5 can be formed in a self-aligned manner.

Concerning the third transistor TR_3 , one source/drain region constitutes the channel forming region CH_1 of the first transistor TR_1 , the other source/drain region is formed of the fifth region SC_5 ,

-324-

and the channel forming region CH_3 constitutes the other source/drain region of the first transistor TR_1 .

The junction-field-effect transistor JF_1 is formed by:

5 (X) optimizing the distance between the facing gate regions (the fifth region SC_5 and the part of the second region SC_2 which part is opposed to the fifth region SC_5), that is, the thickness of the channel region CH_{J1} , and

10 (Y) optimizing impurity concentrations of the facing gate regions (the fifth region SC_5 and the part of the second region SC_2 which part is opposed to the fifth region SC_5) and the channel region CH_{J1} (the fourth region SC_4).

15 The common gate ($G_1 + G_3$) and the gate G_2 of the second transistor TR_2 are connected to a first line (word line) for memory cell selection. The third region SC_3 is connected to a write-in information setting line WISL, the portion of the fourth region SC_4 constituting
20 the other source/drain region of the junction-field-effect transistor JF_{J1} is connected to a second line, the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential, and the first region SC_1 is
25 connected to a fourth line. The electrode EL constituting the other end of the MIS type diode DT is connected to the third line through a high-resistance element R having a resistance of approximately 10^9 to $10^{12} \Omega$. There may be employed an embodiment in which
30 the second line to which the fourth region SC_4 is connected is used as a bit line and a second predetermined potential is applied to the fourth line to which the first region SC_1 is connected, or an
35 embodiment in which the a second predetermined potential is applied to the second line to which the fourth region SC_4 is connected and the fourth line to which the first region SC_1 is connected is used as a bit line.

-325-

Figs. 200, 201A and 201B show schematic partial cross-sectional views of variants of the semiconductor memory cell of Example 21. In the variant shown in Fig. 200, positions of the common gate ($G_1 + G_3$) and the gate G_2 of the second transistor TR_2 are nearly aligned with regard to the perpendicular direction, differing from their positional relationship in Fig. 199A. Forming such a structure serves to decrease the area of the semiconductor memory cell. In the variants shown in Figs. 201A and 201B, the supporting substrate SPS, the insulating interlayer IL_1 , the common gate ($G_1 + G_3$) and the gate G_2 of the second transistor TR_2 are arranged in this order from below. The positional relationship of these regions with regard to the perpendicular direction is reverse to the positional relationship of the regions of the semiconductor memory cells shown in Figs. 199A and Fig. 200. In the variant shown in Fig. 201B, positions of the common gate ($G_1 + G_3$) and the gate G_2 of the second transistor TR_2 are nearly aligned with regard to the perpendicular direction, differing from their positional relationship in Fig. 201A.

Example 22

Example 22 is concerned with the semiconductor memory cell according to the twenty-ninth aspect of the present invention. Fig. 202 shows the principle, and Fig. 203A shows a partial schematic cross-sectional view of one example of the semiconductor memory cell of Example 22. The semiconductor memory cell of Example 22 has a semiconductor layer having two main surfaces opposed to each other, the main surfaces being a first main surface A_1 and a second main surface A_2 , and comprises;

(1) a first transistor TR_1 for readout, having a first conductivity type (for example, n-channel type), and having source/drain regions, a semi-conductive channel forming region CH_1 which is in contact with the

-326-

source/drain regions and spaces out the source/drain regions, and a gate G_1 capacitively coupled with the channel forming region CH_1 ,

(2) a second transistor TR_2 for switching, having
5 a second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_2 which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate G_2 capacitively coupled with the
10 channel forming region CH_2 ,

(3) a third transistor TR_3 for current control, having the second conductivity type (for example, p-channel type), and having source/drain regions, a semi-conductive channel forming region CH_3 which is in
15 contact with the source/drain regions and spaces out the source/drain regions, and a gate G_3 capacitively coupled with the channel forming region CH_3 ,

(4) a first junction-field-effect transistor JF_{J1} for current control, having source/drain regions, a
20 channel region CH_{J1} and gate regions,

(5) a second junction-field-effect transistor JF_{J2} for current control, having source/drain regions, a channel region CH_{J2} and gate regions, and

(6) an MIS type diode for retaining information.
25 The semiconductor memory cell of Example 22 has such a structure that the structure of the semiconductor memory cell according to the twenty-seventh aspect of the present invention explained in Example 20 is combined with the structure of the
30 semiconductor memory cell according to the twenty-eighth aspect of the present invention explained in Example 21. That is, the semiconductor memory cell of Example 22 has a structure in which a semi-conductive or conductive sixth region SC_6 is further formed, a second junction-
35 field-effect transistor JF_{J2} for current control is added and a third transistor TR_3 for current control, having the second conductivity type is further added

-327-

into the structure of the semiconductor memory cell according to the twenty-sixth aspect of the present invention.

In the semiconductor memory cell of Example 22 shown in Fig. 203A, positions of the common gate ($G_1 + G_3$) and the gate G_2 of the second transistor TR_2 are deviated to some extent with regard to the perpendicular direction. Further, the semiconductor memory cell has a so-called SOI structure in which it is surrounded by an insulation material layer IL_0 formed on a supporting substrate SPS. In the semiconductor memory cell of Example 22 shown in Fig. 203A, the supporting substrate SPS, an insulating interlayer IL_1 , the gate G_2 of the second transistor TR_2 and the common gate ($G_1 + G_3$) are arranged in this order from below.

In a semiconductor memory cell of Example 22, the layout of the first region SC_1 , the second region SC_2 , the third region SC_3 , the fourth region SC_4 , the fifth region SC_5 and the sixth region SC_6 is the same as that of the semiconductor memory cell of Example 20.

Further, the structures of the first transistor TR_1 , the second transistor TR_2 , the first junction-field-effect transistor JF_1 and the second junction-field-effect transistor JF_2 are the same as those of the semiconductor memory cell of Example 20. The semiconductor memory cell of Example 22 differs from the semiconductor memory cell of Example 20 in that the common gate ($G_1 + G_3$) is formed on the first insulation layer formed on the first main surface A_1 so as to bridge the first region SC_1 and the fourth region SC_4 and so as to bridge the second region SC_2 and the fifth region SC_5 and is shared by the first transistor TR_1 and the third transistor TR_3 , and in that the sixth region SC_6 is not connected to the fourth line.

The third transistor TR_3 has a similar structure to the semiconductor memory cell of Example 21. That is, one source/drain region constitutes the channel

-328-

forming region CH_1 of the first transistor TR_1 , the other source/drain region is formed of the sixth region SC_6 , and the channel forming region CH_3 constitutes the other source/drain region of the first transistor TR_1 .

5 The junction-field-effect transistors JF_1 and JF_{J2} are formed by:

(X) optimizing the distance between the facing gate regions (the fifth region SC_5 and the third region SC_3 which is opposed to the fifth region SC_5), that is,
10 the thickness of the channel region CH_{J1} , and optimizing the distance between the facing gate regions (the sixth region SC_6 and the part of the second region SC_2 which part is opposed to the sixth region SC_6), that is, the thickness of the channel region CH_{J2} , and

15 (Y) optimizing impurity concentrations of the facing gate regions (the fifth region SC_5 and the third region SC_3 which is opposed to the fifth region SC_5 , and the sixth region SC_6 and the part of the second region SC_2 which part is opposed to the sixth region SC_6) and
20 the channel regions CH_{J1} and CH_{J2} (the first region SC_1 and the fourth region SC_4).

The common gate ($G_1 + G_3$) and the gate G_2 of the second transistor TR_2 are connected to a first line (word line) for memory cell selection. The third region
25 SC_3 is connected to a write-in information setting line WISL, the portion of the fourth region SC_4 constituting the other source/drain region of the second junction-field-effect transistor JF_{J2} is connected to a second line, the electrode constituting the other end of the
30 MIS type diode is connected to a third line having a predetermined potential, and the fifth region SC_5 is connected to a fourth line. The electrode EL constituting the other end of the MIS type diode DT is connected to the third line through a high-resistance
35 element R having a resistance of approximately 10^9 to $10^{12} \Omega$. There may be employed an embodiment in which the second line to which the fourth region SC_4 is

-329-

connected is used as a bit line and a second predetermined potential is applied to the fifth line to which the first region SC_1 is connected, or an embodiment in which the a second predetermined potential is applied to the second line to which the fourth region SC_4 is connected and the fifth line to which the first region SC_1 is connected is used as a bit line.

Figs. 203B, 204A and 204B show schematic partial cross-sectional views of variants of the semiconductor memory cell of Example 22. In the variant shown in Fig. 203B, positions of the common gate ($G_1 + G_3$) and the gate G_2 of the second transistor TR_2 are nearly aligned with regard to the perpendicular direction, differing from their positional relationship in Fig. 203A. Forming such a structure serves to decrease the area of the semiconductor memory cell. In the variants shown in Figs. 204A and 204B, the supporting substrate SPS, the insulating interlayer IL_1 , the common gate ($G_1 + G_3$) and the gate G_2 of the second transistor TR_2 are arranged in this order from below. The positional relationship of these regions with regard to the perpendicular direction is reverse to the positional relationship of the regions of the semiconductor memory cell shown in Figs. 203A and 203B. In the variant shown in Fig. 204B, positions of the common gate ($G_1 + G_3$) and the gate G_2 of the second transistor TR_2 are nearly aligned with regard to the perpendicular direction, differing from their positional relationship in Fig. 204A.

Figs. 206A, 206B, 207A, 207B, 208A, 208B, 209A and 209B show partial schematic cross-sectional views of other variants of the semiconductor memory cell of Example 22, and Fig. 205 shows the principle thereof. In these semiconductor memory cells, the fifth region SC_5 is connected to the write-in information setting line WISL in place of being connected to the fourth line. Being connected to the write-in information setting line

-330-

WISL is equivalent being connected to the third region SC_3 . The structures of the semiconductor memory cells shown in Figs. 206A, 206B, 207A and 207B are substantially the same as those of the semiconductor memory cells shown in Figs. 203A and 203B, respectively, and the detailed description thereof is therefore omitted. Further, the structures of the semiconductor memory cells shown in Figs. 208A, 208B, 209A and 209B are substantially the same as those of the semiconductor memory cells shown in Figs. 204A and 204B, respectively, and the detailed description thereof is therefore omitted. In these cases, it is preferred that the second line is used as a bit line and a second predetermined potential is applied to the fifth line, or that a second predetermined potential is applied to the second line and the fifth line is used as a bit line.

In the semiconductor memory cell of Example 22, when an impurity containing layer having the second conductivity type (for example, p^+ -type) is formed in the surface region of the fourth region SC_4 which surface region constitutes the channel forming region CH_3 of the third transistor TR_3 , the third transistor TR_3 is brought into on-state on information retaining period in which the first line is set at, for example, 0 volt. As a result, the MIS type diode DT and the channel forming region SC_1 of the first transistor TR_1 are brought into conducted state. The impurity concentration of the impurity-containing layer is adjusted such that the third transistor TR_3 is brought into an off-state by the potential in the first line applied during the reading of information.

The operation of the semiconductor memory cell of Example 5 will be explained below. It should be noted that the principles of operation of the semiconductor memory cells of other Examples are substantially same. When the write-in information setting line also serves as the second line (for example,

-331-

bit line), the term "the write-in information setting line" in the following paragraphs is literally convertible to "the second line (for example, bit line)".

In write-in operation, potentials at
 5 portions of the semiconductor memory cell are set as shown in the following Table 8.

Table 8

10 First line for memory cell selection

: V_W

Write-in information setting line

when writing "0"(first information)

: V_0 (first potential)

15 when writing "1"(second information)

: V_1 (second potential)

In read-out operation, potentials at
 portions of the semiconductor memory cell are set as
 20 shown in the following Table 9. When the write-in
 information setting line is provided separately from the
 second line, the predetermined potential including 0
 volt is applied to the write-in information setting line.

25 Table 9

First line for memory cell selection

(for example, word line)

: V_R

Second line (for example, bit line)

: V_2

30

Further, the electrode EL constituting the
 other end of the MIS type diode DT is connected to the
 line (third line) having a predetermined potential, and
 the predetermined potential is set at V_{DD} . When the
 35 first conductivity type is n-type and the second
 conductivity type is p-type, V_{DD} is a negative value.

A threshold voltage of the first transistor

-332-

TR_1 seen from the gate G_1 is given as shown in the following Table 10. Further, the relationship among potentials in the first transistor TR_1 is set as shown in Table 10. A potential in the channel forming region
 5 CH_1 of the first transistor TR_1 when information "0" (the first information) is read out is different from that when information "1" (the second information) is read out. As a result, the threshold voltage of the first transistor TR_1 seen from the gate G_1 changes,
 10 depending upon whether the stored information is "0" or "1". When the ratio of an on-state current to an off-state current of the junction-field-effect transistor JF_1 for current control is large, the information can be read out without any error even if $|V_R| \geq |V_{TH_11}|$.

15

Table 10

When "0" (first information) is read out	: V_{TH_10}
When "1" (second information) is read out	: V_{TH_11}
20 $ V_{TH_11} > V_R > V_{TH_10} $	

[Operation to write information]

In operation to write "0" (the first information, and the potential in the write-in
 25 information setting line: V_0) or write "1" (the second information, and the potential in the write-in information setting line: V_1), the potential in the first line is set at V_W (< 0). As a result, the potential in the gate G_2 of the second transistor TR_2 is
 30 set at V_W (< 0) as well, and the second transistor TR_2 is brought into an on-state. Therefore, the potential in the channel forming region CH_1 of the first transistor TR_1 is V_0 (the first potential) when information "0" is written in, or V_1 (the second
 35 potential) when information "1" is written in. As a result, the potential in one end of the MIS type diode DT is V_0 (the first potential) when information "0" is

-333-

written in, or V_1 (the second potential) when information "1" is written in.

Meanwhile, if a current flowing in the wide gap thin film WG is greater than a reverse bias junction leak current between the second region SC_2 and the first region SC_1 , the first region SC_1 is in a steady state in which the first region SC_1 is pulled up toward the other end of the MIS type diode DT. When the wide gap thin film WG is composed of an SiO_2 or $SiON$ layer having a thickness of approximately 3 nm, and if the absolute value of a difference between V_{DD} and the potential in the first region SC_1 is 2 volts or greater (at least 2.5 volts for the necessity of carrier multiplication to be explained below), the above state is materialized.

When the potential in one end of the MIS type diode DT is at the level of V_0 (the case of information of "0") which is the first potential, and when the value of $|V_{DD}-V_0|$ is, for example, 2.5 volts or greater, electrons flow in the wide gap thin film WG from the electrode EL constituting the other end of the MIS type diode DT due to a tunnel effect (direct-tunnel phenomenon or Fowler-Nordheim tunnel phenomenon), i.e., a tunnel current flows, and the electrons are injected into the surface of the first region SC_1 . When the injected electrons have an energy which is higher than an energy gap equivalent of the first region SC_1 when viewed from the conduction band of the first region SC_1 , carrier multiplication takes place, and electron-hole pairs are generated. In Example 5, the first region SC_1 has a p-type conductivity, so that holes are stored or accumulated in a portion of the first region SC_1 (extending portion of the channel forming region CH_1 of the first transistor TR_1), and even after the second transistor TR_2 comes to be off, the first region SC_1 is retained at the level of V_0 which is the first potential or a potential close thereto. And, the injection of electrons from the electrode EL constituting the MIS

-334-

type diode DT is continued, and as a result, the carrier multiplication continues. That is, the potential in the channel forming region CH_1 of the first transistor TR_1 is retained on nearly at the first potential ($\frac{1}{2}V_0$). When the first region SC_1 is formed of a silicon containing a p-type impurity, and when the electrode EL of the MIS type diode DT is composed of a polysilicon thin layer containing an n-type impurity, the above phenomenon takes place when the value of $|V_{DD}-V_0|$ is 2.5 volts or greater. When the storing or accumulating of holes proceeds, the potential in the channel forming region CH_1 of the first transistor TR_1 sometimes comes to be higher than V_0 by approximately 0.1 to 0.2 volt when the conductivity type of the first transistor TR_1 is an n-type.

When the potential in one end of the MIS type diode DT is at the level of V_1 (the case of information of "1") which is the second potential, and when the value of $|V_{DD}-V_0|$ is equivalent to, or smaller than, the band gap of a material constituting the first region SC_1 , the carrier multiplication does not take place. Actually, even if the value of $|V_{DD}-V_0|$ equals approximately the band gap of a material constituting the first region $SC_1 + 0.5$ volt, no carrier multiplication takes place. As a result, the junction leak current between the second region SC_2 and the first region SC_1 is compensated by the transition of majority carriers (holes) in the extending portion of the channel forming region CH_1 of the first transistor TR_1 to the electrode EL through the wide gap thin film WG according to the tunnel transition, and the potential in the first region SC_1 is retained at the level of V_1 which is the second potential. That is, the channel forming region CH_1 of the first transistor TR_1 is retained on at the level of the second potential (V_1).

In operation to write information, the potential in the gate G_1 of the first transistor TR_1 is

-335-

also set at $V_w (< 0)$. As a result, the first transistor TR_1 is in an off-state. In this state, the potential in the channel forming region CH_1 of the first transistor TR_1 is V_0 when information "0" is written in, or, V_1 when
 5 information "1" is written in. This state is maintained until operation of reading out information.

In an information maintaining state after the information has been written in and before the information is read out, potentials in portions in the
 10 first transistor TR_1 and the second transistor TR_2 should be set at such values that these transistors do not conduct. For this purpose, typically, the potential in the first line is set at 0 volt and the potential in the write-in information setting line is set at V_1 .

15 [Operation to read out information]

In operation to read out the information "0" or "1", the potential in the first line is set at $V_R (> 0)$. Therefore, the potential in the gate G_2 of the second transistor TR_2 is also set at $V_R (> 0)$. As a
 20 result, the second transistor TR_2 is brought into an off-state.

The potential in the gate G_1 of the first transistor TR_1 is set at $V_R (> 0)$ as well. The threshold voltage of the first transistor TR_1 seen from the gate
 25 G_1 is V_{TH_10} or V_{TH_11} for stored information of "0" or "1", respectively. The threshold voltage of the first transistor TR_1 depends upon the state of the potential in the channel forming region CH_1 . The relationship among the potentials and the threshold voltages is as
 30 follows.

$$|V_{TH_11}| > |V_R| > |V_{TH_10}|$$

Therefore, when the stored information is "0", the first transistor TR_1 is brought into an on-state. When the stored information is "1", on the other hand, the first
 35 transistor TR_1 is brought into an off-state. However, when the ratio of an on-state current to an off-state current of the junction-field-effect transistor JF_1 is

-336-

large, the information can be read out without any error even if $|V_R| \geq |V_{TH_{11}}|$.

Further, the first transistor TR_1 for readout is controlled by the junction-field-effect transistor JF_1 on the basis of the bias conditions of the gate regions of the junction-field-effect transistor JF_1 which are constituted of the fifth region SC_5 and the first region SC . That is, when the stored information is "0", the junction-field-effect transistor JF_1 is brought into an on-state. When the stored information is "1", on the other hand, the junction-field-effect transistor JF_1 is brought into an off-state.

In the above manner, the first transistor TR_1 can be brought into an on-state or an off-state with a high degree of reliability depending upon the stored information. Since the fourth region SC_4 is connected to the second line (for example, bit line), a current flows or does not flow in the first transistor TR_1 depending upon whether the stored information is "0" or "1". As a result, the stored information can be read out by the first transistor TR_1 .

The operating states of the first transistor TR_1 for readout and the second transistor TR_2 for switching described above are summarized in Table 11. It should be noted that the values of potentials shown in Table 11 are no more than typical values, which can be any values as long as the conditions described above are satisfied.

- 337 -

Table 11

unit : volt

Write-in operation	Write-in of "0"		Write-in of "1"	
Potential in first line	V_W	-1.5	V_W	-1.5
Potential in write-in information setting line	V_0	0	V_1	-1.5
Potential in gate	V_W	-1.5	V_W	-1.5
State of TR_2	ON		ON	
Potential in channel forming region CH_1	V_0	$\cong 0$	V_1	-1.5
State of TR_1	OFF		OFF	
Potential in the other end of MIS type diode DT	-2.5			

Read-out operation	Read-out of "0"		Read-out of "1"	
Potential in first line	V_R	0.8	V_R	0.8
Potential in gate	V_R	0.8	V_R	0.8
State of TR_2	OFF		OFF	
Potential in channel forming region CH_1	V_0	0	V_1	-1.5
Threshold voltage of TR_1 seen from gate	V_{TH1_0}	0.25	V_{TH1_1}	1.3
State of TR_1	ON		OFF	
Potential in second line	V_2	0	V_2	0

-338-

The semiconductor memory cell of the present invention has been explained with reference to preferred embodiments hereinabove, while the present invention shall not be limited to those embodiments. The

5 structures of the semiconductor memory cells, and voltages, potentials, etc., in the semiconductor memory cells explained as embodiments are examples, and may be changed as required. For example, in the semiconductor memory cells explained as embodiments, the first

10 transistor for readout and the junction-field-effect transistor(s) JF_1 , JF_2 may be p-type transistors, and the second transistor for switching and the third transistor for current control may be n-type transistors. In this case, further, it is sufficient to reverse the

15 relationship of holes and electrons and the polarity of V_{DD} (predetermined potential in the line (third line) to which the electrode constituting the other end of the MIS type diode is connected) with regard to the MIS type diode DT. The layout of elements in each transistor is

20 an example, and may be changed as required. The SOI structure shown in Figs. 52 and 73 and so on and the TFT structure can be applied to the semiconductor memory cell of the present invention. An impurity may be introduced into each region not only by an ion-

25 implanting method but also by a solid-phase diffusion method. Further, the present invention can be applied not only to a semiconductor memory cell composed of a silicon semiconductor but also to a semiconductor memory cell composed of a compound semiconductor, for example,

30 of a GaAs system. Moreover, the semiconductor memory cell of the present invention can be applied to a semiconductor memory cell having an MES FET structure.

In the present invention, the MIS type diode for retaining information is provided, and the potential

35 in the channel forming region of the first transistor can be retained on during writing the information into the semiconductor memory cell, so that the refreshing

-339-

operation required in a conventional DRAM is no longer required.

Further, an extremely large capacitor required in a conventional DRAM is no longer required.

5 Further, the semiconductor memory cell having the MIS type diode for retaining information, provided by the present invention, can be integrated into only two transistor regions. The semiconductor memory cell of the present invention can be manufactured by a CMOS
10 logic circuit manufacturing process with increasing a few steps alone.

Further, when the junction-field-effect transistor for current control is provided, the junction-field-effect transistor for current control is
15 controlled to turn on/off during the reading of information, so that the margin of a current to flow between the second region and the third region can be remarkably broadened. As a result, the number of semiconductor memory cells which are connected to a bit
20 line is less limited, and the time period for retaining information in the semiconductor memory cell (retention time) can be increased. Further, when the third transistor is provided, the gate is structured so as to extend up to an end of the surface region of the fourth
25 region, and, for example, the sixth region can be formed in a self-alignment manner, so that the area of the semiconductor memory cell can be further decreased.

* * * * *

- 340 -

WHAT IS CLAIMED IS:

1. A semiconductor memory cell comprising;
 - (1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,
 - (2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region, and
 - (3) an MIS type diode for retaining information,wherein:
 - one source/drain region of the first transistor corresponds to the channel forming region of the second transistor,
 - one source/drain region of the second transistor corresponds to the channel forming region of the first transistor, and
 - one end of the MIS type diode is formed of an extending portion of the channel forming region of the first transistor, the other end of the MIS type diode is formed of an electrode composed of an electrically conductive material, and the electrode is connected to a line having a predetermined potential.
2. The semi-conductor memory cell according to claim 1, wherein a material is interposed between one end and the other end of the MIS diode, in which material the tunnel transition of carriers is caused depending upon a potential difference between the potential in the channel forming region of the first

- 341 -

transistor and the potential in the other end of the MIS type diode.

3. The semi-conductor memory cell according to claim 2, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the channel forming region of the first transistor depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

4. The semi-conductor memory cell according to claim 1, wherein the gate of the first transistor and the gate of the second transistor are connected to a word line,

the other source/drain region of the first transistor is connected to a bit line,

- 342 -

the other source/drain region of the second transistor is connected to a write-in information setting line, and

the other end of the MIS type diode is connected to the line having a predetermined potential through a high-resistance element.

5. The semi-conductor memory cell according to claim 1, wherein the gate of the first transistor and the gate of the second transistor are connected to a word line,

one source/drain region of the first transistor is connected to a bit line,

the other source/drain region of the second transistor is connected to a write-in information setting line, and

the other end of the MIS type diode is connected to the line having a predetermined potential through a high-resistance element.

6. The semi-conductor memory cell according to claim 1, wherein a diode is further provided,

the gate of the first transistor and the gate of the second transistor are connected to a word line,

one source/drain region of the first transistor is connected to a write-in information setting line through the diode,

the other source/drain region of the first transistor is connected to a bit line,

the other source/drain region of the second transistor is connected to the write-in information setting line, and

the other end of the MIS type diode is connected to the line having a predetermined potential through a high-resistance element.

- 343 -

7. The semi-conductor memory cell according to claim 1, wherein a diode is further provided,

a write-in information setting line functions as a bit line,

the gate of the first transistor and the gate of the second transistor are connected to a word line,

one source/drain region of the first transistor is connected to the write-in information setting line through the diode,

the other source/drain region of the second transistor is connected to the write-in information setting line, and

the other end of the MIS type diode is connected to the line having a predetermined potential through a high-resistance element.

8. The semiconductor memory cell according to claim 1, wherein the first transistor and the second transistor have a common gate.

9. The semiconductor memory cell according to claim 1, wherein a wide gap thin film is formed between the extending portion of channel forming region of the first transistor constituting the MIS type diode and the electrode.

10. A semiconductor memory cell comprising;

(1) a first transistor for readout, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming

- 344 -

region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region, and

(3) an MIS type diode for retaining information,

the semiconductor memory cell having;

(a) a semi-conductive first region having a first conductivity type,

(b) a semi-conductive second region being in contact with the first region and having a second conductivity type,

(c) a third region which is formed in a surface region of the first region to be spaced from the second region and is in contact with the first region so as to form a rectifier junction together with the first region, and

(d) a fourth region which is formed in a surface region of the second region to be spaced from the first region and is in contact with the second region so as to form a rectifier junction together with the second region,

wherein:

(A-1) one source/drain region of the first transistor is formed of a surface region of the first region which surface region is interposed between the second region and the third region,

(A-2) the other source/drain region of the first transistor is formed of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a surface region of the second region which surface region is interposed between the surface region of the first region and the fourth region,

(A-4) the gate of the first transistor is formed on the channel forming region of the first transistor through an insulation layer,

- 345 -

(B-1) one source/drain region of the second transistor is formed of the surface region of the second region which surface region constitutes the channel forming region of the first transistor,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of the surface region of the first region which surface region constitutes one source/drain region of the first transistor,

(B-4) the gate of the second transistor is formed on the channel forming region of the second transistor through an insulation layer,

(C-1) one end of the MIS type diode is formed of part of the second region,

(C-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to said part of the second region constituting one end of the MIS type diode, through a wide gap thin film,

(D) the gate of the first transistor and the gate of the second transistor are connected to a first line for memory cell selection,

(E) the third region is connected to a write-in information setting line,

(F) the fourth region is connected to a second line,

(G) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential, and

(H) the first region is connected to a fourth line.

11. The semiconductor memory cell according to claim 10, wherein the electrode is connected to the third line through a high-resistance element.

12. The semiconductor memory cell according to

- 346 -

claim 11, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

13. The semiconductor memory cell according to claim 10, wherein the gate of the first transistor and the gate of the second transistor are formed so as to bridge the first region and the fourth region and so as to bridge the second region and third region through the insulation layer, and are shared by the first transistor and the second transistor.

14. The semiconductor memory cell according to claim 10, wherein the first region and the third region constitute a diode, and

the first region is connected to the write-in information setting line through the third region in place of being connected to the fourth line.

15. The semiconductor memory cell according to claim 10, wherein a majority carrier-diode comprising the first region and a diode-constituting region provided in a surface region of the first region is further provided, and

the first region is connected to the write-in information setting line through the diode-constituting region in place of being connected to the fourth line.

16. The semiconductor memory cell according to claim 10, wherein the second region is formed in a surface region of the first region.

17. The semiconductor memory cell according to claim 10, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the

- 347 -

potential in the channel forming region of the first transistor and the potential in the other end of the MIS type diode.

18. The semi-conductor memory cell according to claim 17, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the channel forming region of the first transistor depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

19. A semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the

- 348 -

source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region, and

(3) an MIS type diode for retaining information,

the semiconductor memory cell having;

(a) a semi-conductive first region having a first conductivity type,

(b) a semi-conductive second region being in contact with the first region and having a second conductivity type,

(c) a third region which is formed in a surface region of the first region to be spaced from the second region and is in contact with the first region so as to form a rectifier junction together with the first region,

(d) a semi-conductive fourth region which is formed in a surface region of the second region to be spaced from the first region and has the first conductivity type, and

(e) a semi-conductive MIS-type-diode constituting region which is formed in a surface region of the fourth region and has the second conductivity type,

wherein:

(A-1) one source/drain region of the first transistor is formed of a surface region of the first region which surface region is interposed between the second region and the third region,

(A-2) the other source/drain region of the first transistor is formed of the fourth region,

- 349 -

(A-3) the channel forming region of the first transistor is formed of a surface region of the second region which surface region is interposed between the surface region of the first region and the fourth region,

(A-4) the gate of the first transistor is formed on the channel forming region of the first transistor through an insulation layer,

(B-1) one source/drain region of the second transistor is formed of the surface region of the second region which surface region constitutes the channel forming region of the first transistor,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of the surface region of the first region which surface region constitutes one source/drain region of the first transistor,

(B-4) the gate of the second transistor is formed on the channel forming region of the second transistor through an insulation layer,

(C-1) one end of the MIS type diode is formed of the MIS-type-diode-constituting region,

(C-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to the MIS-type-diode-constituting region constituting one end of the MIS type diode, through a wide gap thin film,

(D) the gate of the first transistor and the gate of the second transistor are connected to a first line for memory cell selection,

(E) the second region is connected to the MIS-type-diode-constituting region,

(F) the third region is connected to a write-in information setting line,

(G) the fourth region is connected to a second line,

(H) the electrode constituting the other end

- 350 -

of the MIS type diode is connected to a third line having a predetermined potential, and

(I) the first region is connected to a fourth line.

20. The semi-conductor memory cell according to claim 19, wherein the electrode is connected to the third line through a high-resistance element.

21. The semi-conductor memory cell according to claim 20, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

22. The semi-conductor memory cell according to claim 19, wherein the gate of the first transistor and the gate of the second transistor are formed so as to bridge the first region and the fourth region and so as to bridge the second region and third region through the insulation layer, and are shared by the first transistor and the second transistor.

23. The semi-conductor memory cell according to claim 19, wherein the first region and the third region constitute a diode, and

the first region is connected to the write-in information setting line through the third region in place of being connected to the fourth line.

24. The semi-conductor memory cell according to claim 19, wherein a majority carrier-diode comprising the first region and a diode-constituting region provided in a surface region of the first region is further provided, and

the first region is connected to the write-in information setting line through the diode-constituting region in place of being connected to the

- 351 -

fourth line.

25. The semi-conductor memory cell according to claim 19, wherein the second region is formed in a surface region of the first region.

26. The semi-conductor memory cell according to claim 19, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the channel forming region of the first transistor and the potential in the other end of the MIS type diode.

27. The semi-conductor memory cell according to claim 26, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the channel forming region of the first transistor depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that

- 352 -

of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

28. A semiconductor memory cell having a semiconductor layer having two main surfaces opposed to each other, the main surfaces being a first main surface and a second main surface,

the semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region, and

(3) an MIS type diode for retaining information,

the semiconductor memory cell further having;

(a) a semi-conductive first region which is formed in the semiconductor layer to extend over from the first main surface to the second main surface and has a first conductivity type,

(b) a semi-conductive second region which is formed in the semiconductor layer to extend over from the first main surface to the second main surface, is in contact with the first region and has a second conductivity type,

(c) a third region which is formed in a

- 353 -

surface region including the second main surface of the first region to be spaced from the second region and is in contact with the first region so as to form a rectifier junction together with the first region,

(d) a fourth region which is formed in a surface region including the first main surface of the second region to be spaced from the first region and is in contact with the second region so as to form a rectifier junction together with the second region,

(e) the gate of the first transistor formed on a first insulation layer formed on the first main surface so as to bridge the first region and the fourth region, and

(f) the gate of the second transistor formed on a second insulation layer formed on the second main surface so as to bridge the second region and the third region,

wherein:

(A-1) one source/drain region of the first transistor is formed of a surface region including the first main surface of the first region,

(A-2) the other source/drain region of the first transistor is formed of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a surface region including the first main surface of the second region which surface region is interposed between the surface region including the first main surface of the first region and the fourth region,

(B-1) one source/drain region of the second transistor is formed of a surface region including the second main surface of the second region,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of a surface region including the second main surface of the first region

- 354 -

which surface region is interposed between the surface region including the second main surface of the second region and the third region,

(C-1) one end of the MIS type diode is formed of part of the second region,

(C-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to said part of the second region constituting one end of the MIS type diode, through a wide gap thin film,

(D) the gate of the first transistor and the gate of the second transistor are connected to a first line for memory cell selection,

(E) the third region is connected to a write-in information setting line,

(F) the fourth region is connected to a second line,

(G) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential, and

(H) the first region is connected to a fourth line.

29. The semi-conductor memory cell according to claim 28, wherein the first region and the third region constitute a diode, and

the first region is connected to the write-in information setting line through the third region in place of being connected to the fourth line.

30. The semi-conductor memory cell according to claim 28, wherein the electrode is connected to the third line through a high-resistance element.

31. The semi-conductor memory cell according to claim 30, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

- 355 -

32. The semi-conductor memory cell according to claim 28, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the channel forming region of the first transistor and the potential in the other end of the MIS type diode.

33. The semi-conductor memory cell according to claim 32, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the channel forming region of the first transistor depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

- 356 -

34. A semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(4) an MIS type diode for retaining information,

wherein:

one source/drain region of the first transistor corresponds to the channel forming region of the second transistor and corresponds to one source/drain region of the junction-field-effect transistor,

one source/drain region of the second transistor corresponds to the channel forming region of the first transistor and corresponds to one gate region of the junction-field-effect transistor, and

one end of the MIS type diode is formed of an extending portion of the channel forming region of the first transistor, the other end of the MIS type diode is formed of an electrode composed of a conductive material, and the electrode is connected to a line having a predetermined potential.

35. The semi-conductor memory cell according to claim 34, wherein a material is interposed between one

- 357 -

end and the other end of the MIS diode, in which material the tunnel transition of carriers is caused depending upon a potential difference between the potential in the channel forming region of the first transistor and the potential in the other end of the MIS type diode.

36. The semiconductor memory cell according to claim 35, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the extending portion of the channel forming region of the first transistor depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

37. The semiconductor memory cell according to

- 358 -

claim 34, wherein the gate of the first transistor and the gate of the second transistor are connected to a first line for memory cell selection,

the other source/drain region of the first transistor is connected to a second line,

the other end of the MIS type diode is connected to a third line corresponding to said line having a predetermined potential through a high-resistance element,

the other gate region of the junction-field-effect transistor is connected to a fourth line,

one source/drain region of the first transistor is connected to a fifth line through the junction-field-effect transistor, and

the other source/drain region of the second transistor is connected to a write-in information setting line.

38. The semiconductor memory cell according to claim 37, wherein one source/drain region of the first transistor is connected to the write-in information setting line through the junction-field-effect transistor and a diode in place of being connected to the fifth line through the junction-field-effect transistor.

39. The semiconductor memory cell according to claim 37, wherein the other gate region of the junction-field-effect transistor is connected to the write-in information setting line in place of being connected to the fourth line.

40. The semi-conductor memory cell according to claim 39, wherein one source/drain region of the first transistor is connected to the write-in information setting line through the junction-field-effect transistor and a diode in place of being connected to

- 359 -

the fifth line through the junction-field-effect transistor.

41. The semiconductor memory cell according to claim 37, wherein one source/drain region of the first transistor is connected to the fourth line through the junction-field-effect transistor and a diode in place of being connected to the fifth line through the junction-field-effect transistor.

42. The semiconductor memory cell according to claim 37, wherein the other gate region of the junction-field-effect transistor is connected to one gate region of the junction-field-effect transistor in place of being connected to the fourth line.

43. The semi-conductor memory cell according to claim 42, wherein one source/drain region of the first transistor is connected to the write-in information setting line through the junction-field-effect transistor and a diode in place of being connected to the fifth line through the junction-field-effect transistor.

44. The semi-conductor memory cell according to claim 34, wherein the first transistor and the second transistor have a common gate.

45. The semi-conductor memory cell according to claim 34, wherein a wide gap thin film is formed between the extending portion of channel forming region of the first transistor constituting the MIS type diode and the electrode.

46. A semiconductor memory cell comprising;
(1) a first transistor for readout, having a first conductivity type, and having source/drain regions,

- 360 -

a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(4) an MIS type diode for retaining information,

wherein:

one source/drain region of the first transistor corresponds to the channel forming region of the second transistor,

the other source/drain region of the first transistor corresponds to one source/drain region of the junction-field-effect transistor,

one source/drain region of the second transistor corresponds to the channel forming region of the first transistor and corresponds to one gate region of the junction-field-effect transistor, and

one end of the MIS type diode is formed of an extending portion of the channel forming region of the first transistor, the other end of the MIS type diode is formed of an electrode composed of a conductive material, and the electrode is connected to a line having a predetermined potential.

47. The semi-conductor memory cell according to claim 46, wherein a material is interposed between one end and the other end of the MIS diode, in which material the tunnel transition of carriers is caused

- 361 -

depending upon a potential difference between the potential in the channel forming region of the first transistor and the potential in the other end of the MIS type diode.

48. The semi-conductor memory cell according to claim 47, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the extending portion of the channel forming region of the first transistor depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

49. The semiconductor memory cell according to claim 46, wherein the gate of the first transistor and the gate of the second transistor are connected to a

- 362 -

first line for memory cell selection,

the other source/drain region of the first transistor is connected to a second line through the junction-field-effect transistor,

the other end of the MIS type diode is connected to a third line corresponding to said line having a predetermined potential through a high-resistance element,

the other gate region of the junction-field-effect transistor is connected to a fourth line,

one source/drain region of the first transistor is connected to a fifth line, and

the other source/drain region of the second transistor is connected to a write-in information setting line.

50. The semiconductor memory cell according to claim 49, wherein one source/drain region of the first transistor is connected to the write-in information setting line through a diode in place of being connected to the fifth line.

51. The semi-conductor memory cell according to claim 49, wherein the other gate region of the junction-field-effect transistor is connected to the write-in information setting line in place of being connected to the fourth line.

52. The semi-conductor memory cell according to claim 51, wherein one source/drain region of the first transistor is connected to the write-in information setting line through a diode in place of being connected to the fifth line.

53. The semi-conductor memory cell according to claim 49, wherein the other gate region of the junction-field-effect transistor is connected to one gate region

- 363 -

of the junction-field-effect transistor in place of being connected to the fourth line.

54. The semi-conductor memory cell according to claim 53, wherein one source/drain region of the first transistor is connected to the write-in information setting line through a diode in place of being connected to the fifth line.

55. The semi-conductor memory cell according to claim 46, wherein the first transistor and the second transistor have a common gate.

56. The semi-conductor memory cell according to claim 46, wherein a wide gap thin film is formed between the extending portion of channel forming region of the first transistor constituting the MIS type diode and the electrode.

57. A semiconductor memory cell comprising;
(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,
(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,
(3) a third transistor for current control, having the second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate

- 364 -

capacitively coupled with the channel forming region,

(4) a junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(5) an MIS type diode for retaining information,

wherein:

one source/drain region of the first transistor corresponds to the channel forming region of the second transistor,

the other source/drain region of the first transistor corresponds to one source/drain region of the junction-field-effect transistor,

one source/drain region of the second transistor corresponds to the channel forming region of the first transistor, corresponds to one gate region of the junction-field-effect transistor and corresponds to one source/drain region of the third transistor,

the other source/drain region of the third transistor corresponds to the other gate region of the junction-field-effect transistor, and

one end of the MIS type diode is formed of an extending portion of the channel forming region of the first transistor, the other end of the MIS type diode is formed of an electrode composed of a conductive material, and the electrode is connected to a line having a predetermined potential.

58. The semi-conductor memory cell according to claim 57, wherein a material is interposed between one end and the other end of the MIS diode, in which material the tunnel transition of carriers is caused depending upon a potential difference between the potential in the channel forming region of the first transistor and the potential in the other end of the MIS type diode.

- 365 -

59. The semi-conductor memory cell according to claim 58, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the extending portion of the channel forming region of the first transistor depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

60. The semi-conductor memory cell according to claim 57, wherein the gate of the first transistor, the gate of the second transistor and the gate of the third transistor are connected to a first line for memory cell selection,

the other source/drain region of the first transistor is connected to a second line through the junction-field-effect transistor,

- 366 -

the other end of the MIS type diode is connected to a third line corresponding to said line having a predetermined potential through a high-resistance element,

one source/drain region of the first transistor is connected to a fourth line, and

the other source/drain region of the second transistor is connected to a write-in information setting line.

61. The semi-conductor memory cell according to claim 60, wherein one source/drain region of the first transistor is connected to the write-in information setting line through a diode in place of being connected to the fourth line.

62. The semi-conductor memory cell according to claim 57, wherein the first transistor, the second transistor and the third transistor have a common gate.

63. The semi-conductor memory cell according to claim 57, wherein a wide gap thin film is formed between the extending portion of channel forming region of the first transistor constituting the MIS type diode and the electrode.

64. A semiconductor memory cell comprising;
(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions

- 367 -

and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a third transistor for current control, having the second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(4) a junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(5) an MIS type diode for retaining information,

wherein:

one source/drain region of the first transistor corresponds to the channel forming region of the second transistor,

the other source/drain region of the first transistor corresponds to one source/drain region of the junction-field-effect transistor,

one source/drain region of the second transistor corresponds to the channel forming region of the first transistor, corresponds to one gate region of the junction-field-effect transistor and corresponds to one source/drain region of the third transistor,

the other source/drain region of the third transistor corresponds to the other gate region of the junction-field-effect transistor, and

one end of the MIS type diode corresponds to the other source/drain region of the third transistor, the other end of the MIS type diode is formed of an electrode composed of a conductive material, and the electrode is connected to a line having a predetermined potential.

65. The semi-conductor memory cell according to claim 64, wherein a material is interposed between one

- 368 -

end and the other end of the MIS type diode, in which material the tunnel transition of carriers is caused depending upon a potential difference between the potential in the other source/drain region of the third transistor and the potential in the other end of the MIS type diode.

66. The semiconductor memory cell according to claim 65, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the other source/drain region of the third transistor depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

67. The semi-conductor memory cell according to claim 64, wherein the gate of the first transistor, the

- 369 -

gate of the second transistor and the gate of the third transistor are connected to a first line for memory cell selection,

the other source/drain region of the first transistor is connected to a second line through the junction-field-effect transistor,

the other end of the MIS type diode is connected to a third line corresponding to said line having a predetermined potential through a high-resistance element,

one source/drain region of the first transistor is connected to a fourth line, and

the other source/drain region of the second transistor is connected to a write-in information setting line.

68. The semi-conductor memory cell according to claim 67, wherein one source/drain region of the first transistor is connected to the write-in information setting line through a diode in place of being connected to the fourth line.

69. The semi-conductor memory cell according to claim 64, wherein the first transistor, the second transistor and the third transistor have a common gate.

70. The semi-conductor memory cell according to claim 64, wherein a wide gap thin film is formed between the other source/drain region of the third transistor constituting the MIS type diode and the electrode.

71. A semiconductor memory cell comprising;
(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled

- 370 -

with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a first junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions,

(4) a second junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(5) an MIS type diode for retaining information,

wherein:

one source/drain region of the first transistor corresponds to the channel forming region of the second transistor and corresponds to one source/drain region of the first junction-field-effect transistor,

the other source/drain region of the first transistor corresponds to one source/drain region of the second junction-field-effect transistor,

one source/drain region of the second transistor corresponds to the channel forming region of the first transistor, corresponds to one gate region of the first junction-field-effect transistor and corresponds to one gate region of the second junction-field-effect transistor, and

one end of the MIS type diode is formed of an extending portion of the channel forming region of the first transistor, the other end of the MIS type diode is formed of an electrode composed of a conductive material, and the electrode is connected to a line having a predetermined potential.

- 371 -

72. The semi-conductor memory cell according to claim 71, wherein a material is interposed between one end and the other end of the MIS diode, in which material the tunnel transition of carriers is caused depending upon a potential difference between the potential in the channel forming region of the first transistor and the potential in the other end of the MIS type diode.

73. The semi-conductor memory cell according to claim 72, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the extending portion of the channel forming region of the first transistor depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

- 372 -

74. The semi-conductor memory cell according to claim 71, wherein the gate of the first transistor and the gate of the second transistor are connected to a first line for memory cell selection,

the other source/drain region of the first transistor is connected to a second line through the second junction-field-effect transistor,

the other end of the MIS type diode is connected to a third line corresponding to said line having a predetermined potential through a high-resistance element,

the other gate region of the second junction-field-effect transistor is connected to a fourth line,

one source/drain region of the first transistor is connected to a fifth line through the first junction-field-effect transistor,

the other gate region of the first junction-field-effect transistor is connected to a write-in information setting line, and

the other source/drain region of the second transistor is connected to the write-in information setting line.

75. The semi-conductor memory cell according to claim 74, wherein one source/drain region of the first transistor is connected to the write-in information setting line through the first junction-field-effect transistor and a diode in place of being connected to the fifth line through the first junction-field-effect transistor.

76. The semi-conductor memory cell according to claim 74, wherein the other gate region of the second junction-field-effect transistor is connected to one gate region of the second junction-field-effect

- 373 -

transistor in place of being connected to the fourth line.

77. The semi-conductor memory cell according to claim 76, wherein one source/drain region of the first transistor is connected to the write-in information setting line through the first junction-field-effect transistor and a diode in place of being connected to the fifth line through the first junction-field-effect transistor.

78. The semi-conductor memory cell according to claim 71, wherein the first transistor and the second transistor have a common gate.

79. The semi-conductor memory cell according to claim 71, wherein a wide gap thin film is formed between the extending portion of channel forming region of the first transistor constituting the MIS type diode and the electrode.

80. A semiconductor memory cell comprising;
(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a third transistor for current control, having the second conductivity type, and having source/drain regions, a semi-conductive channel forming

- 374 -

region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(4) a first junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions,

(5) a second junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(6) an MIS type diode for retaining information,

wherein:

one source/drain region of the first transistor corresponds to the channel forming region of the second transistor and corresponds to one source/drain region of the first junction-field-effect transistor,

the other source/drain region of the first transistor corresponds to one source/drain region of the second junction-field-effect transistor,

one source/drain region of the second transistor corresponds to the channel forming region of the first transistor, corresponds to one gate region of the first junction-field-effect transistor, corresponds to one gate region of the second junction-field-effect transistor and corresponds to one source/drain region of the third transistor,

the other source/drain region of the third transistor corresponds to the other gate region of the second junction-field-effect transistor, and

one end of the MIS type diode is formed of an extending portion of the channel forming region of the first transistor, the other end of the MIS type diode is formed of an electrode composed of a conductive material, and the electrode is connected to a line having a predetermined potential.

- 375 -

81. The semi-conductor memory cell according to claim 80, wherein a material is interposed between one end and the other end of the MIS diode, in which material the tunnel transition of carriers is caused depending upon a potential difference between the potential in the channel forming region of the first transistor and the potential in the other end of the MIS type diode.

82. The semi-conductor memory cell according to claim 81, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the extending portion of the channel forming region of the first transistor depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

- 376 -

83. The semi-conductor memory cell according to claim 80, wherein the first transistor, the second transistor and the third transistor have a common gate.

84. The semi-conductor memory cell according to claim 80, wherein a wide gap thin film is formed between the extending portion of channel forming region of the first transistor constituting the MIS type diode and the electrode.

85. The semi-conductor memory cell according to claim 80, wherein the gate of the first transistor, the gate of the second transistor and the gate of the third transistor are connected to a first line for memory cell selection,

the other source/drain region of the first transistor is connected to a second line through the second junction-field-effect transistor,

the other end of the MIS type diode is connected to a third line corresponding to said line having a predetermined potential through a high-resistance element,

one source/drain region of the first transistor is connected to a fourth line through the first junction-field-effect transistor,

the other source/drain region of the second transistor is connected to a write-in information setting line, and

the other gate region of the first junction-field-effect transistor is connected to the write-in information setting line.

86. The semi-conductor memory cell according to claim 85, wherein one source/drain region of the first transistor is connected to the write-in information setting line through the first junction-field-effect

- 377 -

transistor and a diode in place of being connected to the fourth line through the first junction-field-effect transistor.

87. A semi-conductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a third transistor for current control, having the second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(4) a first junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions,

(5) a second junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(6) an MIS type diode for retaining information,

wherein:

one source/drain region of the first transistor corresponds to the channel forming region of the second transistor and corresponds to one source/drain region of the first junction-field-effect transistor,

- 378 -

the other source/drain region of the first transistor corresponds to one source/drain region of the second junction-field-effect transistor,

one source/drain region of the second transistor corresponds to channel forming region of the first transistor, corresponds to one gate region of the first junction-field-effect transistor, corresponds to one gate region of the second junction-field-effect transistor and corresponds to one source/drain region of the third transistor,

the other source/drain region of the third transistor corresponds to the other gate region of the second junction-field-effect transistor, and

one end of the MIS type diode corresponds to the other source/drain region of the third transistor, the other end of the MIS type diode is formed of an electrode composed of a conductive material, and the electrode is connected to a line having a predetermined potential.

88. The semi-conductor memory cell according to claim 87, wherein a material is interposed between one end and the other end of the MIS type diode, in which material the tunnel transition of carriers is caused depending upon a potential difference between the potential in the other source/drain region of the third transistor and the potential in the other end of the MIS type diode.

89. The semi-conductor memory cell according to claim 88, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a

- 379 -

second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the other source/drain region of the third transistor depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

90. The semi-conductor memory cell according to claim 87, wherein the first transistor, the second transistor and the third transistor have a common gate.

91. The semi-conductor memory cell according to claim 87, wherein a wide gap thin film is formed between the other source/drain region of the third transistor constituting the MIS type diode and the electrode.

92. The semi-conductor memory cell according to claim 87, wherein the gate of the first transistor, the gate of the second transistor and the gate of the third transistor are connected to a first line for memory cell selection,

the other source/drain region of the first transistor is connected to a second line through the second junction-field-effect transistor,

- 380 -

the other end of the MIS type diode is connected to a third line corresponding to said line having a predetermined potential through a high-resistance element,

one source/drain region of the first transistor is connected to a fourth line through the first junction-field-effect transistor,

the other source/drain region of the second transistor is connected to a write-in information setting line, and

the other gate region of the first junction-field-effect transistor is connected to the write-in information setting line.

93. The semi-conductor memory cell according to claim 92, wherein one source/drain region of the first transistor is connected to the write-in information setting line through the first junction-field-effect transistor and a diode in place of being connected to the fourth line through the first junction-field-effect transistor.

94. A semiconductor memory cell comprising;
(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a junction-field-effect transistor for current control, having source/drain regions, a channel

- 381 -

region and gate regions, and

(4) an MIS type diode for retaining information,

the semiconductor memory cell having;

(a) a semi-conductive first region having a second conductivity type,

(b) a semi-conductive second region which is formed in a surface region of the first region and has a first conductivity type,

(c) a third region which is formed in a surface region of the second region and is in contact with the second region so as to form a rectifier junction together with the second region,

(d) a fourth region which is formed in a surface region of the first region to be spaced from the second region and is in contact with the first region so as to form a rectifier junction together with the first region, and

(e) a fifth region which is formed in a surface region of the second region to be spaced from the third region and is in contact with the second region so as to form a rectifier junction together with the second region,

wherein:

(A-1) one source/drain region of the first transistor is formed of a portion of a surface region of the second region,

(A-2) the other source/drain region of the first transistor is formed of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a portion of a surface region of the first region which portion is interposed between said portion of the surface region of the second region and the fourth region,

(A-4) the gate of the first transistor is formed on the channel forming region of the first transistor through an insulation layer,

- 382 -

(B-1) one source/drain region of the second transistor is formed of other portion of the surface region of the first region,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of other portion of the surface region of the second region which other portion is interposed between said other portion of the surface region of the first region and the third region,

(B-4) the gate of the second transistor is formed on the channel forming region of the second transistor through an insulation layer,

(C-1) the gate regions of the junction-field-effect transistor are formed of the fifth region and part of the first region which part is opposed to the fifth region,

(C-2) the channel region of the junction-field-effect transistor is formed of part of the second region which part is interposed between the fifth region and said part of the first region,

(C-3) one source/drain region of the junction-field-effect transistor is formed of said portion of the surface region of the second region which portion extends from one end of the channel region of the junction-field-effect transistor and constitutes one source/drain region of the first transistor,

(C-4) the other source/drain region of the junction-field-effect transistor is formed of a portion of the second region which portion extends from the other end of the channel region of the junction-field-effect transistor,

(D-1) one end of the MIS type diode is formed of part of the first region,

(D-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to said part of the first region constituting one end of

- 383 -

the MIS type diode, through a wide gap thin film,

(E) the gate of the first transistor and the gate of the second transistor are connected to a first line for memory cell selection,

(F) the third region is connected to a write-in information setting line,

(G) the fourth region is connected to a second line,

(H) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential, and

(I) the fifth region is connected to a fourth line.

95. The semi-conductor memory cell according to claim 94, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

96. The semi-conductor memory cell according to claim 95, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

97. The semi-conductor memory cell according to claim 94, wherein the second region and the third region constitute a diode, and the second region is connected to the write-in information setting line through the third region.

98. The semi-conductor memory cell according to claim 94, wherein further provided is a diode-constituting-region which is formed in a surface region of the second region and is in contact with the second region so as to form a rectifier junction together with the second region,

a majority carrier diode comprises the

- 384 -

diode-constituting-region and the second region, and
the second region is connected to the write-in information setting line through the diode-constituting region.

99. The semi-conductor memory cell according to claim 94, wherein further provided is a diode-constituting region which is formed in a surface region of the second region and is in contact with the second region so as to form a rectifier junction together with the second region,

a diode comprises the diode-constituting region and the second region, and

the second region is connected to the fourth line through the diode-constituting region.

100. The semi-conductor memory cell according to claim 94, wherein the fifth region is connected to the first region in place of being connected to the fourth region.

101. The semi-conductor memory cell according to claim 100, wherein the second region and the third region constitute a diode, and the second region is connected to the write-in information setting line through the third region.

102. The semi-conductor memory cell according to claim 100, wherein further provided is a diode-constituting-region which is formed in a surface region of the second region and is in contact with the second region so as to form a rectifier junction together with the second region,

a majority carrier diode comprises the diode-constituting-region and the second region, and

the second region is connected to the write-in information setting line through the diode-

- 385 -

constituting region.

103. The semi-conductor memory cell according to claim 94, wherein the fifth region is connected to the first region in place of being connected to the fourth region.

104. The semi-conductor memory cell according to claim 103, wherein the second region and the third region constitute a diode, and the second region is connected to the write-in information setting line through the third region.

105. The semi-conductor memory cell according to claim 103, wherein further provided is a diode-constituting-region which is formed in a surface region of the second region and is in contact with the second region so as to form a rectifier junction together with the second region,

a majority carrier diode comprises the diode-constituting-region and the second region, and the second region is connected to the write-in information setting line through the diode-constituting region.

106. The semi-conductor memory cell according to claim 94, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the first region and the potential in the other end of the MIS type diode.

107. The semiconductor memory cell according to claim 106, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a

- 386 -

first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the portion of the first region constituting one end of the MIS type diode depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

108. A semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

- 387 -

(3) a junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(4) an MIS type diode for retaining information,

the semiconductor memory cell having;

(a) a semi-conductive first region having a second conductivity type,

(b) a semi-conductive second region which is formed in a surface region of the first region and has a first conductivity type,

(c) a third region which is formed in a surface region of the second region and is in contact with the second region so as to form a rectifier junction together with the second region,

(d) a fourth region which is formed in a surface region of the first region to be spaced from the second region and is in contact with the first region so as to form a rectifier junction together with the first region, and

(e) a semi-conductive fifth region which is formed in a surface region of the second region to be spaced from the third region and has the second conductivity type,

wherein:

(A-1) one source/drain region of the first transistor is formed of a portion of a surface region of the second region,

(A-2) the other source/drain region of the first transistor is formed of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a portion of a surface region of the first region which portion is interposed between said portion of the surface region of the second region and the fourth region,

(A-4) the gate of the first transistor is formed on the channel forming region of the first

- 388 -

transistor through an insulation layer,

(B-1) one source/drain region of the second transistor is formed of other portion of the surface region of the first region,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of other portion of the surface region of the second region which other portion is interposed between said other portion of the surface region of the first region and the third region,

(B-4) the gate of the second transistor is formed on the channel forming region of the second transistor through an insulation layer,

(C-1) the gate regions of the junction-field-effect transistor are formed of the fifth region and part of the first region which part is opposed to the fifth region,

(C-2) the channel region of the junction-field-effect transistor is formed of part of the second region which part is interposed between the fifth region and said part of the first region,

(C-3) one source/drain region of the junction-field-effect transistor is formed of said portion of the surface region of the second region which portion extends from one end of the channel region of the junction-field-effect transistor and constitutes one source/drain region of the first transistor,

(C-4) the other source/drain region of the junction-field-effect transistor is formed of a portion of the second region which portion extends from the other end of the channel region of the junction-field-effect transistor,

(D-1) one end of the MIS type diode is formed of the fifth region,

(D-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to the

- 389 -

fifth region constituting one end of the MIS type diode, through a wide gap thin film,

(E) the gate of the first transistor and the gate of the second transistor are connected to a first line for memory cell selection,

(F) the third region is connected to a write-in information setting line,

(G) the fourth region is connected to a second line,

(H) the fifth region is connected to the first region, and

(I) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential.

109. The semi-conductor memory cell according to claim 108, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

110. The semi-conductor memory cell according to claim 109, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

111. The semi-conductor memory cell according to claim 108, wherein the second region and the third region constitute a diode, and the second region is connected to the write-in information setting line through the third region.

112. The semi-conductor memory cell according to claim 108, wherein further provided is a diode-constituting-region which is formed in a surface region of the second region and is in contact with the second region so as to form a rectifier junction together with the second region,

- 390 -

a majority carrier diode comprises the diode-constituting-region and the second region, and the second region is connected to the write-in information setting line through the diode-constituting region.

113. The semi-conductor memory cell according to claim 108, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the fifth region and the potential in the other end of the MIS type diode.

114. The semiconductor memory cell according to claim 113, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the fifth region depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other

- 391 -

end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

115. A semiconductor memory cell;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(4) an MIS type diode for retaining information,

the semiconductor memory cell having;

(a) a semi-conductive first region having a first conductivity type,

(b) a semi-conductive second region which is in contact with the first region and has a second conductivity type,

(c) a third region which is formed in a surface region of the first region and is in contact with the first region so as to form a rectifier junction together with the first region,

(d) a fourth region which is formed in a surface region of the second region and is in contact with the second region so as to form a rectifier junction together with the second region, and

(e) the gate which is formed, through an

- 392 -

insulation layer, so as to bridge the first region and the fourth region and so as to bridge the second region and the third region and is shared by the first transistor and the second transistor,

wherein:

(A-1) one source/drain region of the first transistor is formed of a surface region of the first region,

(A-2) the other source/drain region of the first transistor is formed of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a surface region of the second region which surface region is interposed between the surface region of the first region and the fourth region,

(B-1) one source/drain region of the second transistor is formed of the surface region of the second region which surface region constitutes the channel forming region of the first transistor,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of the surface region of the first region which surface region constitutes one source/drain region of the first transistor,

(C-1) the gate regions of the junction-field-effect transistor are formed of the third region and part of the second region which part is opposed to the third region,

(C-2) the channel region of the junction-field-effect transistor is formed of part of the first region which part is interposed between the third region and said part of the second region,

(C-3) one source/drain region of the junction-field-effect transistor is formed of the surface region of the first region which surface region extends from one end of the channel region of the

- 393 -

junction-field-effect transistor and constitutes one source/drain region of the first transistor,

(C-4) the other source/drain region of the junction-field-effect transistor is formed of a portion of the first region which portion extends from the other end of the channel region of the junction-field-effect transistor,

(D-1) one end of the MIS type diode is formed of part of the second region or an extending portion of the second region,

(D-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to said part of the second region or said extending portion of the second region which constitutes one end of the MIS type diode, through a wide gap thin film,

(E) the gate is connected to a first line for memory cell selection,

(F) the third region is connected to a write-in information setting line,

(G) the fourth region is connected to a second line, and

(H) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential.

116. The semi-conductor memory cell according to claim 115, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

117. The semi-conductor memory cell according to claim 116, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

118. The semi-conductor memory cell according to claim 115, wherein the first region and the third region

- 394 -

constitute a diode, and the first region is connected to the write-in information setting line through the third region.

119. The semi-conductor memory cell according to claim 115, wherein further provided is a diode-constituting region which is formed in a surface region of the first region and is in contact with the first region so as to form a rectifier junction together with the first region,

a majority carrier diode comprises the diode-constituting region and the first region, and

the first region is connected to the write-in information setting line through the diode-constituting region.

120. The semi-conductor memory cell according to claim 115, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in said part of the second region or the extending region of the second region constituting one end of the MIS type diode and the potential in the other end of the MIS type diode.

121. The semiconductor memory cell according to claim 120, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first

- 395 -

potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in said part of the second region or the extending portion of the second region constituting one end of the MIS type diode depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

122. A semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(4) an MIS type diode for retaining information,

the semiconductor memory cell having;

- 396 -

(a) a semi-conductive first region having a second conductivity type,

(b) a semi-conductive second region which is formed in a surface region of the first region and has a first conductivity type,

(c) a third region which is formed in a surface region of the second region and is in contact with the second region so as to form a rectifier junction together with the second region,

(d) a semi-conductive fourth region which is formed in a surface region of the first region to be spaced from the second region and has the first conductivity type, and

(e) a fifth region which is formed in a surface region of the fourth region and is in contact with the fourth region so as to form a rectifier junction together with the fourth region,

wherein:

(A-1) one source/drain region of the first transistor is formed of a portion of a surface region of the second region,

(A-2) the other source/drain region of the first transistor is formed of a surface region of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a portion of a surface region of the first region which portion is interposed between said portion of the surface region of the second region and the surface region of the fourth region,

(A-4) the gate of the first transistor is formed on the channel forming region of the first transistor through an insulation layer,

(B-1) one source/drain region of the second transistor is formed of other portion of the surface region of the first region,

(B-2) the other source/drain region of the second transistor is formed of the third region,

- 397 -

(B-3) the channel forming region of the second transistor is formed of other portion of the surface region of the second region which other portion is interposed between said other portion of the surface region of the first region and the third region,

(B-4) the gate of the second transistor is formed on the channel forming region of the second transistor through an insulation layer,

(C-1) the gate regions of the junction-field-effect transistor are formed of the fifth region and part of the first region which part is opposed to the fifth region,

(C-2) the channel region of the junction-field-effect transistor is formed of part of the fourth region which part is interposed between the fifth region and said part of the first region,

(C-3) one source/drain region of the junction-field-effect transistor is formed of the surface region of the fourth region which surface region extends from one end of the channel region of the junction-field-effect transistor and constitutes the other source/drain region of the first transistor,

(C-4) the other source/drain region of the junction-field-effect transistor is formed of a portion of the fourth region which portion extends from the other end of the channel region of the junction-field-effect transistor,

(D-1) one end of the MIS type diode is formed of part of the first region,

(D-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to said part of the first region which part constitutes one end of the MIS type diode, through a wide gap thin film,

(E) the gate of the first transistor and the gate of the second transistor are connected to a first line for memory cell selection,

(F) the third region is connected to a

- 398 -

write-in information setting line,

(G) said portion of the fourth region which portion constitutes the other source/drain region of the junction-field-effect transistor is connected to a second line,

(H) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential, and

(I) the fifth region is connected to a fourth line.

123. The semi-conductor memory cell according to claim 122, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

124. The semi-conductor memory cell according to claim 123, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

125. The semi-conductor memory cell according to claim 122, wherein the second region and the third region constitute a diode, and the second region is connected to the write-in information setting line through the third region.

126. The semi-conductor memory cell according to claim 122, wherein further provided is a diode-constituting-region which is formed in a surface region of the second region and is in contact with the second region so as to form a rectifier junction together with the second region,

a majority carrier diode comprises the diode-constituting-region and the second region, and

the second region is connected to the write-in information setting line through the diode-

- 399 -

constituting region.

127. The semi-conductor memory cell according to claim 122, wherein the fifth region is connected to the write-in information setting line in place of being connected to the fourth line.

128. The semi-conductor memory cell according to claim 127, wherein the second region and the third region constitute a diode, and the second region is connected to the write-in information setting line through the third region.

129. The semi-conductor memory cell according to claim 127, wherein further provided is a diode-constituting-region which is formed in a surface region of the second region and is in contact with the second region so as to form a rectifier junction together with the second region,

a majority carrier diode comprises the diode-constituting-region and the second region, and

the second region is connected to the write-in information setting line through the diode-constituting region.

130. The semi-conductor memory cell according to claim 122, wherein the fifth region is connected to the write-in information setting line in place of being connected to the fourth line.

131. The semi-conductor memory cell according to claim 130, wherein the second region and the third region constitute a diode, and the second region is connected to the write-in information setting line through the third region.

132. The semi-conductor memory cell according to

- 400 -

claim 130, wherein further provided is a diode-constituting-region which is formed in a surface region of the second region and is in contact with the second region so as to form a rectifier junction together with the second region,

a majority carrier diode comprises the diode-constituting-region and the second region, and

the second region is connected to the write-in information setting line through the diode-constituting region.

133. The semi-conductor memory cell according to claim 122, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the first region and the potential in the other end of the MIS type diode.

134. The semiconductor memory cell according to claim 133, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in said portion of the first region constituting one end of the MIS type diode depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region

- 401 -

of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

135. A semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(4) an MIS type diode for retaining information,

the semiconductor memory cell having;

(a) a semi-conductive first region having a second conductivity type,

(b) a semi-conductive second region which is formed in a surface region of the first region and has a first conductivity type,

(c) a third region which is formed in a surface region of the second region and is in contact with the second region so as to form a rectifier

- 402 -

junction together with the second region,

(d) a semi-conductive fourth region which is formed in a surface region of the first region to be spaced from the second region and has the first conductivity type, and

(e) a semi-conductive fifth region which is formed in a surface region of the fourth region and has the second conductivity type,

wherein:

(A-1) one source/drain region of the first transistor is formed of a portion of a surface region of the second region,

(A-2) the other source/drain region of the first transistor is formed of a surface region of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a portion of a surface region of the first region which portion is interposed between said portion of the surface region of the second region and the surface region of the fourth region,

(A-4) the gate of the first transistor is formed on the channel forming region of the first transistor through an insulation layer,

(B-1) one source/drain region of the second transistor is formed of other portion of the surface region of the first region,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of other portion of the surface region of the second region which other portion is interposed between said other portion of the surface region of the first region and the third region,

(B-4) the gate of the second transistor is formed on the channel forming region of the second transistor through an insulation layer,

(C-1) the gate regions of the junction-

- 403 -

field-effect transistor are formed of the fifth region and part of the first region which part is opposed to the fifth region,

(C-2) the channel region of the junction-field-effect transistor is formed of part of the fourth region which part is interposed between the fifth region and said part of the first region,

(C-3) one source/drain region of the junction-field-effect transistor is formed of the surface region of the fourth region which surface region extends from one end of the channel region of the junction-field-effect transistor and constitutes the other source/drain region of the first transistor,

(C-4) the other source/drain region of the junction-field-effect transistor is formed of a portion of the fourth region which portion extends from the other end of the channel region of the junction-field-effect transistor,

(D-1) one end of the MIS type diode is formed of the fifth region,

(D-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to the fifth region constituting one end of the MIS type diode, through a wide gap thin film,

(E) the gate of the first transistor and the gate of the second transistor are connected to a first line for memory cell selection,

(F) the third region is connected to a write-in information setting line,

(G) said portion of the fourth region which portion constitutes the other source/drain region of the junction-field-effect transistor is connected to a second line,

(H) the fifth region is connected to the first region, and

(I) the electrode constituting the other end of the MIS type diode is connected to a third line

- 404 -

having a predetermined potential.

136. The semi-conductor memory cell according to claim 135, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

137. The semi-conductor memory cell according to claim 136, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

138. The semi-conductor memory cell according to claim 135, wherein the second region and the third region constitute a diode, and the second region is connected to the write-in information setting line through the third region.

139. The semi-conductor memory cell according to claim 135, wherein further provided is a diode-constituting-region which is formed in a surface region of the second region and is in contact with the second region so as to form a rectifier junction together with the second region,

a majority carrier diode comprises the diode-constituting-region and the second region, and the second region is connected to the write-in information setting line through the diode-constituting region.

140. The semi-conductor memory cell according to claim 135, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the fifth region and the potential in the other end of the MIS type diode.

- 405 -

141. The semi-conductor memory cell according to claim 140, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the fifth region depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

142. A semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having

- 406 -

source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(4) an MIS type diode for retaining information,

the semiconductor memory cell having;

(a) a semi-conductive first region having a first conductivity type,

(b) a semi-conductive second region which is in contact with the first region and has a second conductivity type,

(c) a third region which is formed in a surface region of the first region and is in contact with the first region so as to form a rectifier junction together with the first region,

(d) a semi-conductive fourth region which is formed in a surface region of the second region and has the first conductivity type,

(e) a fifth region which is formed in a surface region of the fourth region and is in contact with the fourth region so as to form a rectifier junction together with the fourth region, and

(f) the gate which is formed, through an insulation layer, so as to bridge the first region and the fourth region and so as to bridge the second region and the third region and is shared by the first transistor and the second transistor,

wherein:

(A-1) one source/drain region of the first transistor is formed of a surface region of the first region,

(A-2) the other source/drain region of the first transistor is formed of a surface region of the

- 407 -

fourth region,

(A-3) the channel forming region of the first transistor is formed of a surface region of the second region which surface region is interposed between the surface region of the first region and the surface region of the fourth region,

(B-1) one source/drain region of the second transistor is formed of the surface region of the second region which surface region constitutes the channel forming region of the first transistor,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of the surface region of the first region which surface region constitutes one source/drain region of the first transistor,

(C-1) the gate regions of the junction-field-effect transistor are formed of the fifth region and part of the second region which part is opposed to the fifth region,

(C-2) the channel region of the junction-field-effect transistor is formed of part of the fourth region which part is interposed between the fifth region and said part of the second region,

(C-3) one source/drain region of the junction-field-effect transistor is formed of the surface region of the fourth region which surface region extends from one end of the channel region of the junction-field-effect transistor and constitutes the other source/drain region of the first transistor,

(C-4) the other source/drain region of the junction-field-effect transistor is formed of a portion of the fourth region which portion extends from the other end of the channel region of the junction-field-effect transistor,

(D-1) one end of the MIS type diode is formed of part of the second region,

- 408 -

(D-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to said part of the second region which part constitutes one end of the MIS type diode, through a wide gap thin film,

(E) the gate is connected to a first line for memory cell selection,

(F) the third region is connected to a write-in information setting line,

(G) said portion of the fourth region which portion constitutes the other source/drain region of the junction-field-effect transistor is connected to a second line,

(H) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential, and

(I) the fifth region is connected to a fourth line.

143. The semi-conductor memory cell according to claim 142, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

144. The semi-conductor memory cell according to claim 143, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

145. The semi-conductor memory cell according to claim 142, wherein the first region and the third region constitute a diode, and the first region is connected to the write-in information setting line through the third region.

146. The semi-conductor memory cell according to claim 142, wherein further provided is a diode-

- 409 -

constituting region which is formed in a surface region of the first region and is in contact with the first region so as to form a rectifier junction together with the first region,

a majority carrier diode comprises the diode-constituting region and the first region, and

the first region is connected to the write-in information setting line through the diode-constituting region.

147. The semi-conductor memory cell according to claim 142, wherein the fifth region is connected to the write-in information setting line in place of being connected to the fourth line.

148. The semi-conductor memory cell according to claim 147, wherein the first region and the third region constitute a diode, and the first region is connected to the write-in information setting line through the third region.

149. The semi-conductor memory cell according to claim 147, wherein further provided is a diode-constituting region which is formed in a surface region of the first region and is in contact with the first region so as to form a rectifier junction together with the first region,

a majority carrier diode comprises the diode-constituting region and the first region, and

the first region is connected to the write-in information setting line through the diode-constituting region.

150. The semi-conductor memory cell according to claim 142, wherein the fifth region is connected to the second region in place of being connected to the fourth line.

- 410 -

151. The semi-conductor memory cell according to claim 150, wherein the first region and the third region constitute a diode, and the first region is connected to the write-in information setting line through the third region.

152. The semi-conductor memory cell according to claim 150, wherein further provided is a diode-constituting region which is formed in a surface region of the first region and is in contact with the first region so as to form a rectifier junction together with the first region,

a majority carrier diode comprises the diode-constituting region and the first region, and

the first region is connected to the write-in information setting line through the diode-constituting region.

153. The semi-conductor memory cell according to claim 142, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the second region and the potential in the other end of the MIS type diode.

154. The semiconductor memory cell according to claim 153, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel

- 411 -

forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in said part of the second region constituting one end of the MIS type diode depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

155. A semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(4) an MIS type diode for retaining information,

the semiconductor memory cell having;

- 412 -

(a) a semi-conductive first region having a first conductivity type,

(b) a semi-conductive second region which is in contact with the first region and has a second conductivity type,

(c) a third region which is formed in a surface region of the first region and is in contact with the first region so as to form a rectifier junction together with the first region,

(d) a semi-conductive fourth region which is formed in a surface region of the second region and has the first conductivity type,

(e) a semi-conductive fifth region which is formed in a surface region of the fourth region and has the second conductivity type, and

(f) the gate which is formed, through an insulation layer, so as to bridge the first region and the fourth region and so as to bridge the second region and the third region and is shared by the first transistor and the second transistor,

wherein:

(A-1) one source/drain region of the first transistor is formed of a surface region of the first region,

(A-2) the other source/drain region of the first transistor is formed of a surface region of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a surface region of the second region which surface region is interposed between the surface region of the first region and the surface region of the fourth region,

(B-1) one source/drain region of the second transistor is formed of the surface region of the second region which surface region constitutes the channel forming region of the first transistor,

(B-2) the other source/drain region of the

- 413 -

second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of the surface region of the first region which surface region constitutes one source/drain region of the first transistor,

(C-1) the gate regions of the junction-field-effect transistor are formed of the fifth region and part of the second region which part is opposed to the fifth region,

(C-2) the channel region of the junction-field-effect transistor is formed of part of the fourth region which part is interposed between the fifth region and said part of the second region,

(C-3) one source/drain region of the junction-field-effect transistor is formed of the surface region of the fourth region which surface region extends from one end of the channel region of the junction-field-effect transistor and constitutes the other source/drain region of the first transistor,

(C-4) the other source/drain region of the junction-field-effect transistor is formed of a portion of the fourth region which portion extends from the other end of the channel region of the junction-field-effect transistor,

(D-1) one end of the MIS type diode is formed of the fifth region,

(D-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to the fifth region which constitutes one end of the MIS type diode, through a wide gap thin film,

(E) the gate is connected to a first line for memory cell selection,

(F) the third region is connected to a write-in information setting line,

(G) said portion of the fourth region which portion constitutes the other source/drain region of the junction-field-effect transistor is connected to a

- 414 -

second line,

(H) the fifth region is connected to the second region, and

(I) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential.

156. The semi-conductor memory cell according to claim 155, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

157. The semi-conductor memory cell according to claim 156, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

158. The semi-conductor memory cell according to claim 155, wherein the first region and the third region constitute a diode, and the first region is connected to the write-in information setting line through the third region.

159. The semi-conductor memory cell according to claim 155, wherein further provided is a diode-constituting region which is formed in a surface region of the first region and is in contact with the first region so as to form a rectifier junction together with the first region,

a majority carrier diode comprises the diode-constituting region and the first region, and

the first region is connected to the write-in information setting line through the diode-constituting region.

160. The semi-conductor memory cell according to claim 155, wherein the wide gap thin film is composed of

- 415 -

a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the fifth region and the potential in the other end of the MIS type diode.

161. The semi-conductor memory cell according to claim 160, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the fifth region depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

162. A semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in

- 416 -

contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a third transistor for current control, having the second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(4) a junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(5) an MIS type diode for retaining information,

the semiconductor memory cell having;

(a) a semi-conductive first region having a first conductivity type,

(b) a semi-conductive second region which is in contact with the first region and has a second conductivity type,

(c) a third region which is formed in a surface region of the first region and is in contact with the first region so as to form a rectifier junction together with the first region,

(d) a semi-conductive fourth region which is formed in a surface region of the second region and has the first conductivity type,

(e) a fifth region which is formed in a surface region of the fourth region and is in contact with the fourth region so as to form a rectifier junction together with the fourth region, and

- 417 -

(f) the gate which is formed, through an insulation layer, so as to bridge the first region and the fourth region, so as to bridge the second region and the third region and so as to bridge the second region and the fifth region and is shared by the first transistor, the second transistor and the third transistor,

wherein:

(A-1) one source/drain region of the first transistor is formed of a surface region of the first region,

(A-2) the other source/drain region of the first transistor is formed of a surface region of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a surface region of the second region which surface region is interposed between the surface region of the first region and the surface region of the fourth region,

(B-1) one source/drain region of the second transistor is formed of the surface region of the second region,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of the surface region of the first region,

(C-1) one source/drain region of the third transistor is formed of the surface region of the second region,

(C-2) the other source/drain region of the third transistor is formed of the fifth region,

(C-3) the channel forming region of the third transistor is formed of the surface region of the fourth region,

(D-1) the gate regions of the junction-field-effect transistor are formed of the fifth region

- 418 -

and part of the second region which part is opposed to the fifth region,

(D-2) the channel region of the junction-field-effect transistor is formed of part of the fourth region which part is interposed between the fifth region and said part of the second region,

(D-3) one source/drain region of the junction-field-effect transistor is formed of the surface region of the fourth region which surface region extends from one end of the channel region of the junction-field-effect transistor and constitutes the other source/drain region of the first transistor and the channel forming region of the third transistor,

(D-4) the other source/drain region of the junction-field-effect transistor is formed of a portion of the fourth region which portion extends from the other end of the channel region of the junction-field-effect transistor,

(E-1) one end of the MIS type diode is formed of part of the second region,

(E-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to said part of the second region which part constitutes one end of the MIS type diode, through a wide gap thin film,

(F) the gate is connected to a first line for memory cell selection,

(G) the third region is connected to a write-in information setting line,

(H) said portion of the fourth region which portion constitutes the other source/drain region of the junction-field-effect transistor is connected to a second line, and

(I) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential.

- 419 -

163. The semi-conductor memory cell according to claim 162, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

164. The semi-conductor memory cell according to claim 163, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

165. The semi-conductor memory cell according to claim 162, wherein the first region and the third region constitute a diode, and the first region is connected to the write-in information setting line through the third region.

166. The semi-conductor memory cell according to claim 162, wherein further provided is a diode-constituting region which is formed in a surface region of the first region and is in contact with the first region so as to form a rectifier junction together with the first region,

a majority carrier diode comprises the diode-constituting region and the first region, and the first region is connected to the write-in information setting line through the diode-constituting region.

167. The semi-conductor memory cell according to claim 162, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the second region and the potential in the other end of the MIS type diode.

168. The semi-conductor memory cell according to claim 167, wherein binary information of first

- 420 -

information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in said part of the second region constituting one end of the MIS type diode depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

169. A semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming

- 421 -

region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a third transistor for current control, having the second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(4) a junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(5) an MIS type diode for retaining information,

the semiconductor memory cell having;

(a) a semi-conductive first region having a first conductivity type,

(b) a semi-conductive second region which is in contact with the first region and has a second conductivity type,

(c) a third region which is formed in a surface region of the first region and is in contact with the first region so as to form a rectifier junction together with the first region,

(d) a semi-conductive fourth region which is formed in a surface region of the second region and has the first conductivity type,

(e) a semi-conductive fifth region which is formed in a surface region of the fourth region and has the second conductivity type, and

(f) the gate which is formed, through an insulation layer, so as to bridge the first region and the fourth region, so as to bridge the second region and the third region and so as to bridge the second region and the fifth region and is shared by the first transistor, the second transistor and the third transistor,

- 422 -

wherein:

(A-1) one source/drain region of the first transistor is formed of a surface region of the first region,

(A-2) the other source/drain region of the first transistor is formed of a surface region of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a surface region of the second region which surface region is interposed between the surface region of the first region and the surface region of the fourth region,

(B-1) one source/drain region of the second transistor is formed of the surface region of the second region,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of the surface region of the first region,

(C-1) one source/drain region of the third transistor is formed of the surface region of the second region,

(C-2) the other source/drain region of the third transistor is formed of the fifth region,

(C-3) the channel forming region of the third transistor is formed of the surface region of the fourth region,

(D-1) the gate regions of the junction-field-effect transistor are formed of the fifth region and part of the second region which part is opposed to the fifth region,

(D-2) the channel region of the junction-field-effect transistor is formed of part of the fourth region which part is interposed between the fifth region and said part of the second region,

(D-3) one source/drain region of the

- 423 -

junction-field-effect transistor is formed of the surface region of the fourth region which surface region extends from one end of the channel region of the junction-field-effect transistor and constitutes the other source/drain region of the first transistor and the channel forming region of the third transistor,

(D-4) the other source/drain region of the junction-field-effect transistor is formed of a portion of the fourth region which portion extends from the other end of the channel region of the junction-field-effect transistor,

(E-1) one end of the MIS type diode is formed of the fifth region,

(E-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to the fifth region which constitutes one end of the MIS type diode, through a wide gap thin film,

(F) the gate is connected to a first line for memory cell selection,

(G) the third region is connected to a write-in information setting line,

(H) said portion of the fourth region which portion constitutes the other source/drain region of the junction-field-effect transistor is connected to a second line, and

(I) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential.

170. The semi-conductor memory cell according to claim 169, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

171. The semi-conductor memory cell according to claim 170, wherein the electrode and the high-resistance element are integrally formed and are composed of a

- 424 -

silicon thin layer.

172. The semi-conductor memory cell according to claim 169, wherein a high-concentration-impurity-containing layer having the second conductivity type is formed in the surface region of the fourth region which surface region constitutes the channel forming region of the third transistor.

173. The semi-conductor memory cell according to claim 169, wherein the first region and the third region constitute a diode, and the first region is connected to the write-in information setting line through the third region.

174. The semi-conductor memory cell according to claim 169, wherein further provided is a diode-constituting region which is formed in a surface region of the first region and is in contact with the first region so as to form a rectifier junction together with the first region,

a majority carrier diode comprises the diode-constituting region and the first region, and the first region is connected to the write-in information setting line through the diode-constituting region.

175. The semi-conductor memory cell according to claim 169, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the fifth region and the potential in the other end of the MIS type diode.

176. The semi-conductor memory cell according to claim 175, wherein binary information of first information or second information is stored in the

- 425 -

semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the fifth region depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

177. A semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate

- 426 -

capacitively coupled with the channel forming region,

(3) a first junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions,

(4) a second junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(5) an MIS type diode for retaining information,

the semiconductor memory cell having;

(a) a semi-conductive first region having a first conductivity type,

(b) a semi-conductive second region which is in contact with the first region and has a second conductivity type,

(c) a third region which is formed in a surface region of the first region and is in contact with the first region so as to form a rectifier junction together with the first region,

(d) a semi-conductive fourth region which is formed in a surface region of the second region and has the first conductivity type,

(e) a fifth region which is formed in a surface region of the fourth region and is in contact with the fourth region so as to form a rectifier junction together with the fourth region, and

(f) the gate which is formed, through an insulation layer, so as to bridge the first region and the fourth region and so as to bridge the second region and the third region and is shared by the first transistor and the second transistor,

wherein:

(A-1) one source/drain region of the first transistor is formed of a surface region of the first region,

(A-2) the other source/drain region of the first transistor is formed of a surface region of the

- 427 -

fourth region,

(A-3) the channel forming region of the first transistor is formed of a surface region of the second region which surface region is interposed between the surface region of the first region and the surface region of the fourth region,

(B-1) one source/drain region of the second transistor is formed of the surface region of the second region,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of the surface region of the first region,

(C-1) the gate regions of the first junction-field-effect transistor are formed of the third region and part of the second region which part is opposed to the third region,

(C-2) the channel region of the first junction-field-effect transistor is formed of part of the first region which part is interposed between the third region and said part of the second region,

(C-3) one source/drain region of the first junction-field-effect transistor is formed of the surface region of the first region which surface region extends from one end of the channel region of the first junction-field-effect transistor and constitutes one source/drain region of the first transistor,

(C-4) the other source/drain region of the first junction-field-effect transistor is formed of a portion of the first region which portion extends from the other end of the channel region of the first junction-field-effect transistor,

(D-1) the gate regions of the second junction-field-effect transistor are formed of the fifth region and part of the second region which part is opposed to the fifth region,

- 428 -

(D-2) the channel region of the second junction-field-effect transistor is formed of part of the fourth region which part is interposed between the fifth region and said part of the second region,

(D-3) one source/drain region of the second junction-field-effect transistor is formed of the surface region of the fourth region which surface region extends from one end of the channel region of the second junction-field-effect transistor and constitutes the other source/drain region of the first transistor,

(D-4) the other source/drain region of the second junction-field-effect transistor is formed of a portion of the fourth region which portion extends from the other end of the channel region of the second junction-field-effect transistor,

(E-1) one end of the MIS type diode is formed of part of the second region,

(E-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to said part of the second region which part constitutes one end of the MIS type diode, through a wide gap thin film,

(F) the gate is connected to a first line for memory cell selection,

(G) the third region is connected to a write-in information setting line,

(H) said portion of the fourth region constituting the other source/drain region of the second junction-field-effect transistor is connected to a second line,

(I) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential, and

(J) the fifth region is connected to a fourth line.

178. The semi-conductor memory cell according to

- 429 -

claim 177, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

179. The semi-conductor memory cell according to claim 178, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

180. The semi-conductor memory cell according to claim 177, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the second region and the potential in the other end of the MIS type diode.

181. The semi-conductor memory cell according to claim 180, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in said part of the second region constituting one end of the MIS type diode depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

- 430 -

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

182. A semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a first junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions,

(4) a second junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(5) an MIS type diode for retaining information,

the semiconductor memory cell having;

(a) a semi-conductive first region having a first conductivity type,

(b) a semi-conductive second region which is in contact with the first region and has a second conductivity type,

(c) a third region which is formed in a surface region of the first region and is in contact

- 431 -

with the first region so as to form a rectifier junction together with the first region,

(d) a semi-conductive fourth region which is formed in a surface region of the second region and has the first conductivity type,

(e) a semi-conductive fifth region which is formed in a surface region of the fourth region and has the second conductivity type, and

(f) the gate which is formed, through an insulation layer, so as to bridge the first region and the fourth region and so as to bridge the second region and the third region and is shared by the first transistor and the second transistor,

wherein:

(A-1) one source/drain region of the first transistor is formed of a surface region of the first region,

(A-2) the other source/drain region of the first transistor is formed of a surface region of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a surface region of the second region which surface region is interposed between the surface region of the first region and the surface region of the fourth region,

(B-1) one source/drain region of the second transistor is formed of the surface region of the second region,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of the surface region of the first region,

(C-1) the gate regions of the first junction-field-effect transistor are formed of the third region and part of the second region which part is opposed to the third region,

- 432 -

(C-2) the channel region of the first junction-field-effect transistor is formed of part of the first region which part is interposed between the third region and said part of the second region,

(C-3) one source/drain region of the first junction-field-effect transistor is formed of the surface region of the first region which surface region extends from one end of the channel region of the first junction-field-effect transistor and constitutes one source/drain region of the first transistor,

(C-4) the other source/drain region of the first junction-field-effect transistor is formed of a portion of the first region which portion extends from the other end of the channel region of the first junction-field-effect transistor,

(D-1) the gate regions of the second junction-field-effect transistor are formed of the fifth region and part of the second region which part is opposed to the fifth region,

(D-2) the channel region of the second junction-field-effect transistor is formed of part of the fourth region which part is interposed between the fifth region and said part of the second region,

(D-3) one source/drain region of the second junction-field-effect transistor is formed of the surface region of the fourth region which surface region extends from one end of the channel region of the second junction-field-effect transistor and constitutes the other source/drain region of the first transistor,

(D-4) the other source/drain region of the second junction-field-effect transistor is formed of a portion of the fourth region which portion extends from the other end of the channel region of the second junction-field-effect transistor,

(E-1) one end of the MIS type diode is formed of the fifth region,

(E-2) an electrode constituting the other

- 433 -

end of the MIS type diode is formed to be opposed to the fifth region which constitutes one end of the MIS type diode, through a wide gap thin film,

(F) the gate is connected to a first line for memory cell selection,

(G) the third region is connected to a write-in information setting line,

(H) said portion of the fourth region constituting the other source/drain region of the second junction-field-effect transistor is connected to a second line,

(I) the fifth region is connected to the second region, and

(J) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential.

183. The semi-conductor memory cell according to claim 182, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

184. The semi-conductor memory cell according to claim 183, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

185. The semi-conductor memory cell according to claim 182, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the fifth region and the potential in the other end of the MIS type diode.

186. The semi-conductor memory cell according to claim 185, wherein binary information of first information or second information is stored in the

- 434 -

semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the fifth region depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

187. A semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate

- 435 -

capacitively coupled with the channel forming region,

(3) a third transistor for current control, having the second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(4) a first junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions,

(5) a second junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(6) an MIS type diode for retaining information,

the semiconductor memory cell having;

(a) a semi-conductive first region having a first conductivity type,

(b) a semi-conductive second region which is in contact with the first region and has a second conductivity type,

(c) a third region which is formed in a surface region of the first region and is in contact with the first region so as to form a rectifier junction together with the first region,

(d) a semi-conductive fourth region which is formed in a surface region of the second region and has the first conductivity type,

(e) a fifth region which is formed in a surface region of the fourth region and is in contact with the fourth region so as to form a rectifier junction together with the fourth region, and

(f) the gate which is formed, through an insulation layer, so as to bridge the first region and the fourth region, so as to bridge the second region and the third region and so as to bridge the second region and the fifth region and is shared by the first

- 436 -

transistor, the second transistor and the third transistor,

wherein:

(A-1) one source/drain region of the first transistor is formed of a surface region of the first region,

(A-2) the other source/drain region of the first transistor is formed of a surface region of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a surface region of the second region which surface region is interposed between the surface region of the first region and the surface region of the fourth region,

(B-1) one source/drain region of the second transistor is formed of the surface region of the second region,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of the surface region of the first region,

(C-1) one source/drain region of the third transistor is formed of the surface region of the second region,

(C-2) the other source/drain region of the third transistor is formed of the fifth region,

(C-3) the channel forming region of the third transistor is formed of the surface region of the fourth region,

(D-1) the gate regions of the first junction-field-effect transistor are formed of the third region and part of the second region which part is opposed to the third region,

(D-2) the channel region of the first junction-field-effect transistor is formed of part of the first region which part is interposed between the

- 437 -

third region and said part of the second region,

(D-3) one source/drain region of the first junction-field-effect transistor is formed of the surface region of the first region which surface region extends from one end of the channel region of the first junction-field-effect transistor and constitutes one source/drain region of the first transistor,

(D-4) the other source/drain region of the first junction-field-effect transistor is formed of a portion of the first region which portion extends from the other end of the channel region of the first junction-field-effect transistor,

(E-1) the gate regions of the second junction-field-effect transistor are formed of the fifth region and part of the second region which part is opposed to the fifth region,

(E-2) the channel region of the second junction-field-effect transistor is formed of part of the fourth region which part is interposed between the fifth region and said part of the second region,

(E-3) one source/drain region of the second junction-field-effect transistor is formed of the surface region of the fourth region which surface region extends from one end of the channel region of the second junction-field-effect transistor and constitutes the other source/drain region of the first transistor and the channel forming region of the third transistor,

(E-4) the other source/drain region of the second junction-field-effect transistor is formed of a portion of the fourth region which portion extends from the other end of the channel region of the second junction-field-effect transistor,

(F-1) one end of the MIS type diode is formed of part of the second region,

(F-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to said part of the second region which part constitutes

- 438 -

one end of the MIS type diode, through a wide gap thin film,

(G) the gate is connected to a first line for memory cell selection,

(H) the third region is connected to a write-in information setting line,

(I) said portion of the fourth region constituting the other source/drain region of the second junction-field-effect transistor is connected to a second line, and

(J) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential.

188. The semi-conductor memory cell according to claim 187, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

189. The semi-conductor memory cell according to claim 188, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

190. The semi-conductor memory cell according to claim 187, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the second region and the potential in the other end of the MIS type diode.

191. The semi-conductor memory cell according to claim 190, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the

- 439 -

first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in said part of the second region constituting one end of the MIS type diode depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

192. A semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a third transistor for current control,

- 440 -

having the second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(4) a first junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions,

(5) a second junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(6) an MIS type diode for retaining information,

the semiconductor memory cell having;

(a) a semi-conductive first region having a first conductivity type,

(b) a semi-conductive second region which is in contact with the first region and has a second conductivity type,

(c) a third region which is formed in a surface region of the first region and is in contact with the first region so as to form a rectifier junction together with the first region,

(d) a semi-conductive fourth region which is formed in a surface region of the second region and has the first conductivity type,

(e) a semi-conductive fifth region which is formed in a surface region of the fourth region and has the second conductivity type, and

(f) the gate which is formed, through an insulation layer, so as to bridge the first region and the fourth region, so as to bridge the second region and the third region and so as to bridge the second region and the fifth region and is shared by the first transistor, the second transistor and the third transistor,

wherein:

- 441 -

(A-1) one source/drain region of the first transistor is formed of a surface region of the first region,

(A-2) the other source/drain region of the first transistor is formed of a surface region of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a surface region of the second region which surface region is interposed between the surface region of the first region and the surface region of the fourth region,

(B-1) one source/drain region of the second transistor is formed of the surface region of the second region,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of the surface region of the first region,

(C-1) one source/drain region of the third transistor is formed of the surface region of the second region,

(C-2) the other source/drain region of the third transistor is formed of the fifth region,

(C-3) the channel forming region of the third transistor is formed of the surface region of the fourth region,

(D-1) the gate regions of the first junction-field-effect transistor are formed of the third region and part of the second region which part is opposed to the third region,

(D-2) the channel region of the first junction-field-effect transistor is formed of part of the first region which part is interposed between the third region and said part of the second region,

(D-3) one source/drain region of the first junction-field-effect transistor is formed of the

- 442 -

surface region of the first region which surface region extends from one end of the channel region of the first junction-field-effect transistor and constitutes one source/drain region of the first transistor,

(D-4) the other source/drain region of the first junction-field-effect transistor is formed of a portion of the first region which portion extends from the other end of the channel region of the first junction-field-effect transistor,

(E-1) the gate regions of the second junction-field-effect transistor are formed of the fifth region and part of the second region which part is opposed to the fifth region,

(E-2) the channel region of the second junction-field-effect transistor is formed of part of the fourth region which part is interposed between the fifth region and said part of the second region,

(E-3) one source/drain region of the second junction-field-effect transistor is formed of the surface region of the fourth region which surface region extends from one end of the channel region of the second junction-field-effect transistor and constitutes the other source/drain region of the first transistor and the channel forming region of the third transistor,

(E-4) the other source/drain region of the second junction-field-effect transistor is formed of a portion of the fourth region which portion extends from the other end of the channel region of the second junction-field-effect transistor,

(F-1) one end of the MIS type diode is formed of the fifth region,

(F-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to the fifth region which constitutes one end of the MIS type diode, through a wide gap thin film,

(G) the gate is connected to a first line for memory cell selection,

- 443 -

(H) the third region is connected to a write-in information setting line,

(I) said portion of the fourth region constituting the other source/drain region of the second junction-field-effect transistor is connected to a second line,

(J) the fifth region is connected to the second region, and

(K) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential.

193. The semi-conductor memory cell according to claim 192, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

194. The semi-conductor memory cell according to claim 193, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

195. The semi-conductor memory cell according to claim 192, wherein a high-concentration-impurity-containing layer having the second conductivity type is formed in the surface region of the fourth region which surface region constitutes the channel forming region of the third transistor.

196. The semi-conductor memory cell according to claim 192, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the fifth region and the potential in the other end of the MIS type diode.

197. The semi-conductor memory cell according to

- 444 -

claim 196, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in the fifth region depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

198. A semiconductor memory cell having a semiconductor layer having two main surfaces opposed to each other, the main surfaces being a first main surface and a second main surface,

the semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled

- 445 -

with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(4) an MIS type diode for retaining information,

the semiconductor memory cell further having;

(a) a semi-conductive first region which is formed in the semiconductor layer to extend over from the first main surface to the second main surface and has a first conductivity type,

(b) a semi-conductive second region which is formed in the semiconductor layer to extend over from the first main surface to the second main surface, is in contact with the first region and has a second conductivity type,

(c) a third region which is formed in a surface region including the second main surface of the first region to be spaced from the second region and is in contact with the first region so as to form a rectifier junction together with the first region,

(d) a fourth region which is formed in a surface region including the first main surface of the second region to be spaced from the first region and is in contact with the second region so as to form a rectifier junction together with the second region,

(e) a fifth region which is formed in a surface region including the first main surface of the first region to be spaced from the second region and is in contact with the first region so as to form a

- 446 -

rectifier junction together with the first region,

(f) the gate of the first transistor formed on a first insulation layer formed on the first main surface so as to bridge the first region and the fourth region, and

(g) the gate of the second transistor formed on a second insulation layer formed on the second main surface so as to bridge the second region and the third region,

wherein:

(A-1) one source/drain region of the first transistor is formed of a surface region including the first main surface of the first region,

(A-2) the other source/drain region of the first transistor is formed of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a surface region including the first main surface of the second region which surface region is interposed between the surface region including the first main surface of the first region and the fourth region,

(B-1) one source/drain region of the second transistor is formed of a surface region including the second main surface of the second region,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of a surface region including the second main surface of the first region which surface region is interposed between the surface region including the second main surface of the second region and the third region,

(C-1) the gate regions of the junction-field-effect transistor are formed of the fifth region and the third region which is opposed to the fifth region,

(C-2) the channel region of the junction-

- 447 -

field-effect transistor is formed of part of the first region which part is interposed between the fifth region and the third region,

(C-3) one source/drain region of the junction-field-effect transistor is formed of a portion of the first region which portion extends from one end of the channel region of the junction-field-effect transistor and constitutes one source/drain region of the first transistor and the channel forming region of the second transistor,

(C-4) the other source/drain region of the junction-field-effect transistor is formed of a portion of the first region which portion extends from the other end of the channel region of the junction-field-effect transistor,

(D-1) one end of the MIS type diode is formed of part of the second region,

(D-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to said part of the second region constituting one end of the MIS type diode, through a wide gap thin film,

(E) the gate of the first transistor and the gate of the second transistor are connected to a first line for memory cell selection,

(F) the third region is connected to a write-in information setting line,

(G) the fourth region is connected to a second line,

(H) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential,

(I) the fifth region is connected to a fourth line, and

(J) said portion of the first region which portion constitutes the other source/drain region of the junction-field-effect transistor is connected to a fifth line.

- 448 -

199. The semi-conductor memory cell according to claim 198, wherein the fifth region is connected to the write-in information setting line in place of being connected to the fourth line.

200. The semi-conductor memory cell according to claim 198, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

201. The semi-conductor memory cell according to claim 200, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

202. The semi-conductor memory cell according to claim 198, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the first region and the potential in the other end of the MIS type diode.

203. The semiconductor memory cell according to claim 202, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode,

- 449 -

whereby carrier multiplication takes place, holes or electrons are stored in said portion of the first region constituting one end of the MIS type diode depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

204. A semiconductor memory cell having a semiconductor layer having two main surfaces opposed to each other, the main surfaces being a first main surface and a second main surface,

the semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(4) an MIS type diode for retaining information,

- 450 -

the semiconductor memory cell further having;

(a) a semi-conductive first region which is formed in the semiconductor layer to extend over from the first main surface to the second main surface and has a first conductivity type,

(b) a semi-conductive second region which is formed in the semiconductor layer to extend over from the first main surface to the second main surface, is in contact with the first region and has a second conductivity type,

(c) a third region which is formed in a surface region including the second main surface of the first region to be spaced from the second region and is in contact with the first region so as to form a rectifier junction together with the first region,

(d) a fourth region which is formed in a surface region including the first main surface of the second region to be spaced from the first region and is in contact with the second region so as to form a rectifier junction together with the second region,

(e) a fifth region which is formed in a surface region of the fourth region and is in contact with the fourth region so as to form a rectifier junction together with the fourth region,

(f) the gate of the first transistor formed on a first insulation layer formed on the first main surface so as to bridge the first region and the fourth region, and

(g) the gate of the second transistor formed on a second insulation layer formed on the second main surface so as to bridge the second region and the third region,

wherein:

(A-1) one source/drain region of the first transistor is formed of a surface region including the first main surface of the first region,

- 451 -

(A-2) the other source/drain region of the first transistor is formed of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a surface region including the first main surface of the second region which surface region is interposed between the surface region including the first main surface of the first region and the fourth region,

(B-1) one source/drain region of the second transistor is formed of a surface region including the second main surface of the second region,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of a surface region including the second main surface of the first region which surface region is interposed between the surface region including the second main surface of the second region and the third region,

(C-1) the gate regions of the junction-field-effect transistor are formed of the fifth region and part of the second region which part is opposed to the fifth region,

(C-2) the channel region of the junction-field-effect transistor is formed of part of the fourth region which part is interposed between the fifth region and said part of the second region,

(C-3) one source/drain region of the junction-field-effect transistor is formed of a portion of the fourth region which portion extends from one end of the channel region of the junction-field-effect transistor and constitutes the other source/drain region of the first transistor,

(C-4) the other source/drain region of the junction-field-effect transistor is formed of a portion of the fourth region which portion extends from the other end of the channel region of the junction-field-

- 452 -

effect transistor,

(D-1) one end of the MIS type diode is formed of part of the second region,

(D-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to said part of the second region constituting one end of the MIS type diode, through a wide gap thin film,

(E) the gate of the first transistor and the gate of the second transistor are connected to a first line for memory cell selection,

(F) said portion of the fourth region constituting the other source/drain region of the junction-field-effect transistor is connected to a second line,

(G) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential,

(H) the third region is connected to a write-in information setting line,

(I) the fifth region is connected to a fourth line, and

(J) the first region is connected to a fifth line.

205. The semi-conductor memory cell according to claim 204, wherein the fifth region is connected to the second region in place of being connected to the fourth line.

206. The semi-conductor memory cell according to claim 204, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

207. The semi-conductor memory cell according to claim 206, wherein the electrode and the high-resistance element are integrally formed and are composed of a

- 453 -

silicon thin layer.

208. The semi-conductor memory cell according to claim 204, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the first region and the potential in the other end of the MIS type diode.

209. The semiconductor memory cell according to claim 208, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in said portion of the first region constituting one end of the MIS type diode depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

- 454 -

210. A semiconductor memory cell having a semiconductor layer having two main surfaces opposed to each other, the main surfaces being a first main surface and a second main surface,

the semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a first junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions,

(4) a second junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(5) an MIS type diode for retaining information,

the semiconductor memory cell further having;

(a) a semi-conductive first region which is formed in the semiconductor layer to extend over from the first main surface to the second main surface and has a first conductivity type,

(b) a semi-conductive second region which is formed in the semiconductor layer to extend over from the first main surface to the second main surface, is in contact with the first region and has a second conductivity type,

- 455 -

(c) a third region which is formed in a surface region including the second main surface of the first region to be spaced from the second region and is in contact with the first region so as to form a rectifier junction together with the first region,

(d) a fourth region which is formed in a surface region including the first main surface of the second region to be spaced from the first region and is in contact with the second region so as to form a rectifier junction together with the second region,

(e) a fifth region which is formed in a surface region including the first main surface of the first region to be spaced from the second region and is in contact with the first region so as to form a rectifier junction together with the first region,

(f) a sixth region which is formed in a surface region of the fourth region and is in contact with the fourth region so as to form a rectifier junction together with the fourth region,

(g) the gate of the first transistor formed on a first insulation layer formed on the first main surface so as to bridge the first region and the fourth region, and

(h) the gate of the second transistor formed on a second insulation layer formed on the second main surface so as to bridge the second region and the third region,

wherein:

(A-1) one source/drain region of the first transistor is formed of a surface region including the first main surface of the first region,

(A-2) the other source/drain region of the first transistor is formed of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a surface region including the first main surface of the second region which surface region is interposed between the surface region

- 456 -

including the first main surface of the first region and the fourth region,

(B-1) one source/drain region of the second transistor is formed of a surface region including the second main surface of the second region,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of a surface region including the second main surface of the first region which surface region is interposed between the surface region including the second main surface of the second region and the third region,

(C-1) the gate regions of the first junction-field-effect transistor are formed of the fifth region and the third region which is opposed to the fifth region,

(C-2) the channel region of the first junction-field-effect transistor is formed of part of the first region which part is interposed between the fifth region and the third region,

(C-3) one source/drain region of the first junction-field-effect transistor is formed of a portion of the first region which portion extends from one end of the channel region of the first junction-field-effect transistor and constitutes one source/drain region of the first transistor and the channel forming region of the second transistor,

(C-4) the other source/drain region of the first junction-field-effect transistor is formed of a portion of the first region which portion extends from the other end of the channel region of the first junction-field-effect transistor,

(D-1) the gate regions of the second junction-field-effect transistor are formed of the sixth region and part of the second region which part is opposed to the sixth region,

- 457 -

(D-2) the channel region of the second junction-field-effect transistor is formed of part of the fourth region which part is interposed between the sixth region and said part of the second region,

(D-3) one source/drain region of the second junction-field-effect transistor is formed of a portion of the fourth region which portion extends from one end of the channel region of the second junction-field-effect transistor and constitutes the other source/drain region of the first transistor,

(D-4) the other source/drain region of the second junction-field-effect transistor is formed of a portion of the fourth region which portion extends from the other end of the channel region of the second junction-field-effect transistor,

(E-1) one end of the MIS type diode is formed of part of the second region,

(E-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to said part of the second region constituting one end of the MIS type diode, through a wide gap thin film,

(F) the gate of the first transistor and the gate of the second transistor are connected to a first line for memory cell selection,

(G) the third region is connected to a write-in information setting line,

(H) said portion of the fourth region constituting the other source/drain region of the second junction-field-effect transistor is connected to a second line,

(I) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential,

(J) the fifth region and the sixth region are connected to a fourth line, and

(K) said portion of the first region constituting the other source/drain region of the first

- 458 -

junction-field-effect transistor is connected to a fifth line.

211. The semi-conductor memory cell according to claim 210, wherein the fifth region is connected to the write-in information setting line in place of being connected to the fourth line, and

the sixth region is connected to the second region in place of being connected to the fourth line.

212. The semi-conductor memory cell according to claim 210, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

213. The semi-conductor memory cell according to claim 212, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

214. The semi-conductor memory cell according to claim 210, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the first region and the potential in the other end of the MIS type diode.

215. The semiconductor memory cell according to claim 214, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

- 459 -

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in said portion of the first region constituting one end of the MIS type diode depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

216. A semiconductor memory cell having a semiconductor layer having two main surfaces opposed to each other, the main surfaces being a first main surface and a second main surface,

the semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a third transistor for current control,

- 460 -

having the second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(4) a junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(5) an MIS type diode for retaining information,

the semiconductor memory cell further having;

(a) a semi-conductive first region which is formed in the semiconductor layer to extend over from the first main surface to the second main surface and has a first conductivity type,

(b) a semi-conductive second region which is formed in the semiconductor layer to extend over from the first main surface to the second main surface, is in contact with the first region and has a second conductivity type,

(c) a third region which is formed in a surface region including the second main surface of the first region to be spaced from the second region and is in contact with the first region so as to form a rectifier junction together with the first region,

(d) a fourth region which is formed in a surface region including the first main surface of the second region to be spaced from the first region and is in contact with the second region so as to form a rectifier junction together with the second region,

(e) a fifth region which is formed in a surface region of the fourth region and is in contact with the fourth region so as to form a rectifier junction together with the fourth region,

(f) the gate formed on a first insulation layer formed on the first main surface so as to bridge

- 461 -

the first region and the fourth region and so as to bridge the second region and the fifth region, and is shared by the first transistor and the third transistor, and

(g) the gate of the second transistor formed on a second insulation layer formed on the second main surface so as to bridge the second region and the third region,

wherein:

(A-1) one source/drain region of the first transistor is formed of a surface region including the first main surface of the first region,

(A-2) the other source/drain region of the first transistor is formed of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a surface region including the first main surface of the second region which surface region is interposed between the surface region including the first main surface of the first region and the fourth region,

(B-1) one source/drain region of the second transistor is formed of a surface region including the second main surface of the second region,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of a surface region including the second main surface of the first region which surface region is interposed between the surface region including the second main surface of the second region and the third region,

(C-1) one source/drain region of the third transistor constitutes the channel forming region of the first transistor,

(C-2) the other source/drain region of the third transistor is formed of the fifth region,

(C-3) the channel forming region of the

- 462 -

third transistor constitutes the other source/drain region of the first transistor,

(D-1) the gate regions of the junction-field-effect transistor are formed of the fifth region and part of the second region which part is opposed to the fifth region,

(D-2) the channel region of the junction-field-effect transistor is formed of part of the fourth region which part is interposed between the fifth region and said part of the second region,

(D-3) one source/drain region of the junction-field-effect transistor is formed of a portion of the fourth region which portion extends from one end of the channel region of the junction-field-effect transistor and constitutes the other source/drain region of the first transistor,

(D-4) the other source/drain region of the junction-field-effect transistor is formed of a portion of the fourth region which portion extends from the other end of the channel region of the junction-field-effect transistor,

(E-1) one end of the MIS type diode is formed of part of the second region,

(E-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to said part of the second region constituting one end of the MIS type diode, through a wide gap thin film,

(F) the gate shared by of the first transistor and the third transistor and the gate of the second transistor are connected to a first line for memory cell selection,

(G) the third region is connected to a write-in information setting line,

(H) said portion of the fourth region constituting the other source/drain region of the junction-field-effect transistor is connected to a second line,

- 463 -

(I) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential, and

(J) the first region is connected to a fourth line.

217. The semi-conductor memory cell according to claim 216, wherein the electrode is connected to the third line having a predetermined potential through a high-resistance element.

218. The semi-conductor memory cell according to claim 217, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

219. The semi-conductor memory cell according to claim 216, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the first region and the potential in the other end of the MIS type diode.

220. The semiconductor memory cell according to claim 219, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode,

- 464 -

whereby carrier multiplication takes place, holes or electrons are stored in said portion of the first region constituting one end of the MIS type diode depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

221. A semiconductor memory cell having a semiconductor layer having two main surfaces opposed to each other, the main surfaces being a first main surface and a second main surface,

the semiconductor memory cell comprising;

(1) a first transistor for readout, having a first conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(2) a second transistor for switching, having a second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate capacitively coupled with the channel forming region,

(3) a third transistor for current control, having the second conductivity type, and having source/drain regions, a semi-conductive channel forming region which is in contact with the source/drain regions and spaces out the source/drain regions, and a gate

- 465 -

capacitively coupled with the channel forming region,

(4) a first junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions,

(5) a second junction-field-effect transistor for current control, having source/drain regions, a channel region and gate regions, and

(6) an MIS type diode for retaining information,

the semiconductor memory cell further having;

(a) a semi-conductive first region which is formed in the semiconductor layer to extend over from the first main surface to the second main surface and has a first conductivity type,

(b) a semi-conductive second region which is formed in the semiconductor layer to extend over from the first main surface to the second main surface, is in contact with the first region and has a second conductivity type,

(c) a third region which is formed in a surface region including the second main surface of the first region to be spaced from the second region and is in contact with the first region so as to form a rectifier junction together with the first region,

(d) a fourth region which is formed in a surface region including the first main surface of the second region to be spaced from the first region and is in contact with the second region so as to form a rectifier junction together with the second region,

(e) a fifth region which is formed in a surface region including the first main surface of the first region to be spaced from the second region and is in contact with the first region so as to form a rectifier junction together with the first region,

(f) a sixth region which is formed in a surface region of the fourth region and is in contact

- 466 -

with the fourth region so as to form a rectifier junction together with the fourth region,

(g) the gate formed on a first insulation layer formed on the first main surface so as to bridge the first region and the fourth region and so as to bridge the second region and the fifth region, and is shared by the first transistor and the third transistor, and

(h) the gate of the second transistor formed on a second insulation layer formed on the second main surface so as to bridge the second region and the third region,

wherein:

(A-1) one source/drain region of the first transistor is formed of a surface region including the first main surface of the first region,

(A-2) the other source/drain region of the first transistor is formed of the fourth region,

(A-3) the channel forming region of the first transistor is formed of a surface region including the first main surface of the second region which surface region is interposed between the surface region including the first main surface of the first region and the fourth region,

(B-1) one source/drain region of the second transistor is formed of a surface region including the second main surface of the second region,

(B-2) the other source/drain region of the second transistor is formed of the third region,

(B-3) the channel forming region of the second transistor is formed of a surface region including the second main surface of the first region which surface region is interposed between the surface region including the second main surface of the second region and the third region,

(C-1) one source/drain region of the third transistor constitutes the channel forming region of the

- 467 -

first transistor,

(C-2) the other source/drain region of the third transistor is formed of the sixth region,

(C-3) the channel forming region of the third transistor constitutes the other source/drain region of the first transistor,

(D-1) the gate regions of the first junction-field-effect transistor are formed of the fifth region and the third region which is opposed to the fifth region,

(D-2) the channel region of the first junction-field-effect transistor is formed of part of the first region which part is interposed between the fifth region and the third region,

(D-3) one source/drain region of the first junction-field-effect transistor is formed of a portion of the first region which portion extends from one end of the channel region of the first junction-field-effect transistor and constitutes one source/drain region of the first transistor and the channel forming region of the second transistor,

(D-4) the other source/drain region of the first junction-field-effect transistor is formed of a portion of the first region which portion extends from the other end of the channel region of the first junction-field-effect transistor,

(E-1) the gate regions of the second junction-field-effect transistor are formed of the sixth region and part of the second region which part is opposed to the sixth region,

(E-2) the channel region of the second junction-field-effect transistor is formed of part of the fourth region which part is interposed between the sixth region and said part of the second region,

(E-3) one source/drain region of the second junction-field-effect transistor is formed of a portion of the fourth region which portion extends from one end

- 468 -

of the channel region of the second junction-field-effect transistor and constitutes the other source/drain region of the first transistor,

(E-4) the other source/drain region of the second junction-field-effect transistor is formed of a portion of the fourth region which portion extends from the other end of the channel region of the second junction-field-effect transistor,

(F-1) one end of the MIS type diode is formed of part of the second region,

(F-2) an electrode constituting the other end of the MIS type diode is formed to be opposed to said part of the second region constituting one end of the MIS type diode, through a wide gap thin film,

(G) the gate shared by of the first transistor and the third transistor and the gate of the second transistor are connected to a first line for memory cell selection,

(H) the third region is connected to a write-in information setting line,

(I) said portion of the fourth region constituting the other source/drain region of the second junction-field-effect transistor is connected to a second line,

(J) the electrode constituting the other end of the MIS type diode is connected to a third line having a predetermined potential, and

(K) the fifth region is connected to a fourth line.

222. The semi-conductor memory cell according to claim 221, wherein the fifth region is connected to the write-in information setting line in place of being connected to the fourth line.

223. The semi-conductor memory cell according to claim 221, wherein the electrode is connected to the

- 469 -

third line having a predetermined potential through a high-resistance element.

224. The semi-conductor memory cell according to claim 223, wherein the electrode and the high-resistance element are integrally formed and are composed of a silicon thin layer.

225. The semi-conductor memory cell according to claim 221, wherein the wide gap thin film is composed of a material in which the tunnel transition of carriers is caused depending upon a potential difference between the potential in the first region and the potential in the other end of the MIS type diode.

226. The semiconductor memory cell according to claim 225, wherein binary information of first information or second information is stored in the semiconductor memory cell, the first information to be stored in the semiconductor memory cell corresponds to a first potential in the channel forming region of the first transistor, and the second information to be stored in the semiconductor memory cell corresponds to a second potential in the channel forming region of the first transistor,

(i) when the potential in the channel forming region of the first transistor is the first potential, the tunnel transition of carriers is caused from the other end to one end of the MIS type diode, whereby carrier multiplication takes place, holes or electrons are stored in said portion of the first region constituting one end of the MIS type diode depending upon the conductivity type of one end of the MIS type diode, and the potential in the channel forming region of the first transistor is held nearly at the first potential, and

(ii) when the potential in the channel

- 470 -

forming region of the first transistor is the second potential, carriers having the polarity opposite to that of the above carriers transit from one end to the other end of the MIS type diode, whereby the potential in the channel forming region of the first transistor is held at the second potential.

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