

WHAT IS CLAIMED IS:

1. A decoder, the decoder comprising circuitry configured to:
 - receive a bitstream including a coded picture, the coded picture including a first region
 - 5 having a first plurality of coding units and a second region having a second plurality of coding units;
 - construct for each coding unit in the first region a motion vector candidate list, each motion vector candidate list having a common motion vector, wherein the order of the motion vector candidates in each motion vector candidate list is determined without regard to frequency
 - 10 of use and the motion vector candidate lists are ordered such that the common motion vector is first;
 - decode the first plurality of coding units using the common motion vector from the motion vector candidate lists, whereby a picture region with common motion is reconstructed in the first region;
 - 15 ascertain from the bitstream individually determined motion vectors for each coding unit of the second region, wherein adjacent coding units in the second region have different individually determined motion vectors, each individually determined motion vector being one of a translational motion vector or a control point motion vector for four parameter or six parameter affine motion; and
 - 20 decode the second plurality of coding units using the individually determined motion vectors, whereby local motion in the second region is reconstructed.
2. The decoder of claim 1, the decoder configured to determine global motion is indicated for the coded picture.
- 25 3. The decoder of claim 1, wherein the common_motion vector includes a control point motion vector.
4. The decoder of claim 3, wherein the control point motion vector is a translational motion
- 30 vector.

5. The decoder of claim 3, wherein the control point motion vector is a vector of a four parameter affine motion model.

6. The decoder of claim 3, wherein the control point motion vector is a vector of a six parameter affine motion model.

7. The decoder of claim 1, the decoder further comprising:

an entropy decoder processor configured to receive the bitstream and decode the bitstream into quantized coefficients;

an inverse quantization and inverse transformation processor configured to process the quantized coefficients including performing an inverse discrete cosine;

a deblocking filter;

a frame buffer; and

an intra prediction processor.

8. The decoder of claim 1, wherein at least a coding unit of the first plurality of coding units forms part of a quadtree plus binary decision tree.

9. The decoder of claim 1, wherein at least a coding unit of the first plurality of coding units is a coding tree unit.

10. The decoder of claim 1, wherein at least a coding unit of the first plurality of coding units is a coding unit.