CLAIMS

What is claimed is :

1. A microelectronic device, comprising:

a microelectronic device structure having a memory array region and a staircase region, the microelectronic device structure comprising:

a stack structure having tiers each comprising a conductive structure and an insulative structure vertically neighboring the conductive structure, the stack structure comprising:

a deck comprising a group of the tiers;

an additional deck vertically overlying the deck and comprising an additional group of the tiers; and

an interdeck section vertically between the deck and the additional deck, the interdeck section comprising:

a dielectric structure horizontally confined within the memory array region and absent from a horizontal area of the staircase region; and

another group of the tiers horizontally confined within of the staircase region and within vertical boundaries of the dielectric structure and;

staircase structures horizontally confined within the staircase region and having steps comprising edges of the tiers of the stack structure within the deck and the additional deck; and

semiconductive pillar structures horizontally confined within the memory array region and vertically extending through the stack structure.

2. The microelectronic device of claim 1, further comprising plug structures within dielectric structure and horizontally surrounding the semiconductive pillar structures.

3. The microelectronic device of claim 1, wherein the other group of the tiers within the interdeck section of the stack structure comprises at least two of the tiers of the stack structure.

4. The microelectronic device of any one of claims 1 through 3, wherein the dielectric structure and the insulative structure of each of the tiers of the stack structure comprise at least one dielectric oxide material.

5. The microelectronic device of any one of claims 1 through 3, wherein the interdeck section of the stack structure is free of any portions of the staircase structures within vertical boundaries thereof.

6. The microelectronic device of any one of claims 1 through 3, wherein the staircase structures comprise:

a first stadium structure within the deck of the stack structure and comprising:

a first staircase structure having positive slope; and

a second staircase structure opposing the first staircase structure and having negative slope; and

a second stadium structure within the additional deck of the stack structure and comprising:

a third staircase structure having positive slope; and

a fourth staircase structure opposing the third staircase structure and having negative slope.

7. A method of forming a microelectronic device, comprising:

forming a microelectronic device structure having a memory array region and a staircase region, the microelectronic device structure formed to comprise a first preliminary stack structure comprising a vertically alternating sequence of first insulative structures and second insulative structures arranged in tiers;

forming a dielectric structure within an upper portion of the first preliminary stack structure, the dielectric structure confined within horizontal boundaries of the memory array region and absent from a horizontal area of the staircase region;

forming a second preliminary stack structure over the first preliminary stack structure and the dielectric structure, the second preliminary stack structure comprising a vertically alternating sequence of

additional first insulative structures and additional second insulative structures arranged in additional tiers;

forming semiconductive pillar structures vertically extending through portions of the second preliminary stack structure, the dielectric structure, and the first preliminary stack structure within the memory array region;

forming staircase structures within the portions of the second preliminary stack structure and the first preliminary stack structure within the staircase region, some of the staircase structures having steps comprising horizontal ends of the tiers of the first preliminary stack structure and other of the staircase structures having additional steps comprising horizontal ends of the additional tiers of the second preliminary stack structure; and

at least partially replacing the second insulative structures and the additional second insulative structures with conductive structures.

8. The method of claim 7, wherein forming a dielectric structure within an upper portion of the first preliminary stack structure comprises:

forming a photoresist structure over portions of the first preliminary stack structure within the staircase region;

selectively removing the upper portion of the first preliminary stack structure using the photoresist structure as a mask to form a recess within the first preliminary stack structure and confined within the horizontal boundaries of the memory array region;

forming a dielectric fill material over exposed surfaces of the first preliminary stack structure inside and outside of the recess; and

removing portions of the dielectric fill material outside of horizontal boundaries and vertical boundaries of the recess to form the dielectric structure.

9. The method of claim 7, further comprising selecting the first insulative structures of the first preliminary stack structure, the dielectric structure, and the additional first insulative structures of the second preliminary stack structure to each comprise a dielectric oxide material.

10. The method of any one of claims 7 through 9, wherein forming semiconductive pillar structures comprises:

forming openings vertically extending through the dielectric structure and a lower portion of the first preliminary stack structure underlying the dielectric structure;

covering the openings with plug structures that partially vertical extend into the openings;

forming the second preliminary stack structure over the first preliminary stack structure, the dielectric structure, and the plug structures;

forming additional openings vertically extending through second preliminary stack structure and the plug structures and to remaining portions of the openings to form relatively larger openings; and

filling the relatively larger openings with semiconductive material.

11. The method of any one of claims 7 through 9, wherein forming staircase structures within the portions of the second preliminary stack structure and the first preliminary stack structure within the staircase region comprises:

forming a stadium structure within the second preliminary stack structure, the stadium structure comprising:

a first of the staircase structures having positive slope; and

a second of the staircase structures opposing the first of the staircase structures and having negative slope; and

forming an additional stadium structure within the first preliminary stack structure, the additional stadium structure comprising:

a third of the staircase structures having positive slope; and

a fourth of the staircase structures opposing the third of the staircase structures and having negative slope.

12. The method of claim 11, wherein forming an additional stadium structure within the first preliminary stack structure comprises subjecting the second preliminary stack structure to a chopping

process to vertically extend an opening defined by another stadium structure formed within the second preliminary stack structure into the first preliminary stack structure and form the additional stadium structure.

13. The method of claim 7, wherein at least partially replacing the second insulative structures and the additional second insulative structures with conductive structures comprises at least partially replacing the second insulative structures and the additional second insulative structures with tungsten.

14. A microelectronic device, comprising:

a microelectronic device structure comprising:

a stack structure having tiers each comprising a conductive structure and an insulative structure vertically neighboring the conductive structure, the stack structure comprising:

a lower deck comprising some of the tiers;

an upper deck overlying the lower deck and comprising other of the tiers; and

an interdeck section between the lower deck and the upper deck, the interdeck section comprising:

an interdeck dielectric structure horizontally confined within the memory array region and absent from a horizontal area of the staircase region; and

additional tiers horizontally between the interdeck dielectric structure, the additional tiers each comprising an additional insulative structure and a further insulative structure vertically neighboring the additional insulative structure;

staircase structures having steps comprising edges of the tiers of the stack structure within the lower deck and the upper deck; and

semiconductive pillar structures vertically extending through the stack structure.

15. The microelectronic device of claim 14, wherein the semiconductive pillar structures are

positioned horizontally between the interdeck dielectric structures.

16. The microelectronic device of claim 15, wherein the semiconductive pillar structures vertically extend through a first group of the tiers within the upper deck of the stack structure, the additional tiers of the stack structure within the interdeck section of the stack structure, and a second group of the tiers within the lower deck of the stack structure.

17. The microelectronic device of any one of claims 14 through 16, further comprising filled slots vertically extending through the tiers of the stack structure and the interdeck dielectric structures, the filled slots each filled with at least one dielectric material.

18. The microelectronic device of any one of claims 14 through 16, wherein the interdeck dielectric structures, the insulative structure of each of the tiers within the lower deck and the upper deck of the stack structure, and the additional insulative structure of each of the additional tiers within the interdeck section of the stack structure comprise at least one dielectric oxide material.

19. The microelectronic device of claim 18, wherein the further insulative structure of each of the additional tiers within the interdeck section of the stack structure comprises at least one dielectric nitride material.

20. The microelectronic device of any one of claims 14 through 16, wherein the staircase structures comprise:

a stadium structure within the upper deck of the stack structure and comprising:

a first staircase structure having positive slope; and

a second staircase structure mirroring the first staircase structure and having negative slope; and

an additional stadium structure within the lower deck of the stack structure and comprising:

a third staircase structure having positive slope; and

a fourth staircase structure mirroring the third staircase structure and having negative slope.

21. A method of forming a microelectronic device, comprising:

forming a microelectronic device structure comprising a first preliminary stack structure comprising a vertically alternating sequence of first insulative structures and second insulative structures arranged in tiers, the microelectronic device structure including a memory array region and a staircase region;

forming dielectric structures vertically extending into the first preliminary stack structure, the dielectric structures horizontally confined within the memory array region and absent from a horizontal area of the staircase region;

forming a second preliminary stack structure over the first preliminary stack structure and the dielectric structures, the second preliminary stack structure comprising a vertically alternating sequence of additional first insulative structures and additional second insulative structures arranged in additional tiers;

forming semiconductive pillar structures vertically extending through portions of the second preliminary stack structure and the first preliminary stack structure positioned horizontally between the dielectric structures;

forming staircase structures within the second preliminary stack structure and the first preliminary stack structure, some of the staircase structures having steps comprising edges of the tiers of the first preliminary stack structure and other of the staircase structures having additional steps comprising edges of the additional tiers of the second preliminary stack structure; and

replacing the additional second insulative structures of the second preliminary stack structure and the second insulative structures of the first preliminary stack structure positioned outside of vertical boundaries of the dielectric structures with conductive structures.

22. The method of claim 21, wherein forming dielectric structures vertically extending into of the first preliminary stack structure comprises:

forming a photoresist structure over the first preliminary stack structure, the photoresist structure comprising a photoresist material have openings vertically extending therethrough;

selectively removing upper portions of the first preliminary stack structure exposed by and within horizontal boundaries of the openings in the photoresist material of the photoresist structure to form recesses within the first preliminary stack structure;

forming a dielectric fill material over exposed surfaces of the first preliminary stack structure inside and outside of the recesses; and

removing portions of the dielectric fill material outside of boundaries of the recesses to form the dielectric structures.

23. The method of claim 21, further comprising:

selecting the first insulative structures of the first preliminary stack structure, the dielectric structures, and the additional first insulative structures of the second preliminary stack structure to each comprise a dielectric oxide material; and

selecting the second insulative structures of the first preliminary stack structure and the additional second insulative structures of the second preliminary stack structure to each comprise a dielectric nitride material.

24. The method of any one of claims 21 through 23, wherein forming semiconductive pillar structures comprises:

forming openings vertically extending through portions of the tiers of the first preliminary stack structure positioned horizontally between the dielectric structures;

covering the openings with plug structures that partially vertical extend into the openings;

forming the second preliminary stack structure over the first preliminary stack structure, the dielectric structures, and the plug structures;

forming additional openings vertically extending through second preliminary stack structure and the plug structures and to remaining portions of the openings to form relatively larger openings; and

filling the relatively larger openings with semiconductive material.

25. The method of any one of claims 21 through 23, wherein forming staircase structures

within the second preliminary stack structure and the first preliminary stack structure comprises:

forming a first stadium structure within the second preliminary stack structure, the first stadium structure comprising:

a first of the staircase structures; and

a second of the staircase structures mirroring the first of the staircase structures; and

forming a second stadium structure within the first preliminary stack structure, the second stadium structure comprising:

a third of the staircase structures; and

a fourth of the staircase structures mirroring the third of the staircase structures.

26. The method of claim 25, wherein forming a second stadium structure within the first preliminary stack structure comprises vertically extending an opening defined by a third stadium structure formed within the second preliminary stack structure into the first preliminary stack structure to form the second stadium structure.

27. An electronic system, comprising:

an input device;

an output device;

a processor device operably coupled to the input device and the output device; and

a memory device operably coupled to the processor device and comprising at least one microelectronic device structure having a memory array region and a staircase region, the at least one microelectronic device structure comprising:

a stack structure having tiers each comprising a conductive structure and an insulative structure vertically neighboring the conductive structure, the stack structure comprising:

a deck comprising some of the tiers;

an additional deck vertically overlying the deck and comprising other of the tiers; and

an interdeck section vertically between the deck and the additional deck, the interdeck section comprising at least one dielectric structure within horizontal boundaries of

the memory array region and absent from a horizontal area of the staircase region;

staircase structures within the staircase region and having steps comprising edges of the tiers of the stack structure within the deck and the additional deck; and

semiconductive pillar structures within the memory array region and vertically extending through the stack structure.