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(71) Applicant (for all designated States except US): IVP INTEGRATED VISION PRODUCTS AB [SE/SE]; Teknikringen 2C, S-583 30 Linköping (SE).			
(72) Inventors; and (75) Inventors/Applicants (for US only): FORCHHEIMER, Robert [SE/SE]; Tingsvägen 24A, S-582 49 Linköping (SE). ÅSTRÖM, Anders [SE/SE]; Heidenstams gatan 15, S-582 49 Linköping (SE).			
(74) Agents: WILLQUIST, Bo et al.; Albihn Willquist AB, S:t Larsgatan 23, S-582 24 Linköping (SE).		SG 9700312-3 Published With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments. In English translation (filed in Swedish).	

(54) Title: ARRANGEMENT AT AN IMAGE PROCESSOR

(57) Abstract

The present invention relates to a parallel processor containing a number of processor elements of the same type which are integrated on one and the same semiconductor chip. The processor is of the type that allows image and signal processing of the information stored in the processor element. The device contains a unit block (3) for each processor element and is characterised in that each unit block comprises at least two incrementing units (1a, 1b) which are designed to add a signal supplied to the unit block and a signal which originates from an incrementing unit corresponding to the respective unit in the closest preceding unit block in every direction of the processor element matrix. Every unit block (3) further contains at least one logical unit (2) which is designed to perform Boolean logic operations on the signals received from the incrementing units of the unit block.

