



(51) International Patent Classification:

G11C 5/14 (2006.01) *G11C 11/4091* (2006.01)
G11C 7/06 (2006.01)

(21) International Application Number:

PCT/EP2013/071159

(22) International Filing Date:

10 October 2013 (10.10.2013)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

1259685 10 October 2012 (10.10.2012) FR

(71) Applicant: SOITEC [FR/FR]; Chemin des Franques, F-38190 Bernin (FR).

(72) Inventor: THEWES, Roland; Herbststr. 16, 82178 Puchheim (DE).

(74) Agent: REGIMBEAU; 20, rue de Chazelles, F-75847 Paris Cedex 17 (FR).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,

BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

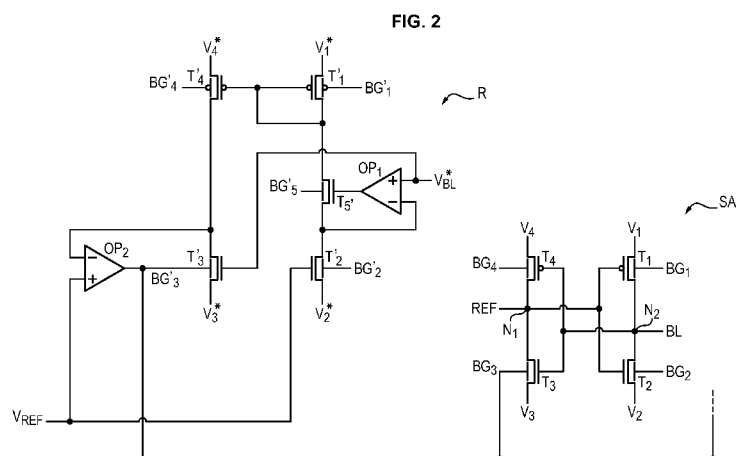
Declarations under Rule 4.17:

— of inventorship (Rule 4.17(iv))

Published:

— with international search report (Art. 21(3))

(54) Title: REFERENCE CIRCUIT TO COMPENSATE FOR PVT VARIATIONS IN SINGLE-ENDED SENSE AMPLIFIERS



(57) Abstract: The invention relates to a semiconductor memory device comprising: - a single-ended sense amplifier (SA) circuit for reading data sensed from selected memory cells in a memory array, the sense amplifier having a first node (N1) used to feed in a reference signal (REF), a second node (N2) coupled to a bit line (BL), and sense transistors (T2, T3) responsible for amplifying the content of a selected memory cell during a sense operation, - a reference circuit (R) having replica transistors (T2, T3) of the sense transistors (T2, T3) and further comprising a regulation network (OP1, T5; OP2) designed so that each replica transistor operates in a stable operating point, and wherein the regulation network generates a control voltage which is applied to the sense amplifier circuit.