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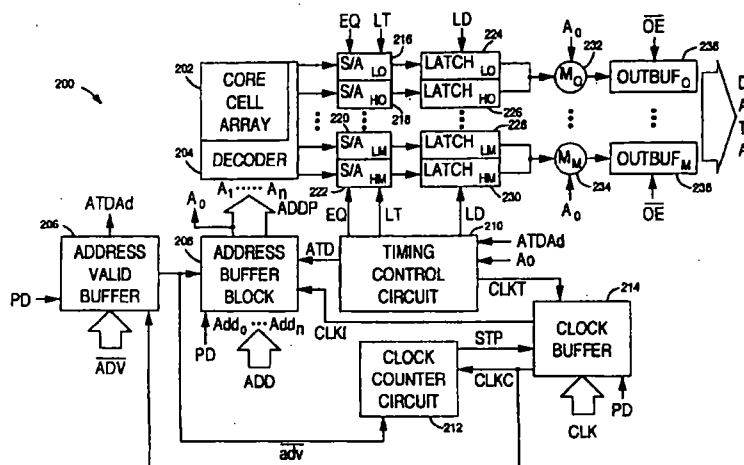
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(54) Title: BURST ARCHITECTURE FOR A FLASH MEMORY



- (57) Abstract:** A burst mode architecture to provide burst mode access to a plurality of data words in a flash memory is described. The burst mode architecture includes a first circuit (216, 220), a control circuit (210) coupled to the first circuit (216, 220), and a data buffer (236, 238) selectively coupled to the first circuit (216, 220) by the control circuit (210). The first circuit (216, 220) accesses a plurality of data words, beginning with an initial access of a first data word and a second data word. The control circuit (210) generates a timing signal having pulses and a second signal. The second signal is generated upon completion of the initial access of the first data word and the second data word. The first circuit (216, 220) follows the initial access with subsequent accesses of the plurality of data words responsively to the second signal and the timing signal. The data buffer has an output and procedures the first data word at the output and successively produces, with each successive pulse of the timing signal following an initial period of time, the second data word, and subsequent data words at the output. The subsequent data words correspond to the subsequent accesses of the plurality of data words.



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