Description

This invention relates to analog comparators and to methods of comparing voltages.

An analog comparator is a basic functional unit utilized in analog circuit design, as, for example, in analog-to-digital converters (ADCs). The relative performance of analog comparators is measured by their specifications, such as input offset voltage, offset current, propagation delay, skew, power consumption, etc. In some applications, the input offset voltage and offset current specification can be relaxed (traded off) when other performance criteria are critical. For example, in optical and digital data receivers or in high speed medium resolution ADCs having embedded analog comparators, e.g., those used in video applications (eight or nine bit resolution with ten megahertz conversion rates), low propagation delay through the analog comparators is the most important criteria. Alternatively, in low speed medium resolution ADCs having embedded analog comparators, e.g., ADCs used in telephone (voice) applications where many thousands thereof are employed in channel banks and line cards of switching systems (eight to twelve bits resolution, eight kilohertz conversion rates), the power consumption of the analog comparators is of primary importance. Hence, it is desirable to have a single analog comparator design easily adaptable for any application.

IBM Technical Disclosure Bulletin, vol.16, no.10, March 1974, pages 3227 to 3228, and US-A-3870966 disclose a differential amplifier having a single amplifier for each input powered by common power buses. The buses are powered by variable resistances coupling to the power supplies.

According to one aspect of this invention there is provided an analog comparator as claimed in claim 1.

According to another aspect of this invention there is provided a method of comparing voltages as claimed in claim 9.

Advantages of embodiments of the invention include a fully differential analog comparator having substantially identical propagation delay from either one of two inputs. The comparator has very low sensitivity to power supply noise and the gain of the comparator can be scaled as needed. Additionally, the comparator can be adapted such that the average differential output voltage (output common mode voltage) can be adjusted for optimally driving subsequent amplifier stages, such as digital inverters. Further, the average differential input voltage (input common mode voltage) can be compensated for to provide precise control of the output common mode voltage with varying input common mode voltage.

The invention will now be described with reference to the accompanying drawings, in which:

FIG. 1 is a schematic of the analog comparator embodying the invention; and

FIGS. 2,3 and 4 are improvements to the analog comparator of FIG. 1.

Detailed Description

A novel, fully-differential analog comparator 20 is shown schematically in FIG. 1 for integration into a common substrate. Two strings 21, 21' of cascaded gain stages 22 provide a predetermined amount of voltage gain for corresponding inputs V+ and V- of comparator 20. Output from each string 21, 21' couples to corresponding node 35, 35'. Each string 21, 21' has the same number of stages 22, and, typically, no more than one or two stages 22 in each string 21, 21' are necessary. Each gain stage 22 resembles a conventional CMOS inverter, having an input terminal 23, an output terminal 24 and two power supply terminals 25, 26. In an exemplary stage 22, a P-channel FET 30 and an N- channel FET 31 are shown having common gates coupling to the input terminal 23 and common drains coupling to output terminal 24. Although shown here as P- and N- channel FETs, it is understood that the P- and N- channel FETs can be interchanged with a corresponding change in power supply polarity. The source of FET 30 couples to power terminal 25, while the source of FET 31 couples to power terminal 26. The ratio of the sizes of FET 30 to FET 31 will be discussed in more detail below, but it is sufficient to state here that the conventional sizing ratio of FET 30 to FET 31, being approximately two- or three-to-one, will produce a comparator 20 having substantially zero propagation delay skew.

The power terminals 25, 26, of cascaded gain stages 22 couple to corresponding buses 32, 33. Buses 32, 33 are powered by current mirrors 40, 50, respectively. Mirrors 40, 50 are correspondingly powered by V_{DD}, the most positive power supply, and V_{SS}, the most negative power supply, which is typically at ground or zero volts. The current mirrors 40, 50 serve to isolate the buses 32, 33 from V_{DD} and V_{SS}, reducing the susceptibility of the comparator 20 to electrical noise on the power supplies V_{DD}, V_{SS}.

Current mirror 40 is shown here as a conventional Widlar current mirror with multiple outputs, but it is understood that other types of current mirrors, such as Wilson or compound current mirrors, may be used. FET 42 of mirror 40 couples to a current source 44, setting the amount supplied by mirror 40 and the overall power current consumption of the comparator 20. Typical current supplied by current source 44 is 100 microamperes to 1 milliamperes depending on output load capacitance on nodes 35, 35' and the desired speed of the comparator 20. FETs 48, 46, 47 of source 40 are sized such that the currents flowing out of the FETs 48, 46, 47 are substantially the same. FET 48 supplies current to bus 32.

Current mirror 50, shown here as a compound current mirror formed by FETs 51, 52, 53, 54, 55, ac-

cepts current from the outputs of the current mirror 40 into control current input nodes 56 of the mirror 50. The resulting mirrored current is inputed from bus 33 into serially connected FETs 54, 55 through mirrored current input node 57. Control current output from control current output nodes 58 of the mirror 50 passes through FETs 61, 62 to the most negative power supply, V_{SS}. As will be discussed in greater detail below, FETs 61, 62 are operated in the triode, or ohmic, region and have substantially the same size. Likewise, mirrored current output from mirrored current output node 59 of mirror 50 passes through paralleled FETs 65, 66 to V_{SS}. Again, as will be discussed in greater detail below, FETs 65, 66 operate in the triode, or ohmic, region and have substantially the same size. As stated above, the current mirror 50 is a compound current mirror for the accurate mirroring of current and is preferably a unity gain current mirror with FETs 51, 53, 54, 55 having substantially the same size. For purposes here, operation of the current mirror 50 is described briefly herein. FET 52 of the mirror 50 establishes a stable gate voltage for FETs 51 and 54 and is typically one-quarter or less the sizes of FETs 51, 53, 54, 55. Further, FET 52 has a sufficiently high threshold voltage to ensure that FETs 51, 53, and correspondingly, FETs 54, 55, are saturated. FET 51 equalizes the drain-to-source voltages on FET 55 and FET 53, substantially eliminating offset currents in the mirror 50. The serially coupled FETs 54, 55 provide a high impedance current sink at node 57 for current from bus 33. Although a simpler current mirror can be used for current mirror 50, such as a Widlar mirror, the more precise the current is mirrored and the higher the impedance of the mirrored current input node 57 is, the better the accuracy of the comparator 20. Therefore, a suitably adapted Wilson current mirror could be used as mirror 50.

Voltage source 68, coupling to the common gate of FETs 61, 62, is a reference voltage for the average voltage on the output nodes 35, 35′ of the strings 21, 21′ to achieve, and is referred to here as the output common mode voltage level set. The desirability of adjusting the output common mode voltage strings 21, 21′ will be discussed below, but for purposes here, the interface of the strings 21, 21′ to a load can be optimized for the characteristics of the load, e.g., digital inverter stages coupled to nodes 35, 35′. Similarly, the paralleled FETs 65, 66, responsive to the voltages on the output nodes 35, 35′ of strings 21, 22 are combined so that the paralleled resistances of the FETs 65, 66 correspond to the average of the voltages on the output nodes 35, 35′, the output common mode voltage. Put another way, the paralleled resistances of FETs 65, 66 represent the output common mode voltage of the cascaded stages 22 of strings 21, 21′. For the purposes of this discussion, it is assumed that the input voltages to comparator 20 (V+, V-) are substantially the same, the threshold "trip point" of the comparator 20. This corresponds to a zero voltage differential input to inputs V+,V- and is useful for examining the biasing and operation of comparator 20. It is understood, however, that the following also applies when the voltage of inputs V+, V- are not substantially the same. It is desired that the output common mode voltage of the strings 21, 21′ be substantially the same as the voltage from source 68. To do so, the resistances of FETs 65, 66 and 61, 62 deviate the current gain of the mirror 50 from unity when the output common mode voltage is not substantially the same as the voltage of source 68. As such, the resistances of FETs 61, 62 are substantially the same and are invariant since the voltage of source 68, for purposes here, is invariant. However, the combined resistances of FETs 65, 66 vary inversely proportionally with the voltages on the output nodes 35, 35′ of the strings 21, 21′, which are dependent on the voltage on the bus 33, hence dependent on the current flowing through the current mirror 50. Since the current through the control current input nodes 56 and through the control current output nodes 58 does not vary, for the comparator 20 to be in equilibrium, there must be substantially equal current flow in the mirrored current and the control current, i.e., unity current gain of the mirror 50. For unity current gain, the combined resistances of the FETs 65, 66 must be substantially the same as the resistances of FETs 61, 62. Hence the average of the voltages on the gates of FETs 65, 66 must be substantially the same as the voltage from voltage source 68, i.e., the output common mode voltage from the cascaded gain stages 22 is substantially the same as the voltage from source 68.

The output nodes 35, 35′ couple to corresponding buffers 45, operating as a conventional CMOS digital inverter. Although only one buffer 45 is shown corresponding to each string 21, 21′, it is understood that multiple, cascaded buffers 45 can be used. Output terminals 24 of buffers 45 are the outputs for the comparator 20, OUTPUT and OUTPUT'. Buffers 45 are similar in structure to a gain stage 22 but with as small a device as possible to reduce capacitive loading of the strings 21, 21′. Power supply terminals 25, 26 of buffers 45 couple to power sources V_{DD} and V_{SS} instead of buses 32, 33. As will be discussed in more detail below, the sizing of the FETs in each buffer 45, corresponding to FETs 30, 31 in stage 22, is typically two- or three-to-one, respectively, for minimum propagation delay skew and a threshold voltage of substantially one-half the voltage difference between V_{DD} and V_{SS}.

The ability to adjust the output common mode voltage of strings 21, 21′ can be used advantageously by recognizing that optimal operation of the comparator 20 requires that, when the voltage on V+ is approximately the same as the voltage on V-, the voltag-

es on nodes 35, 35' should be approximately the threshold voltages of buffers 45. The threshold voltage of the buffer 45 is the input voltage at which the output of the buffer 45 transitions from V_{DD} to V_{SS}, and vice versa. This minimizes propagation delay skew through comparator 20. Therefore, the output common mode voltage of strings 21, 21' should be approximately the threshold voltage of buffers 45. This is accomplished by having the voltage of voltage source 68 be substantially that of the threshold voltage of buffers 45. Referring temporarily to FIG. 2, source 68 (FIG. 1) is shown having a buffer 75, substantially similar to the buffers 45 in FIG. 1 and preferably integrated on the same substrate therewith, with input terminal 23 coupling to output terminal 24 and with power terminals 25, 26 coupling to corresponding power sources V_{DD} and V_{SS}. Having buffer 75 operating with input 23 coupled to output 24, the voltage on input terminal 23 is substantially the threshold voltage of the buffer 75. Hence the voltage of voltage source 68 (FIG. 1) is substantially the threshold voltage of buffers 45 (FIG. 1). By having buffer 75 on the same chip as buffers 45 (FIG. 2), variations in threshold voltage of buffers 45 due to temperature and processing variations will be compensated for by variations in threshold voltage of buffer 75.

Returning to FIG. 1, it is recognized that due to the finite output resistances of FETs, the output common mode voltage of strings 21, 21' will not precisely match that of voltage source 68 when inputs V+ and V- are substantially the same, i.e., when the input voltages are at the comparator threshold. As noted above, when the V+ and V- inputs are substantially the same, by virtue of the disclosed invention, the output common mode voltage of nodes 35, 35' should be substantially equal to the voltage of source 68. However, the voltage on bus 32 is different from the voltage on the drains of FETs 46,47, hence the voltage across FET 48 is different from the voltage across FETs 46, 47. This results in differing current flow through FETs 46, 47 from that through FET 48 due to the voltage across FETs 46, 47 being different from the voltage across FET 48 with the inherent output resistances of the FETs 46, 47, 48. Furthermore, the voltage on bus 32 varies with the average voltage of the inputs V+,V-, referred to here as the input common mode voltage. To compensate for the different current flow, the gain of the current mirror must decrease. This is accomplished by the output common mode voltage changing from the desired voltage until equilibrium is reached. To equalize the currents through FETs 46, 47, 48, and thus make the output common mode voltage on nodes 35, 35' more closely equal to the voltage of voltage source 68, at breakpoints 70, 70' and 71, 71', the circuit in FIG. 3 is substituted. In FIG. 3, two FETs 76, 77 have common gates coupling to a voltage source 78, referred to here as the input common mode voltage set. The FETs 76, 77, are each sized to be substantially 2N times the size of FET 30 in a gain stage 22 (FIG. 1), N being the number of gain stages 22 in a string 21, 21' and disposed on the same substrate as FET 30. This assures that the voltage across FETs 46, 47 is substantially the same as the voltage across FET 48 (FIG. 1) when the input common mode voltage of inputs V+, V- of comparator 20 (FIG. 1) is known. However, if the input common mode voltage is not known, then the circuit in FIG. 4 can be used to derive the input common mode voltage from inputs V+, V- by having FETs 79, 80, 81, 82 in the arrangement shown disposed between breakpoints 70, 70' and 71, 71' in FIG. 1 and preferably integrated onto a substrate common with the circuitry in FIG. 1. The sizes of FETs 79, 80, 81, 82 are each N times the size of FET 30 (FIG. 1), N being the number of stages 22 in a string 21, 21'. This will assure that the voltage across FETs 46, 47 is substantially the same as the voltage across FET 48 with varying input common mode voltage, thus ensuring that the output common mode voltage on nodes 35, 35' remains substantially the same as the voltage from voltage source 68.

As stated above, the sizing of the FETs 30, 31 in stages 22 and, correspondingly, in buffers 45 and 75 (FIG. 2), are an exemplary two- or three-to-one to yield a threshold voltage approximately one-half the voltage between power supply terminals 25, 26 and for minimum propagation delay skew. However, it is understood that the sizing of the FETs 30, 31 can be one-to-one for minimum propagation delay through stages 22, buffers 45, or any combination thereof.

Having described the preferred embodiment of this invention, it is apparent that other embodiments will occur to those skilled in the art.

Claims

1. An analog comparator formed on an integrated circuit for comparing a first voltage input to a second voltage input, comprising

a first gain stage (22) having an input, an output and first and second power terminals, the corresponding power terminals coupling to first and second buses, and the input coupling to the first voltage input of the comparator; and

a second gain stage having an input, an output and first and second power terminals, the corresponding power terminals coupling to the first and second buses, and the input coupling to the second voltage input of the comparator;

CHARACTERIZED BY

a first current mirror (40) having a transistor (48) with an output node for coupling a first current to the first bus (32); and

a second current mirror (50) having a tran-

es on nodes 35, 35′ should be approximately the threshold voltages of buffers 45. The threshold voltage of the buffer 45 is the input voltage at which the output of the buffer 45 transitions from V_{DD} to V_{SS}, and vice versa. This minimizes propagation delay skew through comparator 20. Therefore, the output common mode voltage of strings 21, 21′ should be approximately the threshold voltage of buffers 45. This is accomplished by having the voltage of voltage source 68 be substantially that of the threshold voltage of buffers 45. Referring temporarily to FIG. 2, source 68 (FIG. 1) is shown having a buffer 75, substantially similar to the buffers 45 in FIG. 1 and preferably integrated on the same substrate therewith, with input terminal 23 coupling to output terminal 24 and with power terminals 25, 26 coupling to corresponding power sources V_{DD} and V_{SS}. Having buffer 75 operating with input 23 coupled to output 24, the voltage on input terminal 23 is substantially the threshold voltage of the buffer 75. Hence the voltage of voltage source 68 (FIG. 1) is substantially the threshold voltage of buffers 45 (FIG. 1). By having buffer 75 on the same chip as buffers 45 (FIG. 2), variations in threshold voltage of buffers 45 due to temperature and processing variations will be compensated for by variations in threshold voltage of buffer 75.

Returning to FIG. 1, it is recognized that due to the finite output resistances of FETs, the output common mode voltage of strings 21, 21′ will not precisely match that of voltage source 68 when inputs V+ and V- are substantially the same, i.e., when the input voltages are at the comparator threshold. As noted above, when the V+ and V- inputs are substantially the same, by virtue of the disclosed invention, the output common mode voltage of nodes 35, 35′ should be substantially equal to the voltage of source 68. However, the voltage on bus 32 is different from the voltage on the drains of FETs 46,47, hence the voltage across FET 48 is different from the voltage across FETs 46, 47. This results in differing current flow through FETs 46, 47 from that through FET 48 due to the voltage across FETs 46, 47 being different from the voltage across FET 48 with the inherent output resistances of the FETs 46, 47, 48. Furthermore, the voltage on bus 32 varies with the average voltage of the inputs V+,V-, referred to here as the input common mode voltage. To compensate for the different current flow, the gain of the current mirror must decrease. This is accomplished by the output common mode voltage changing from the desired voltage until equilibrium is reached. To equalize the currents through FETs 46, 47, 48, and thus make the output common mode voltage on nodes 35, 35′ more closely equal to the voltage of voltage source 68, at breakpoints 70, 70′ and 71, 71′, the circuit in FIG. 3 is substituted. In FIG. 3, two FETs 76, 77 have common gates coupling to a voltage source 78, referred to here as the input common mode voltage set. The FETs 76, 77, are each sized to be substantially 2N times the size of FET 30 in a gain stage 22 (FIG. 1), N being the number of gain stages 22 in a string 21, 21′ and disposed on the same substrate as FET 30. This assures that the voltage across FETs 46, 47 is substantially the same as the voltage across FET 48 (FIG. 1) when the input common mode voltage of inputs V+, V- of comparator 20 (FIG. 1) is known. However, if the input common mode voltage is not known, then the circuit in FIG. 4 can be used to derive the input common mode voltage from inputs V+, V- by having FETs 79, 80, 81, 82 in the arrangement shown disposed between breakpoints 70, 70′ and 71, 71′ in FIG. 1 and preferably integrated onto a substrate common with the circuitry in FIG. 1. The sizes of FETs 79, 80, 81, 82 are each N times the size of FET 30 (FIG. 1), N being the number of stages 22 in a string 21, 21′. This will assure that the voltage across FETs 46, 47 is substantially the same as the voltage across FET 48 with varying input common mode voltage, thus ensuring that the output common mode voltage on nodes 35, 35′ remains substantially the same as the voltage from voltage source 68.

As stated above, the sizing of the FETs 30, 31 in stages 22 and, correspondingly, in buffers 45 and 75 (FIG. 2), are an exemplary two- or three-to-one to yield a threshold voltage approximately one-half the voltage between power supply terminals 25, 26 and for minimum propagation delay skew. However, it is understood that the sizing of the FETs 30, 31 can be one-to-one for minimum propagation delay through stages 22, buffers 45, or any combination thereof.

Having described the preferred embodiment of this invention, it is apparent that other embodiments will occur to those skilled in the art.

Claims

1. An analog comparator formed on an integrated circuit for comparing a first voltage input to a second voltage input, comprising

a first gain stage (22) having an input, an output and first and second power terminals, the corresponding power terminals coupling to first and second buses, and the input coupling to the first voltage input of the comparator; and

a second gain stage having an input, an output and first and second power terminals, the corresponding power terminals coupling to the first and second buses, and the input coupling to the second voltage input of the comparator;

CHARACTERIZED BY

a first current mirror (40) having a transistor (48) with an output node for coupling a first current to the first bus (32); and

a second current mirror (50) having a tran-

sistor (54) with a node for coupling a second current from the second bus (33);

the second current mirror (50) being responsive to an output current from the first current mirror (40) such that the second current is substantially the same as the first current.

2. A comparator as claimed in claim 1 comprising further gain stages whereby the first gain stage is the first stage in a first string (21) of cascaded gain stages (22,22); and the second gain stage is the first stage in a second string (21') of cascaded gain stages (22,22), each further stage having an input, an output and first and second power terminals, the corresponding power terminals coupling to the first and second buses.

3. A comparator as claimed in claim 1 or 2, comprising at least one digital inverter (45) responsive, as the case may be, to at least one of the outputs of the first and second gain stages, or to at least one of the outputs of the first and second strings.

4. A comparator as claimed in claim 1,2 or 3, wherein each gain stage comprises a first transistor (30) of a first polarity and a second transistor (31) of a second polarity, each transistor having two output terminals and an input terminal, the input terminals of the two transistors coupling together to form the input to the gain stage, two corresponding output terminals from the two transistors coupling together to form the output of the gain stage, and the remaining output terminals of the two transistors forming the corresponding first and second power terminals of the gain stage.

5. A comparator as claimed in claim 1,2,3 or 4 wherein the first current mirror has first and second outputs, the first output being the output node for coupling a first current to the first bus, the second current mirror comprises

a first control current input (56), a first control current output (58), a mirrored current input (57) and a mirrored current output (59), the first control current input coupling to the second output of the first current mirror and the mirrored current input being the node for coupling a second current from the second bus (33); and there is provided

a first node (68) having a first predetermined voltage thereon;

a first transistor network (61,62) having a first and second output terminals and an input terminal, the first output terminal coupling to the first control current output of the second current mirror, the second output terminal coupling to a first power source and the input terminal coupling to the first node; and

a second transistor network (65,66) having two output terminals and two input terminals, the corresponding output terminals coupling between the mirrored current output of the second current mirror and the first power source, each input terminal coupling to the corresponding output, as the case may be, of the first and second gain stage or the first and second string;

whereby the average of the voltages on the outputs, as the case may be, of the first and second gain stages or the first and second strings is approximately that of the first predetermined voltage on the first node.

6. A comparator as claimed in claim 5, wherein the first and second transistor networks operate as variable resistors responsive to voltages applied to the corresponding input terminals.

7. A comparator as claimed in claim 6, wherein the first current mirror has first, second and third mirrored current outputs and a control current output, the control current output coupling to a predetermined current source (44); the first mirrored current output is the first output of the first current mirror and the second mirrored current output is the second output of the first current mirror; the first transistor network has a third output terminal; and the second current mirror is a compound current mirror having a second control current input (56) and a second control current output (58), the second control current input coupling to the third mirrored current output of the first current mirror and the second control current output coupling to the third output terminal of the first transistor network.

8. A comparator as claimed in claim 7, comprising a third transistor network (76,77) disposed between the second and third mirrored current outputs of the first current mirror and the first and second control current inputs of the second current mirror, and responsive to a second predetermined voltage source (78).

9. A method of comparing first and second input voltages, comprising the steps of:

amplifying the first voltage with cascaded gain stages powered by first and second buses; and

amplifying the second voltage with cascaded gain stages powered by the first and second buses;

wherein the first and second buses are powered by respective first and second current mirrors, the first current mirror (40) having a trasnsistor (48) with an output node for coupling

* C L M S *

a first current to the first bus (32), the second current mirror (50) having a transistor (54) with a node for coupling a second current from the second bus (33), and the second current mirror (50) being responsive to an output current from the first current mirror (40) such that the second current is substantially the same as the first current; and

the amplified first and second voltages are complementary outputs indicating whether the second voltage is greater than or less than the first voltage.

10. A method as claimed in claim 9, wherein the magnification factor of one of the current mirrors is variable, and comprising the steps of:

increasing the magnification factor in response to a first predetermined voltage source;

sensing the average voltage of the amplified first and second voltages; and,

decreasing the magnification factor in response to the sensed average voltage;

such that the magnification factor settles to a value necessary for the average voltage of the amplified first and second voltages to be substantially the same as the first predetermined voltage.

11. A method as claimed in claim 10, comprising the steps of:

buffering at least one of the amplified first and second voltages with a first digital inverter having a predetermined threshold voltage; and

generating the first predetermined voltage from a second digital inverter having substantially the same threshold voltage as the first digital inverter by coupling the input of the second digital inverter to the output thereof.

Patentansprüche

1. Analog-Komparator in einer integrierten Schaltung zum Vergleich einer ersten Eingangsspannung mit einer zweiten Eingangsspannung mit einer ersten Verstärkungsstufe (22) mit einem Eingang, einem Ausgang sowie einem ersten und einem zweiten Stromversorgungsanschluß, wobei die Stromversorgungsanschlüsse an den ersten bzw. zweiten Bus und der Eingang an die erste Eingangsspannung des Komparators angekoppelt sind, und
einer zweiten Verstärkungsstufe mit einem Eingang, einem Ausgang sowie einem ersten und einem zweiten Stromversorgungsanschluß, wobei die Stromversorgungsanschlüsse an den ersten bzw. zweiten Bus und der Eingang an die zweite Eingangsspannung des Komparators angekoppelt sind,
gekennzeichnet durch
einen ersten Stromspiegel (40), der einen Transistor (48) mit einem Ausgangsknoten zur Ankopplung eines ersten Stroms an den ersten Bus (32) aufweist, und
einen zweiten Stromspiegel (50), der einen Transistor (54) mit einem Knoten zur Auskopplung eines zweiten Stroms aus dem zweiten Bus (33) aufweist, wobei
der zweite Stromspiegel (50) auf einen Ausgangsstrom des ersten Stromsspiegels (40) anspricht, derart, daß der zweite Strom im wesentlichen gleich dem ersten Strom ist.

2. Komparator nach Anspruch 1 mit weiteren Verstärkungsstufen,
wobei die erste Verstärkungsstufe die erste Stufe in einer ersten Kette (21) kaskadierter Verstärkungsstufen (22, 22) ist, und die zweite Verstärkungsstufe die erste Stufe in einer zweiten Kette (21') kaskadierter Verstärkungsstufen (22, 22) ist, jede weitere Stufe einen Eingang, einen Ausgang sowie einen ersten und einen zweiten Stromversorgungsanschluß besitzt und die Stromversorgungsanschlüsse an den ersten bzw. zweiten Bus angekoppelt sind.

3. Komparator nach Anspruch 1 oder 2
mit wenigstens einem digitalen Inverter (45), der auf wenigstens einen der Ausgänge der ersten und zweiten Verstärkungsstufe oder auf wenigstens einen der ersten Ausgänge der ersten und zweiten Kette anspricht.

4. Komparator nach Anspruch 1, 2 oder 3,
bei dem jede Verstärkungsstufe einen ersten Transistor (30) einer ersten Polarität und einen zweiten Transistor (31) einer zweiten Polarität aufweist, jeder Transistor zwei Ausgangsanschlüsse und einen Eingangsanschluß besitzt, die beiden Eingangsanschlüsse der beiden Transistoren miteinander verbunden sind und den Eingang der Verstärkungsstufe bilden, zwei sich entsprechende Ausgangsanschlüsse der beiden Transistoren miteinander verbunden sind und den Ausgang der Verstärkungsstufe bilden und die verbleibenden Ausgangsanschlüsse der beiden Transistoren den ersten bzw. zweiten Stromversorgungsanschluß der Verstärkungsstufe darstellen.

5. Komparator nach Anspruch 1, 2, 3 oder 4,
bei dem der erste Stromspiegel einen ersten und einen zweiten Ausgang besitzt, der erste Ausgang der Ausgangsknoten zur Ankopplung eines ersten Stroms an den ersten Bus ist, und der zweite Stromspiegel aufweist:

* C L M S *

einen ersten Steuerstromeingang (56), einen ersten Steuerstromausgang (58), einen gespiegelten Stromeingang (57) und einen gespiegelten Stromausgang (59), wobei der erste Steuerstromeingang mit dem zweiten Ausgang des ersten Stromspiegels verbunden und der gespiegelte Stromeingang der Knoten zur Auskopplung eines zweiten Stroms aus dem zweiten Bus (33) sind, und bei dem vorgesehen sind:
ein erster Knoten (68), der eine erste vorbestimmte Spannung führt,
ein erstes Transistornetzwerk (61, 62) mit einem ersten und einem zweiten Ausgangsanschluß sowie einem Eingangsanschluß, wobei der erste Ausgangsanschluß mit dem ersten Steuerstromausgang des zweiten Stromspiegels, der zweite Ausgangsanschluß mit einer ersten Stromversorgungsquelle und der Eingangsanschluß mit dem ersten Knoten verbunden sind, und
ein zweites Transistornetzwerk (65, 66) mit zwei Ausgangsanschlüssen und zwei Eingangsanschlüssen, wobei die Ausgangsanschlüsse zwischen dem gespiegelten Stromausgang des zweiten Stromspiegels und die erste Stromversorgungsquelle geschaltet sind und jeder Eingangsanschluß mit dem entsprechenden Ausgang der ersten und zweiten Verstärkungsstufe oder der ersten und zweiten Kette verbunden sind,
wodurch der Mittelwert der Spannungen am Ausgang der ersten und der zweiten Verstärkungsstufe oder der ersten und zweiten Kette etwa gleich der ersten vorbestimmten Spannung am ersten Knoten ist.

6. Komparator nach Anspruch 5,
bei dem das erste und das zweite Transistornetzwerk unter Ansprechen auf Spannungen, die an die entsprechenden Eingangsanschlüsse angelegt sind, als variable Widerstände betrieben werden.

7. Komparator nach Anspruch 6,
bei dem der erste Stromspiegel einen ersten, zweiten und dritten, gespiegelten Stromausgang sowie einen Steuerstromausgang besitzt, der Steuerstromausgang mit einer vorgegebenen Stromquelle (44) verbunden ist, der erste gespiegelte Stromausgang der erste Ausgang des ersten Stromspiegels und der zweite gespiegelte Stromausgang der zweite Ausgang des ersten Stromspiegels sind, das erste Transistornetzwerk einen dritten Ausgangsanschluß besitzt, der zweite Stromspiegel ein zusammengesetzter Stromspiegel mit einem zweiten Steuerstromeingang (56) und einem zweiten Steuerstromausgang (58) ist und der zweite Steuerstromeingang mit dem dritten gespiegelten Stromausgang des ersten Stromspiegels und der zweite Steuerstromausgang mit dem dritten Ausgangsanschluß des ersten Transistornetzwerks verbunden sind.

8. Komparator nach Anspruch 7
mit einem dritten Transistornetzwerk (76, 77), das zwischen den zweiten und dritten, gespiegelten Stromausgang des ersten Stromspiegels sowie den ersten und zweiten Steuerstromeingang des zweiten Stromspiegels geschaltet ist und auf eine zweite vorgegebene Spannungsquelle (78) anspricht.

9. Verfahren zum Vergleichen erster und zweiter Eingangsspannungen mit dem den Verfahrensschritten:
Verstärken der ersten Spannung durch kaskadierte Verstärkungsstufen, die durch einen ersten und einen zweiten Bus gespeist werden; und
Verstärken der zweiten Spannung durch kaskadierte Verstärkungsstufen, die durch den ersten und den zweiten Bus gespeist werden, wobei
der erste und der zweite Bus durch einen ersten bzw. zweiten Stromspiegel gespeist werden, der erste Stromspiegel (40) einen Transistor (48) mit einem Ausgangsknoten zur Ankopplung eines ersten Stroms an den ersten Bus (32) besitzt, der zweite Stromspiegel (50) einen Transistor (54) mit einem Knoten zur Auskopplung eines zweiten Stroms aus dem zweiten Bus (33) aufweist und der zweite Stromspiegel (50) auf einen Ausgangsstrom des ersten Stromspiegels (40) anspricht, derart, daß der zweite Strom im wesentlichen gleich dem ersten Strom ist, und
die verstärkte erste und zweite Spannung komplementäre Ausgangsspannungen sind, die angeben, ob die zweite Spannung größer oder kleiner als die erste Spannung ist.

10. Verfahren nach Anspruch 9,
bei dem der Verstärkungsfaktor eines der Stromspiegel variabel ist, mit den Verfahrensschritten:
Vergrößern des Verstärkungsfaktors unter Ansprechen auf eine erste vorbestimmte Spannungsquelle,
Abfühlen der mittleren Spannung der verstärkten ersten und zweiten Spannung und
verkleinern des Verstärkungsfaktors unter Ansprechen auf die abgefühlte mittlere Spannung, derart, daß der Verstärkungsfaktor sich auf einen Wert einstellt, der erforderlich ist, damit die mittlere Spannung der verstärkten ersten und zweiten Spannung im wesentlichen gleich der ersten vorbestimmten Spannung ist.

* C L M S *

11. Verfahren nach Anspruch 10, mit den Verfahrensschritten:
Puffern wenigstens einer der verstärkten ersten und zweiten Spannung durch einen ersten digitalen Inverter mit einer vorbestimmten Schwellenspannung und
Erzeugen der ersten vorbestimmten Spannung durch einen zweiten digitalen Inverter mit im wesentlichen der gleichen Schwellenspannung wie der erste digitale Inverter durch Ankoppeln des Eingangs des zweiten digitalen Inverters mit dessen Ausgang.

Revendications

1. Un comparateur analogique formé sur un circuit intégré pour comparer les tensions présentes sur une première entrée de tension et sur une seconde entrée de tension, comprenant
un premier étage de gain (22) ayant une entrée, une sortie et des première et seconde bornes d'alimentation, les bornes d'alimentation correspondantes étant connectées à des premier et second bus, et l'entrée étant connectée à la première entrée de tension du comparateur ; et
un second étage de gain ayant une entrée, une sortie et des première et seconde bornes d'alimentation, les bornes d'alimentation correspondantes étant connectées aux premier et second bus, et l'entrée étant connectée à la seconde entrée de tension du comparateur ;
CARACTERISE PAR
un premier miroir de courant (40) ayant un transistor (48) avec un noeud de sortie pour appliquer un premier courant au premier bus (32) ; et
un second miroir de courant (50) ayant un transistor (54) avec un noeud pour appliquer un second courant provenant du second bus (33) ;
le second miroir de courant (50) réagissant à un courant de sortie du premier miroir de courant (40), de façon que le second courant soit pratiquement le même que le premier courant.

2. Un comparateur selon la revendication 1, comprenant des étages de gain supplémentaires, dans une configuration dans laquelle le premier étage de gain est le premier étage dans une première chaîne (21) d'étages de gain (22, 22) connectés en cascade, et le second étage de gain est le premier étage de gain dans une seconde chaîne (21') d'étages de gain (22, 22) connectés en cascade, chaque étage supplémentaire ayant une entrée, une sortie et des première et seconde bornes d'alimentation, les bornes d'alimentation correspondantes étant connectées aux premier et second bus.

3. Un comparateur selon la revendication 1 ou 2, comprenant au moins un inverseur numérique (45) qui, selon le cas, fonctionne sous la dépendance de l'une au moins des sorties des premier et second étages de gain, ou de l'une au moins des sorties des première et seconde chaînes.

4. Un comparateur selon la revendication 1, 2 ou 3, dans lequel chaque étage de gain comprend un premier transistor (30) d'une première polarité et un second transistor (31) d'une seconde polarité, chaque transistor ayant deux bornes de sortie et une borne d'entrée, les bornes d'entrée des deux transistors étant connectées ensemble pour former l'entrée de l'étage de gain, deux bornes de sortie correspondantes des deux transistors étant connectées ensemble pour former la sortie de l'étage de gain, et les bornes de sortie restantes des deux transistors formant les première et seconde bornes d'alimentation correspondantes de l'étage de gain.

5. Un comparateur selon la revendication 1, 2, 3 ou 4, dans lequel le premier miroir de courant comporte des première et seconde sorties, la première sortie étant le noeud de sortie pour l'application d'un premier courant au premier bus, et le second miroir de courant comprend
une première entrée de courant de commande (56), une première sortie de courant de commande (58), une entrée de courant miroir (57) et une sortie de courant miroir (59), la première entrée de courant de commande étant connectée à la seconde sortie du premier miroir de courant, et l'entrée de courant miroir étant le noeud pour l'application d'un second courant à partir du second bus (33) ; et dans lequel il existe
un premier noeud (68) sur lequel une première tension prédéterminée est présente ;
un premier réseau de transistors (61, 62) ayant des première et seconde bornes de sortie et une borne d'entrée, la première borne de sortie étant connectée à la première sortie de courant de commande du second miroir de courant, la seconde borne de sortie étant connectée à une première source d'alimentation et la borne d'entrée étant connectée au premier noeud ; et
un second réseau de transistors (65, 66) ayant deux bornes de sortie et deux bornes d'entrée, les bornes de sortie correspondantes étant connectées entre la sortie de courant miroir du second miroir de courant et la première source d'alimentation, chaque borne d'entrée étant connectée à la sortie correspondante du premier et du second étage de gain, ou de la première chaîne et de la seconde chaîne, selon le cas ;
grâce à quoi la moyenne des tensions sur les sorties des premier et second étages de gain,

* C L M S *

ou des première et seconde chaînes, selon le cas, est approximativement égale à la première tension prédéterminée sur le premier noeud.

6. Un comparateur selon la revendication 5, dans lequel les premier et second réseaux de transistors fonctionnent à la manière de résistances variables qui réagissent à des tensions appliquées sur les bornes d'entrée correspondantes.

7. Un comparateur selon la revendication 6, dans lequel le premier miroir de courant comporte des première, seconde et troisième sorties de courant miroir et une sortie de courant de commande, la sortie de courant de commande étant connectée à une source de courant prédéterminée (44) ; la première sortie de courant miroir est la première sortie du premier miroir de courant et la seconde sortie de courant miroir est la seconde sortie du premier miroir de courant ; le premier réseau de transistors comporte une troisième borne de sortie ; et le second miroir de courant est un miroir de courant combiné ayant une seconde entrée de courant de commande (56) et une seconde sortie de courant de commande (58), la seconde entrée de courant de commande étant connectée à la troisième sortie de courant miroir du premier miroir de courant et la seconde sortie de courant de commande étant connectée à la troisième borne de sortie du premier réseau de transistors.

8. Un comparateur selon la revendication 7, comprenant un troisième réseau de transistors (76, 77) disposé entre les seconde et troisième sorties de courant miroir du premier miroir de courant et les première et seconde entrées de courant de commande du second miroir de courant, et fonctionnant sous la dépendance d'une seconde source de tension prédéterminée (78).

9. Un procédé de comparaison d'une première tension d'entrée et d'une seconde tension d'entrée, comprenant les étapes suivantes:

on amplifie la première tension avec des étages de gain connectés en cascade, alimentés par des premier et second bus ; et

on amplifie la seconde tension avec des étages de gain connectés en cascade, alimentés par les premier et second bus ;

dans lequel les premier et second bus sont alimentés par des premier et second miroirs de courant respectifs, le premier miroir de courant (40) ayant un transistor (48) avec un noeud de sortie pour appliquer un premier courant au premier bus (32), le second miroir de courant (50) ayant un transistor (54) avec un noeud pour appliquer un second courant à partir du premier bus (33), et le second miroir de courant (50) réagissant à un courant de sortie qui provient du premier miroir de courant (40), de façon que le second courant soit pratiquement identique au premier courant ; et

les première et seconde tensions amplifiées sont des tensions de sortie complémentaires qui indiquent si la seconde tension est supérieure ou inférieure à la première tension.

10. Un procédé selon la revendication 9, dans lequel le facteur d'amplification de l'un des miroirs de courant est variable, et le procédé comprend les étapes suivantes :

on augmente le facteur d'amplification sous la dépendance d'une première source de tension prédéterminée ;

on détecte la tension moyenne des première et seconde tensions amplifiées ; et

on diminue le facteur d'amplification sous la dépendance de la tension moyenne détectée ;

de façon que le facteur d'amplification se stabilise à une valeur nécessaire pour que la tension moyenne des première et seconde tensions amplifiées soit pratiquement égale à la première tension prédéterminée.

11. Un procédé selon la revendication 10, comprenant les étapes suivantes :

on applique une opération d'amplification-séparation à l'une au moins des première et seconde tensions amplifiées, avec un premier inverseur numérique ayant une tension de seuil prédéterminée ; et

on génère la première tension prédéterminée à partir d'un second inverseur numérique ayant pratiquement la même tension de seuil que le premier inverseur numérique, en connectant l'entrée du second inverseur numérique à sa sortie.

* C L M S *