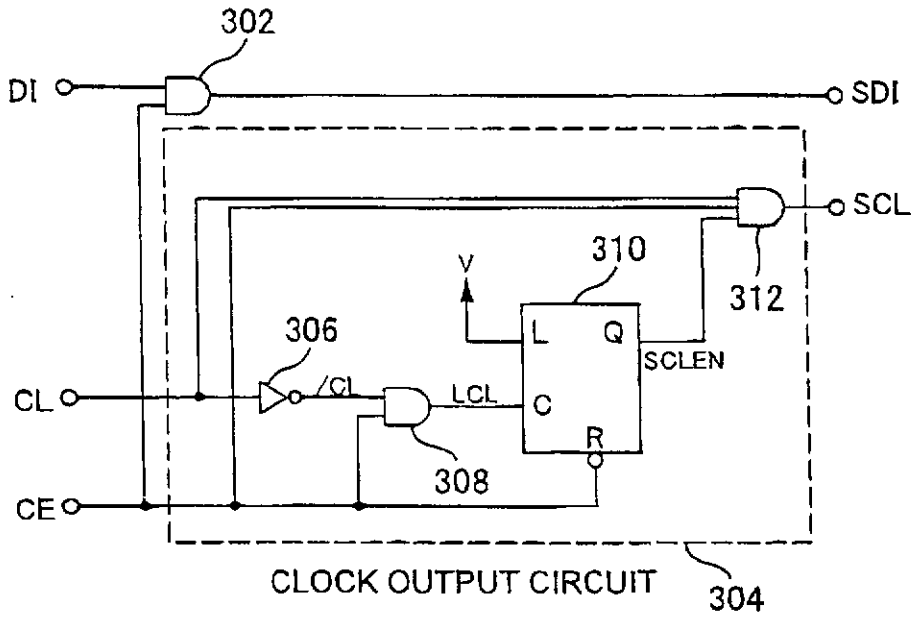

302
DI
SDI
SCL
310
V
312
306
L
Q
SCLEN
CL
/CL
LCL
C
R
308
CE
CLOCK OUTPUT CIRCUIT
304

FIG.1

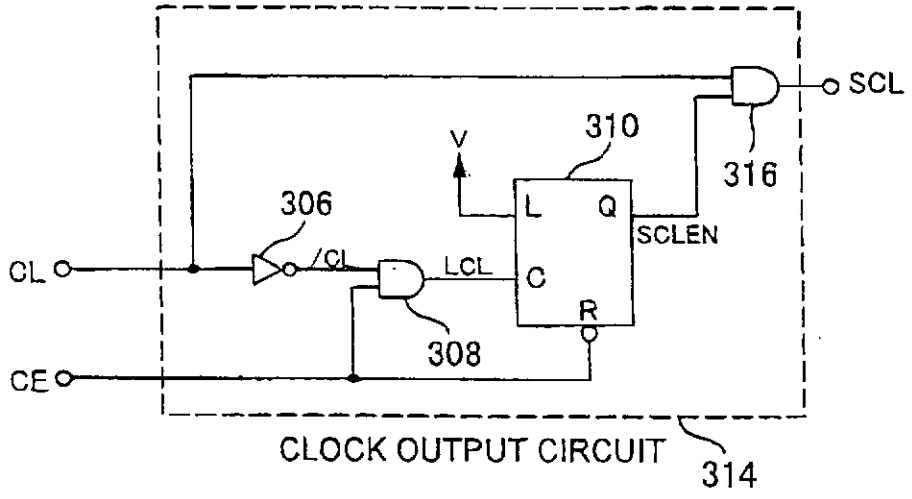

SCL
310
V
316
306
L
Q
SCLEN
CL
/CL
LCL
C
R
308
CE
CLOCK OUTPUT CIRCUIT
314

FIG.2

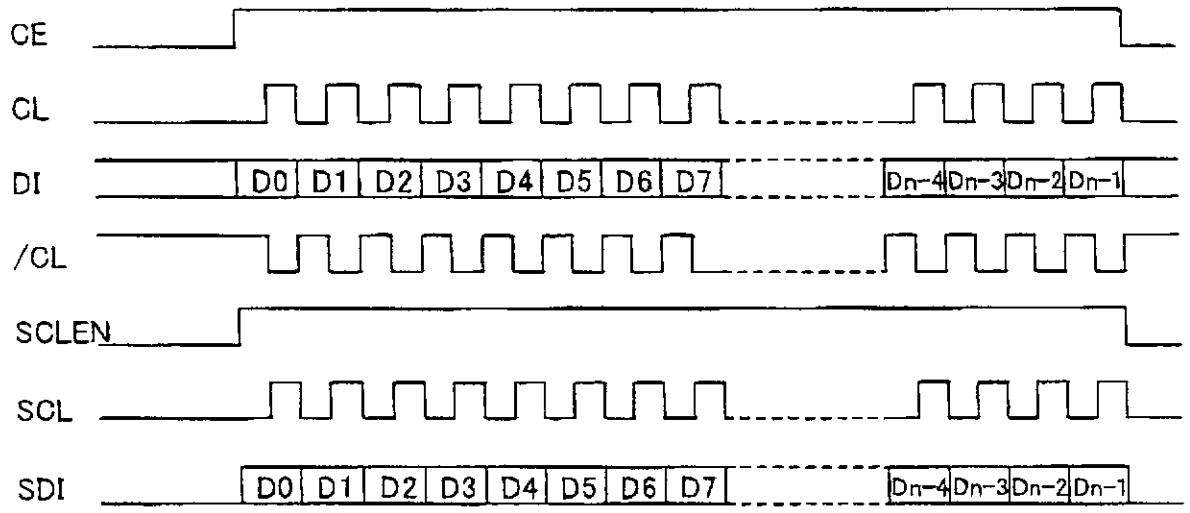

CE
CL
DI
D0 D1 D2 D3 D4 D5 D6 D7
Dn-4 Dn-3 Dn-2 Dn-1
/CL
SCLEN
SCL
SDI
D0 D1 D2 D3 D4 D5 D6 D7
Dn-4 Dn-3 Dn-2 Dn-1

FIG.3

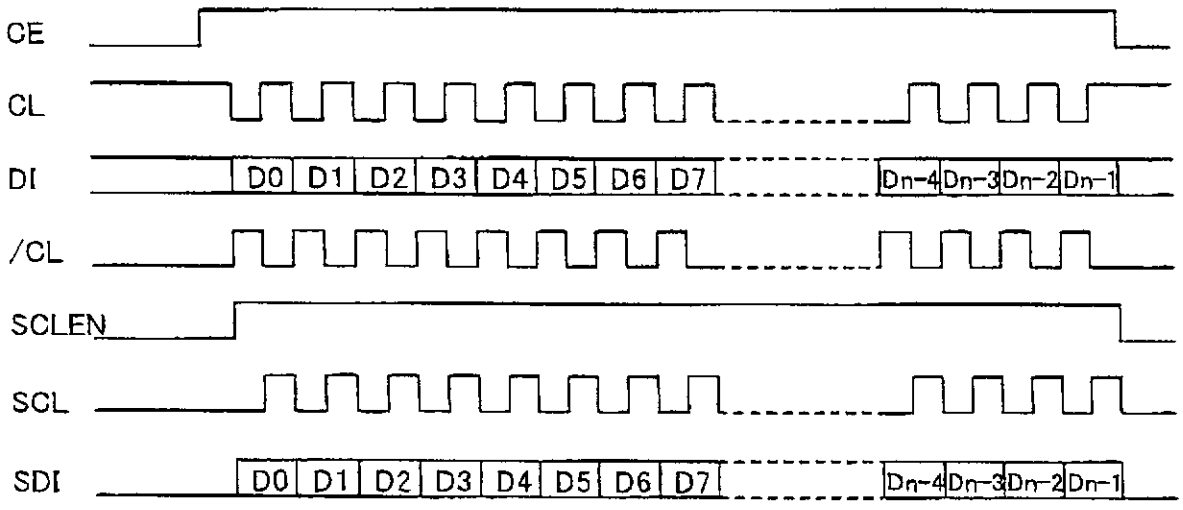

CE
CL
DI
D0 D1 D2 D3 D4 D5 D6 D7
Dn-4 Dn-3 Dn-2 Dn-1
/CL
SCLEN
SCL
SDI
D0 D1 D2 D3 D4 D5 D6 D7
Dn-4 Dn-3 Dn-2 Dn-1

FIG.4

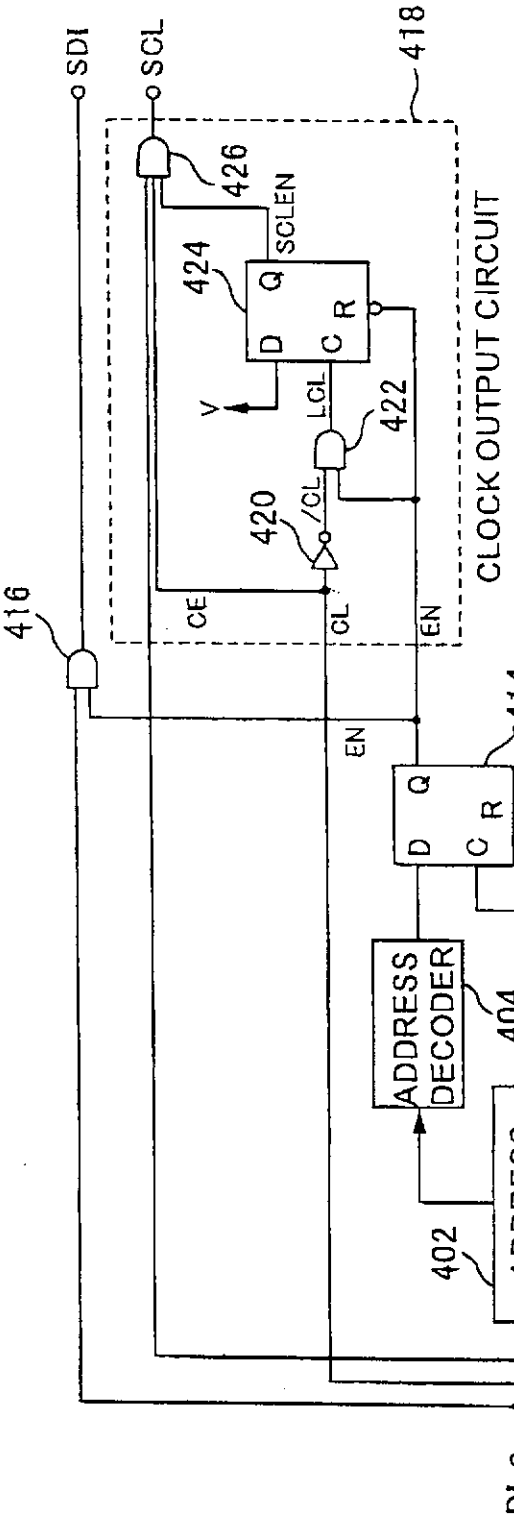

SDI
SCL
418
426
SCLEN
424
Q
D
C
R
V
LGL
422
/CL
420
CE
CL
EN
CLOCK OUTPUT CIRCUIT
416
EN
414
Q
D
C
R
ADDRESS DECODER
404
410
412
408
ADDRESS REGISTER
402
DELAY
406
DI
CL
CE

FIG.5

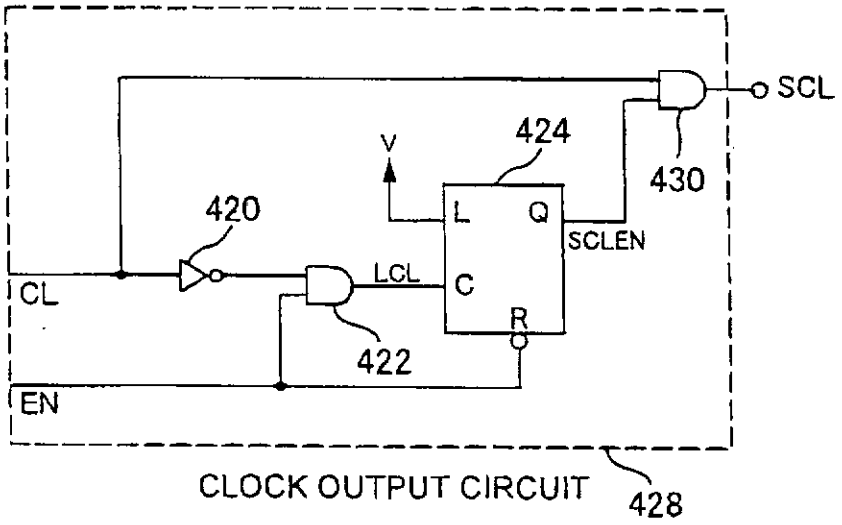

SCL
V
424
430
420
L
Q
SCLEN
LCL
C
CL
R
422
EN
CLOCK OUTPUT CIRCUIT
428

FIG.6

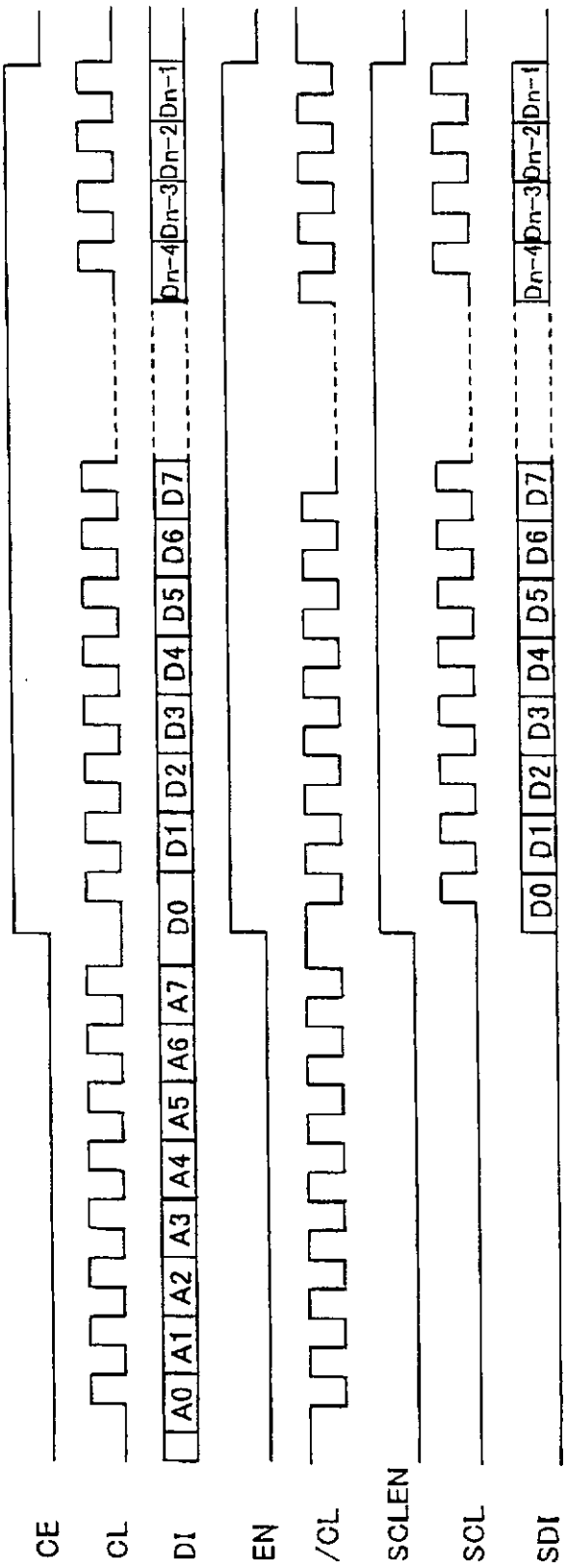

CE
CL
DI
EN
/CL
SCLEN
SCL
SDI
A0 A1 A2 A3 A4 A5 A6 A7 D0 D1 D2 D3 D4 D5 D6 D7 Dn-4 Dn-3 Dn-2 Dn-1
D0 D1 D2 D3 D4 D5 D6 D7 Dn-4 Dn-3 Dn-2 Dn-1

FIG.7

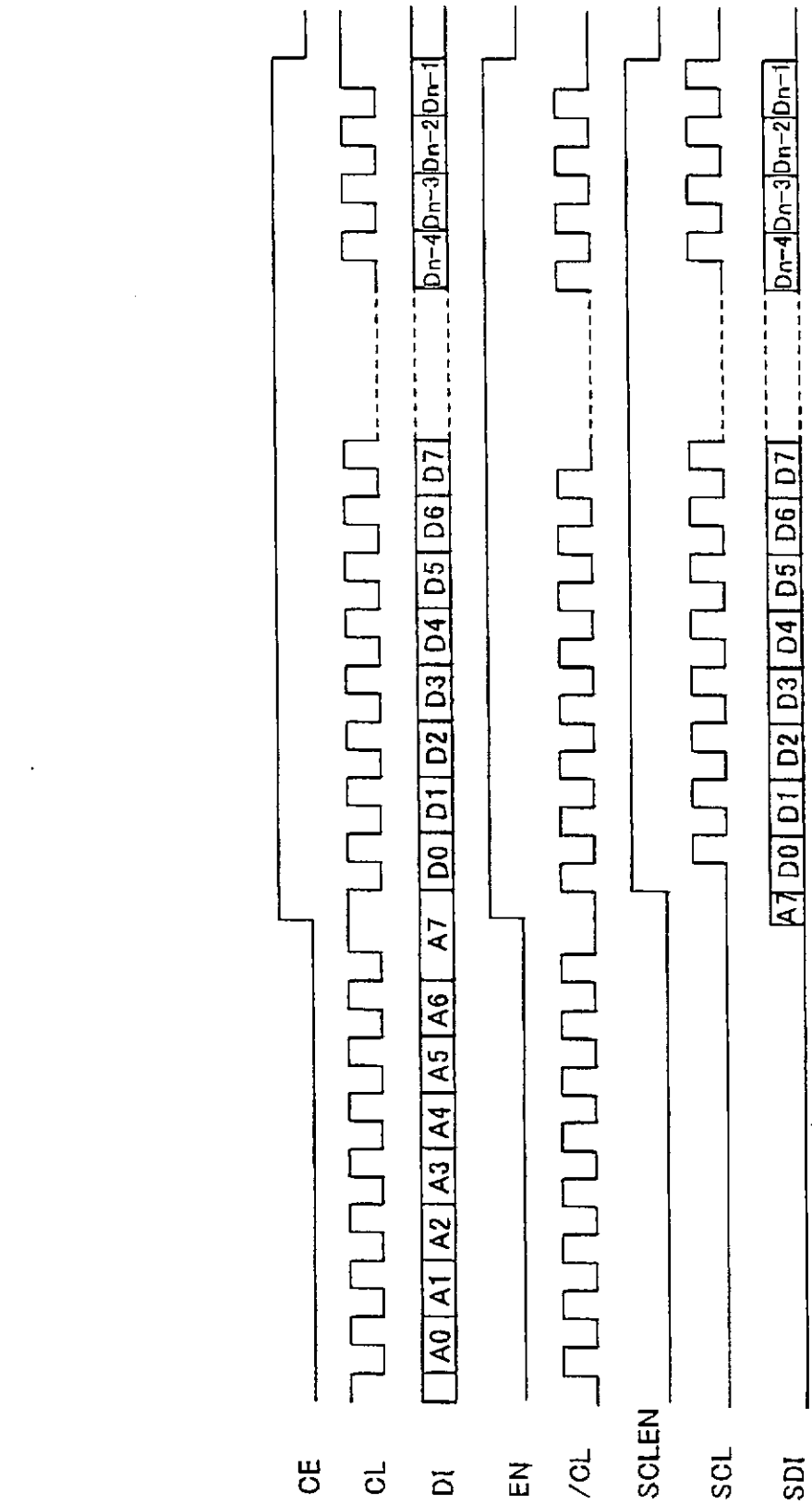

CE
CL
DI
EN
/CL
SCLEN
SCL
SDI
A0 A1 A2 A3 A4 A5 A6 A7 D0 D1 D2 D3 D4 D5 D6 D7
Dn-4 Dn-3 Dn-2 Dn-1
A7 D0 D1 D2 D3 D4 D5 D6 D7
Dn-4 Dn-3 Dn-2 Dn-1

FIG.8

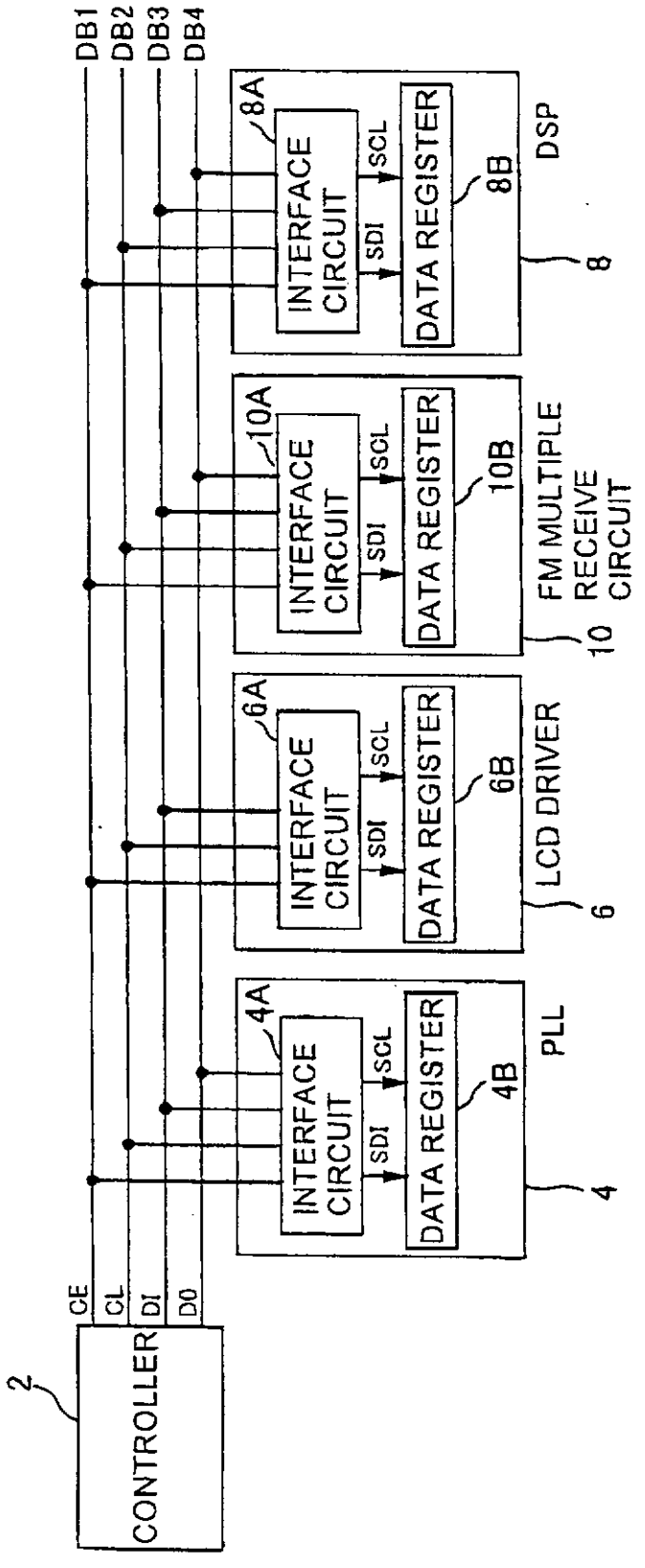

DB1
DB2
DB3
DB4
CE
CL
DI
DO
2
CONTROLLER
4A
INTERFACE CIRCUIT
SDI
SCL
DATA REGISTER
4B
PLL
4
6A
INTERFACE CIRCUIT
SDI
SCL
DATA REGISTER
6B
LCD DRIVER
6
10A
INTERFACE CIRCUIT
SDI
SCL
DATA REGISTER
10B
FM MULTIPLE RECEIVE CIRCUIT
10
8A
INTERFACE CIRCUIT
SDI
SCL
DATA REGISTER
8B
DSP
8

FIG.9

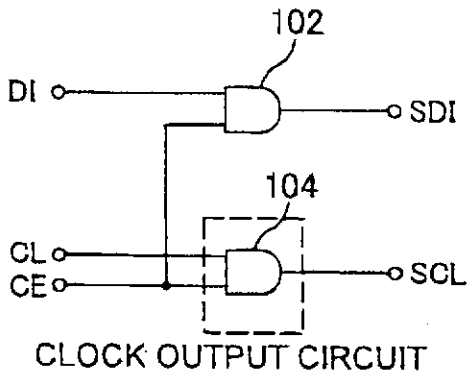


FIG.10

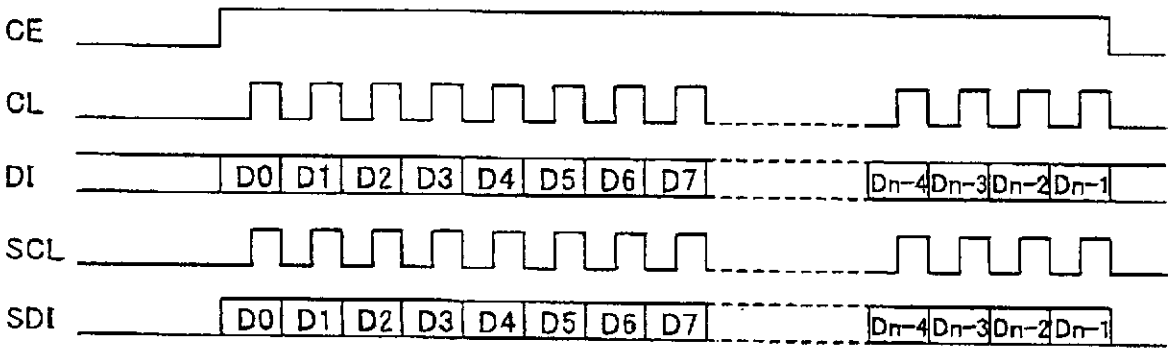


FIG.11

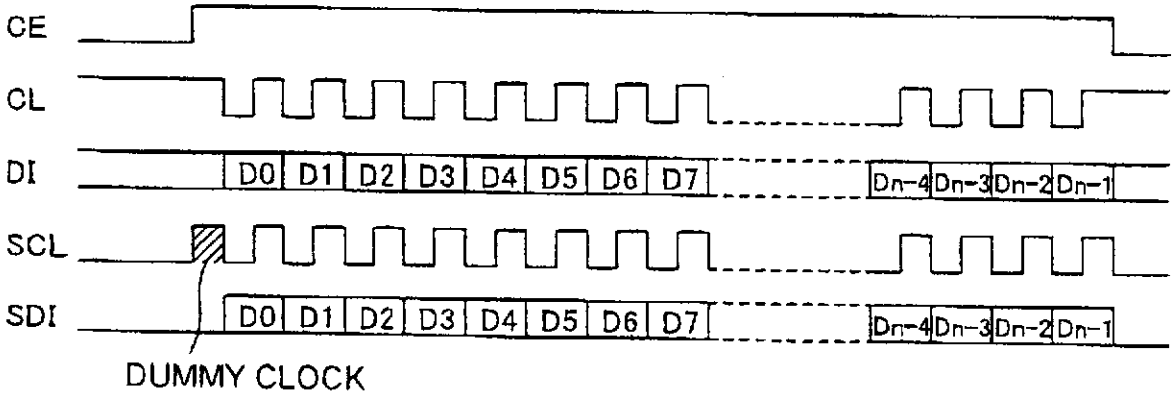


FIG.12

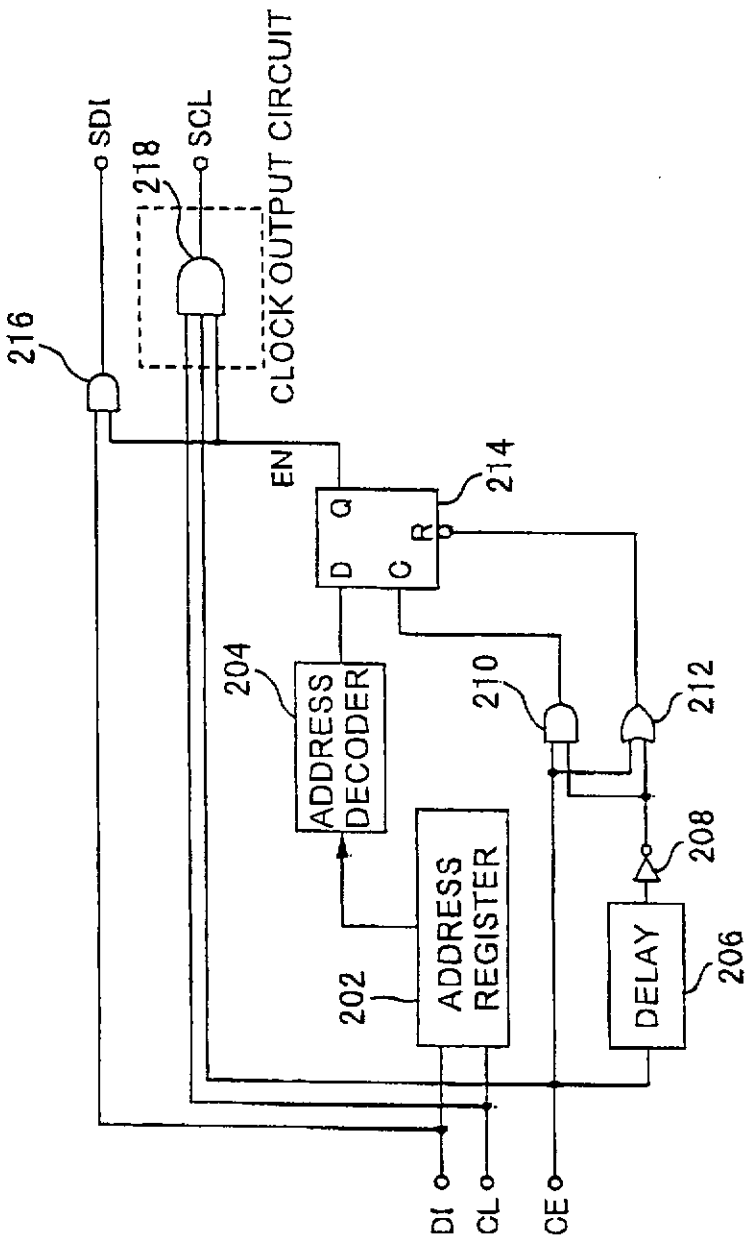

SDI
SCL
218
CLOCK OUTPUT CIRCUIT
216
EN
D
Q
C
R
214
204
ADDRESS DECODER
210
212
208
ADDRESS REGISTER
202
DELAY
206
DI
CL
CE

FIG.13

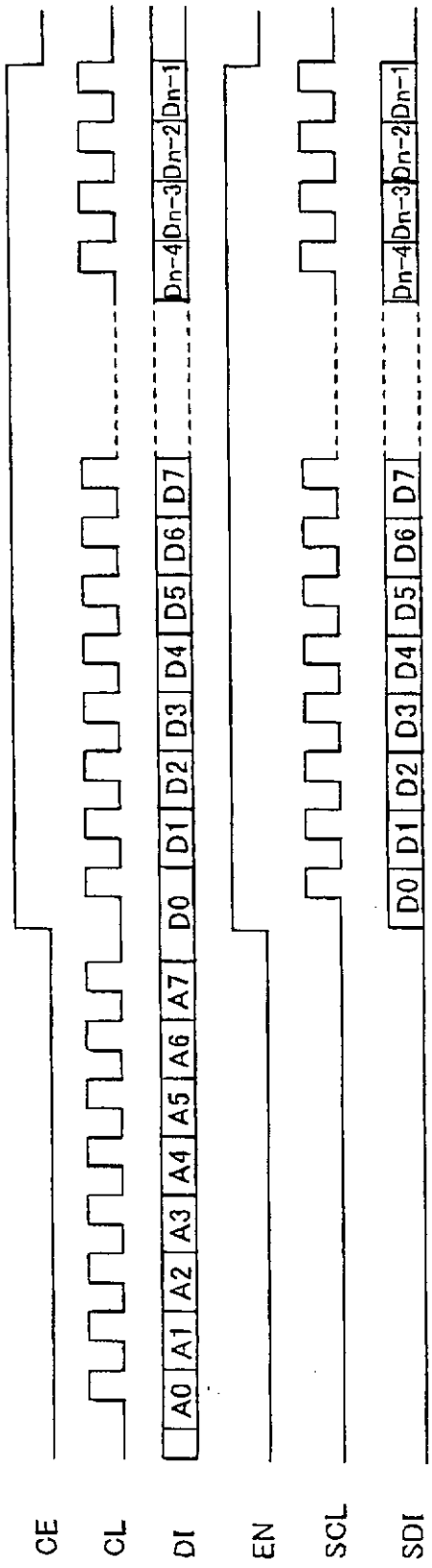

CE
CL
DI
EN
SCL
SDI
A0 A1 A2 A3 A4 A5 A6 A7 D0 D1 D2 D3 D4 D5 D6 D7 Dn-4 Dn-3 Dn-2 Dn-1
D0 D1 D2 D3 D4 D5 D6 D7 Dn-4 Dn-3 Dn-2 Dn-1

FIG.14

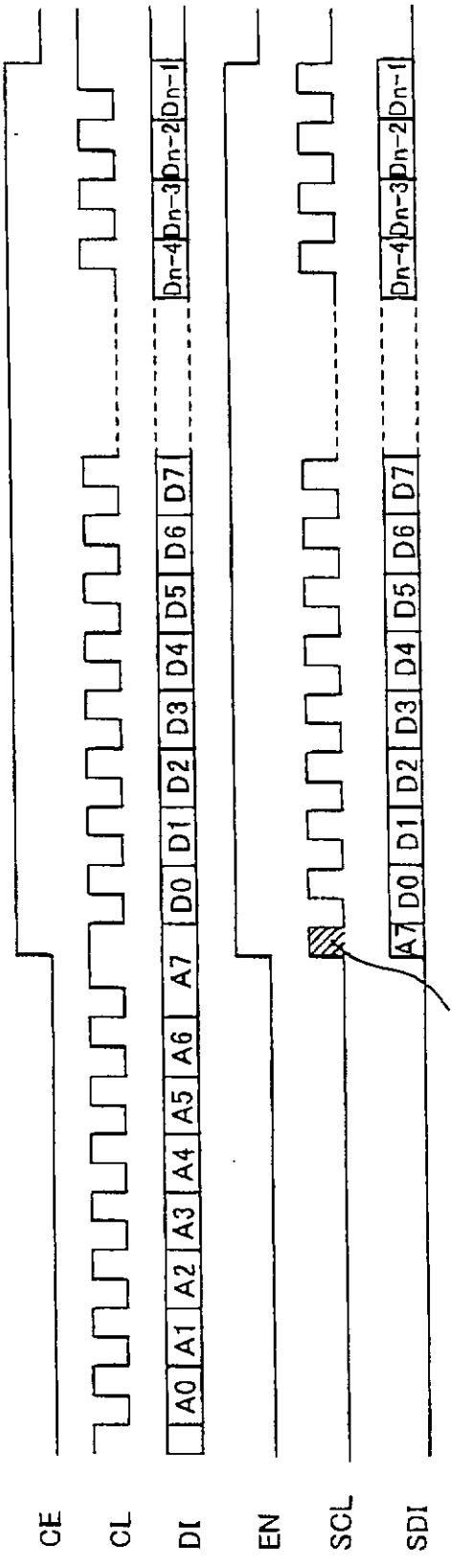

CE
CL
DI
EN
SCL
SDI
A0 A1 A2 A3 A4 A5 A6 A7 D0 D1 D2 D3 D4 D5 D6 D7
Dn-4 Dn-3 Dn-2 Dn-1
A7 D0 D1 D2 D3 D4 D5 D6 D7
Dn-4 Dn-3 Dn-2 Dn-1
DUMMY CLOCK

FIG.15