CLAIMS

1. An inspection system that inspects gaming chips, the inspection system comprising:

an area in which can be placed, in a stacked manner, a plurality of gaming chips that include (a) first gaming chip information and (b) second gaming chip information, the second gaming chip information provided in an optically readable form on respective side surfaces of the gaming chips; and

an inspecting device configured to inspect the gaming chips placed in the area, the inspecting device includes:

a first reader configured to acquire the first gaming chip information of all of the gaming chips placed in the area;

a second reader configured to optically read the side surfaces of the gaming chips placed in the area; and

a processor configured to determine, respectively for each gaming chip of the plurality of gaming chips placed in the area, whether there is a discrepancy between (a) the respective first gaming chip information acquired by the first reader for the respective gaming chip and (b) the respective second gaming chip information acquired by the second reader for the respective second gaming chip to thereby determine whether the gaming chips placed in the area are in a pass state or a fail state.

2. The inspection system according to claim 1, wherein the first gaming chip information and the second gaming chip information of respective ones of the gaming chips include common information portions for inclusion of respective common information of the respective gaming chips, and the processor is configured to determine that the plurality of the gaming chips placed in the area are in the fail state when the common information portions of a plurality of pieces of the first gaming chip information acquired by the first reader do not coincide with corresponding common information portions of a plurality of pieces of the second gaming chip information acquired by the second reader.

3. The inspection system according to claim 1, wherein one or both of the first gaming chip information and the second gaming chip information includes individual identification information individually identifying respective ones of the gaming chips.

4. The inspection system according to claim 3, wherein the processor is configured to determine that the plurality of the gaming chips placed in the area are determined to be in the fail state when the individual identification information of a plurality of pieces of first gaming chip information acquired by the first reader does not coincide with the individual identification information of a plurality of pieces of second gaming chip information acquired by the second reader.

5. The inspection system according to claim 1, wherein the second gaming chip information includes information indicated by designated colors that indicate respective values of the gaming chips.

6. The inspection system according to claim 1, further comprising:

a storage unit configured to store respective individual identification information of at least the first or second gaming chip information of the gaming chips authorized to be placed in the area, and

wherein the processor is configured to determine that the plurality of gaming chips placed in the area in the fail state when a plurality of pieces of individual identification information of the respective first gaming chip information of the respective gaming chips acquired by the first reader or a plurality of pieces of individual identification information of the respective second gaming chip information of the respective gaming chips acquired by the second reader do not coincide with a plurality of pieces of individual identification information of the first and second gaming chip information stored in the storage unit.

7. The inspection system according to claim 1, wherein the processor is configured to determine that a plurality of the gaming chips placed in the area are in the fail state when a number of pieces of the first gaming chip information acquired by the first reader or a number of pieces of the second gaming chip information acquired by the second reader is not a predetermined number.

8. The inspection system according to claim 1, wherein:

the gaming chips include color information indicating respective values of the gaming chips as the second gaming chip information, and include respective value information identifying respective values of

the gaming chips as the first gaming chip information; and

the processor is configured to determine that a plurality of the gaming chips placed in the area are in the fail state when the color information does not coincide with the value information of the first gaming chip information.

9. The inspection system according to claim 8, wherein:

the second gaming chip information further includes respective value information of the respective gaming chips in addition to the color information; and

the inspection system further includes a display via which the inspection system is configured to display a result of the determination that distinguishes between those of the gaming chips that are in the pass state and those of the gaming chips that are in the fail state so that a respective one of the gaming chips that is in the fail state can be identified when a value of the respective gaming chip indicated by the color information in the second gaming chip information of the respective gaming chip does not coincide with the value information of the second gaming chip information, the value information of the first gaming chip information of the respective gaming chip, or a combination thereof.

10. The inspection system according to claim 8, wherein:

the second gaming chip information further includes respective value information of the respective gaming chips in addition to the color information; and

the processor is configured to determine that a plurality of the gaming chips placed in the area are in the fail state when a value of a respective one of the gaming chips indicated by the color information in the second gaming chip information of the respective gaming chip does not coincide with the value information of the second gaming chip information, the value information of the first gaming chip information, or a combination thereof.

11. The inspection system according to claim 10, wherein the processor is configured to determine a respective number of the gaming chips placed in the area for each of the values or a total amount of the values of all of the gaming chips based on the color information or the value information of the first gaming chip information or the second gaming chip information.

12. The inspection system according to claim 10, wherein the processor is configured to determine that the plurality of the gaming chips placed in the area are in the fail state when the color information does not coincide with (a) the value information of the first gaming chip information or the second gaming chip information, (b) common information, or (c) individual identification information of the first gaming chip information or the second gaming chip information.

13. The inspection system according to claim 1, wherein the first gaming chip information is included in respective radio tags of the gaming chips.

14. The inspection system according to claim 1, wherein

the first gaming chip information, the second gaming chip information, or both the first and second gaming chip information includes group information indicating respective groups to which respective ones of the gaming chips belong, and the groups are classified in accordance with respective values of the gaming chips, manufacturing times, manufacturers, use game halls, or a combination thereof.

15. The inspection system according to claim 1, wherein:

the second gaming chip information includes respective designated colors indicating respective values of the gaming chips on respective side surfaces of the gaming chips; and

the second reader comprises:

a camera configured to capture an image of the side surfaces of the gaming chips placed in the area; and

a processor that is configured to:

analyze the image captured by the camera;

identify and output the respective designated colors of each of the plurality of gaming chips based on the analysis; and

identify and output the respective values of the plurality of gaming chips in accordance with the identified designated colors.

16. The inspection system according to claim 15, wherein the designated colors are respectively interposed, in a thickness direction of the side surfaces of the gaming chips, between common colors which are commonly assigned to gaming chips having different values.

17. The inspection system according to claim 1, wherein:

the second gaming chip information is notation information inscribed on the side surfaces to be optically readable; and

the second reader comprises:

a camera that is configured to capture an image of the side surfaces of the gaming chips stacked and placed in the area; and

a processor configured to:

analyze the image captured by the camera;

based on the analysis, identify the respective notation information of each of the gaming chips; and

identify and output the second gaming chip information of each of the gaming chips in accordance with the identified notation information.

18. The inspection system according to claim 17, wherein:

the notation information is inscribed using infrared reaction ink that emits in response to infrared rays or using infrared absorption ink that absorbs infrared rays; and

the camera includes an infrared camera.

19. The inspection system according to claim 17, wherein:

the notation information is inscribed using ink that emits light in response to ultraviolet rays; and

the inspecting device further includes an ultraviolet irradiator that is configured to irradiate the side surfaces of the gaming chips with ultraviolet rays.

20. The inspection system according to claim 1, wherein:

the area is a case that has a seal which is broken when the case is opened to allow the gaming chips to be withdrawn from the case;

the inspecting device further comprises a sensor that is configured to detect whether the seal is unbroken; and

the processor is configured to determine that the gaming chips contained in the case are in the fail state when the unbroken seal is not detected by the sensor.

21. The inspection system according to claim 1, wherein the processor is configured to determine that the plurality of gaming chips placed in the area are in the fail state when a number of the acquired first gaming chip information does not coincide with a number of the acquired second gaming chip information.

22. The inspection system according to claim 1, wherein the processor is configured to determine that the plurality of gaming chips placed in the area are in the fail state when a number of the acquired first gaming chip information for a respective value does not coincide with a number of the acquired second gaming chip information for the respective value.

23. The inspection system according to claim 1, further comprising a display via which the inspection system is configured to display a result of the determination that distinguishes between those of the gaming chips that in the pass state and those of the gaming chips that are in the fail state so that the gaming chips for which there is a lack of correspondence between the respective acquired first

gaming chip information and the respective acquired second gaming chip information are identifiable.

24. The inspection system according to claim 1, wherein:

both of the first gaming chip information and the second gaming chip information includes individual identification information individually identifying respective ones of the gaming chips; and

the inspection system further comprises a display via which the inspection system is configured to display a result of the determination that distinguishes between those of the gaming chips that in the pass state and those of the gaming chips that are in the fail state so that the gaming chips in the fail state are identifiable when a plurality of piece of individual identification information of a plurality of pieces of the first gaming chip information acquired by the first reader and a plurality of piece of individual identification information of a plurality of pieces of the second gaming chip information acquired by the second reader do not coincide with each other.

25. The inspection system according to claim 1, further comprising:

a storage unit, wherein the storage unit is configured to store respective individual identification information of at least the first or the second gaming chip information of the gaming chips authorized to be placed in the area, and

wherein the processor is configured to determine that the plurality of gaming chips placed in the area are in the fail state when a plurality of pieces of individual identification information of a plurality of pieces of the first gaming chip information acquired by the first reader or a plurality of piece of individual identification information of a plurality of pieces of the second gaming chip information acquired by the second reader do not coincide with a plurality of pieces of individual identification information of the first or the second gaming chip information stored in the storage unit.

26. The inspection system according to claim 1, further comprising:

a storage unit, wherein the storage unit is configured to store a correspondence relation between the first gaming chip information and the second gaming chip information, and wherein the processor is configured to determine that the plurality of gaming chips placed in the area are in the fail state when a plurality of pieces of the first gaming chip information acquired by the first reader and a plurality of pieces of the second gaming chip information acquired by the second reader do not coincide with the correspondence relation stored in the storage unit.

27. The inspection system according to claim 1, further comprising:

a display; and

a storage unit;

wherein:

both of the first gaming chip information and the second gaming chip information include individual identification information individually identifying respective ones of the gaming chips;

the storage unit is configured to store respective individual identification information of at least the first or the second gaming chip information of the gaming chips authorized be placed in the area; and

the inspection system is configured to display a result of the determination that distinguishes between those of the gaming chips that are in the pass state and those of the gaming chips that are in the fail state so that the gaming chips that are in the fail state can be identified when a plurality of pieces of individual identification information of the plurality of pieces of the first gaming chip information acquired by the first reader or a plurality of pieces of individual identification information of the plurality of pieces of the second gaming chip information acquired by the second reader does not coincide with the individual identification information of the first or the second gaming chip information stored in the storage unit.

28. The inspection system according to claim 1, further comprising:

a storage unit configured to store a correspondence relation between the first gaming chip information

and the second gaming chip information; and

a display via which the inspection system is configured to display a result of the determination that distinguishes between those of the gaming chips that are in the pass state and those of the gaming chips that are in the fail state so that the gaming chips in the fail state can be identified when a plurality of pieces of the first gaming chip information acquired by the first reader and a plurality of pieces of the second gaming chip information acquired by the second reader do not coincide with the correspondence relation stored in the storage unit.

29. The inspection system according to claim 1, wherein:

the gaming chips include color information indicating respective values of the gaming chips as the second gaming chip information and include respective value information identifying respective values of the gaming chips as the first gaming chip information; and

the inspection system further comprises a display via which the inspection system is configured to display a result of the determination that distinguishes between the gaming chips in the pass state and the gaming chips in the fail state so that the gaming chips in the fail state can be identified when the respective color information of the gaming chips in the fail state does not coincide with the respective value information of the first gaming chip information of the gaming chips in the fail state.

30. The inspection system according to claim 1, wherein:

the area is a case that has a light transmitting part through which light transmits; and

the second reader is configured to optically read the surface of the gaming chips contained in the case through the light transmitting part.

31. The inspection system according to claim 30, wherein the light transmitting part is made of transparent material.

32. The inspection system according to claim 1, wherein:

the area is a case; and

the inspecting device further includes a receiving portion in which the case is received.

33. The inspection system according to claim 1, wherein the area is a portable case.

34. The inspection system according to claim 1, wherein the area comprises a two-tiered chip float or chip tray configured to hold the gaming chips at a game table.