# PROCESS OF TREATING DEFECTS DURING THE BONDING OF WAFERS

## DESCRIPTION

### TECHNICAL FIELD AND PRIOR ART

The invention concerns the field of microelectronics and techniques used in this field to perform a processing of wafers that may notably have components on their surface.

In this field of microelectronics, it is in particular important to be able to perform transfers of thin layers containing circuits. These transfers of thin layers enables notably to transfer the circuits onto wafers different than those that were used to produce them.

For example, these wafers may be semiconductor wafers containing electronic components or wafers having properties different from the substrates that were used to produce the components.

In some cases, it is sought to have access to the rear face of the components, the face that rests on a substrate on which or from which they may have been prepared.

A known technique for doing this is illustrated in figures 1A–1D. It consist of bonding a first wafer 2, on which a treated thin layer 5 is formed, on the front face with a second wafer 8, and thinning or removing its substrate 1 on the rear face.

The wafer 2, or rather its treated thin layer 5, contains in particular some circuits 3, 6 (figure 1A).

In preparation for a bonding by molecular adhesion with this second wafer 8, in general a layer 4 of bonding material is deposited on the front face of the thin layer 5 in order to be levelled off and compatible with direct bonding (figure 1A). Lacking such a levelled off layer 4, non-bonded zones (corresponding to zones with a topology on the surface of the circuit) may be present at the bonding interface and interfere with the transfer of the thin layer 5.

The second wafer 8 for its part is surface oxidised (figure 1B). The reference 10 designates the surface layer of oxide.

The bonding step can then take place, after the adhesive layer 4 has been levelled off (figure 1C).

Finally, the part 1 of the first wafer 2 not containing the treated zone is thinned or removed (figure 1D), for example by planing, or by chemical etching (dry or wet). The surface 5' of the wafer 5 containing the circuits 3, 6 is then buried at the bonding interface formed by the bonding layer 4.

In some cases, the thin layer 5 is a layer comprising some components 3, 6, which may be very elaborate, and may therefore be of a very high cost, and it is not acceptable not to be able to perform the transfer step onto the second wafer 8 with an efficiency that is equal to, or very close to, 100%.

More generally, the simple fact that there is a bonding defect vertically in line with a chip or a component makes it unusable. The defects may be particles that are present on the surface and difficult to clean or defects buried in the oxide layer.

The presence of defects on the levelled off surface therefore causes bonding defects, which greatly affect the yield by making some chips unusable.

For example, after the step illustrated in figure 1D, a cutting into individual circuits may be performed, along cutting lines such as those indicated by the arrows 11, 13 (figure 1D). If defects or voids are present at the bonding interface between the layer 4 and the substrate 8, this may make the whole of the wafer unusable.

The same problem may appear in the case of a surface that is structured but homogeneous (ie: not comprising multiple layers and materials of different natures), for example the surface of at least part of the thin layer 5 without components 3, 6, this surface having however a topology with defects or voids during bonding.

Furthermore, the problem is posed of finding a novel process to ease the carrying out of the transfer of a layer, such as the thin layer 5, which may contain some circuits or components and having a surface topology, on a support such as the second wafer 8.

**DISCLOSURE OF THE INVENTION**

The inventors have found that, during an operation of polishing the layer of adhesion material 4 (figure 1B), difficulties may present themselves because of the topology that the surface 4' of this layer reproduces according to the initial topology of the thin layer 5.

This surface topology of the thin layer 5 results from differences in level e between the elevated zones and the low zones of this surface, which may correspond to several levels, at different altitudes with respect to an axis perpendicular to the plane of the thin layer 5, for example to several levels of metal in different zones or, more generally, to different stacks of materials in different zones. These differences in level may be as much as around several µm, and are for example between 500 nm, or 1 µm, and 5 µm, or less than 10 µm.

The topology of the surface 4' of the adhesive layer 4 is not visible in figures 1A and 1B but is shown in figure 2A.

Having regard to the considerable topologies indicated above, which may be as much as 5 µm or 10 µm, the surface 4' is not flat but, as in figure 2A, rather very irregular, with peaks 20 and patterns in relief. Some of these peaks or patterns may have a base with a width L between a few µm or tens of µm and approximately 100 µm, for a height h which may be around a few µm.

This surface 4' of the adhesive layer 4 therefore has, with respect to a mid-plane AA' whose outline is shown in figure 2A, patterns 20 in the form of peaks and patterns 22 in the form of pits.

The inventors have shown that, despite the use of a technique of polishing, for example of the mechanical/chemical type, of the adhesive layer 4, implemented prior to the assembly with the second substrate 8, surface defects, peaks or "voids" 24, 26 may remain, as illustrated in figure 2B. The problems already mentioned above therefore remain.

Figure 2B shows in more detail the surface of the layer of adhesion material 4, after the polishing step. The peaks or pits 24, 26, which may have a width or a diameter Φ that may be less than a millimetre or around 1 millimetre, will not make it possible to make a perfect bonding or molecular assembly with the second substrate 8. Thus defects of the particle type from 0.3 μm to a few μm in height may give rise to bonding defects of around 1 mm to several mm.

To solve this problem, an object of the invention is a process for preparing a layer, for example a thin layer, to be transferred onto a substrate, this layer may be having a surface topology, for example with a maximum amplitude of between 1 μm and 5 μm, this process comprising the formation, on said layer, of a layer of adhesive material, for example an oxide such as a silicon oxide ($SiO_x$) or a silicon oxynitride ($SiO_xN_y$), the thickness of which makes it possible to perform a

step of levelling off (or planarization, the expressions "planarization" and "levelling off" being considered as equivalent here and in the rest of this document) and/or conditioning its surface, or a plurality of steps of levelling off and/or conditioning its surface, in order to eliminate any defect or any "void", or almost any defect or "void", in preparation for an assembly by a bonding of the molecular kind in order to limit the non-bonded zones.

The adhesive layer preferably has an initial thickness lying between:

- a minimum thickness $E_{min}$ making it possible, after a single levelling off (or planarization) and/or conditioning step, to obtain a good molecular bonding, or are brought in contact without bonding defect or almost without bonding defect,

- and a maximum value Emax making it possible, after several polishing steps, to obtain good molecular bonding, that is to say making it possible to eliminate any defect or "void" or almost any defect or void, with a view to assembly by bonding of the molecular kind.

Preferably, the thickness E of the adhesive layer is also limited to a value that does not risk causing excessively high stresses that may result in a deformation of the wafer on which it is deposited. Typically, a value of E of less than 12 µm corresponds to requirements in the field of treatment of semiconductor wafers.

The initial thickness E is therefore chosen so as to be less than 10 µm or 12 µm and preferably greater than 0.5 µm or 3 µm.

The thin layer or adhesive layer may have a surface topology, and therefore variations in altitude and level, in a direction perpendicular to a plane defined by the thin layer.

The thin layer may comprise some components, for example of the electronic and/or optical circuit type, and/or of the microsystem type.

A preparation process according to the invention may also comprise an assembly step, preferably via molecular adhesion bonding, with the second substrate, and an identification or detection step, for example by acoustic microscopy or infrared microscopy, for defects in the contact or bonding interface.

The second substrate and the adhesive layer may be separated if the identification step reveals the presence of one or more defects, liable to be present on the bonding interface, and the adhesive layer undergoes a new step of levelling off and/or conditioning, assembling and detection. This cycle may be recommenced as many times as necessary to obtain good bonding (with no defects or very few defects) by virtue of the fact that the adhesive layer present on the thin layer has a thickness $E_{min}$.

Another object of the invention is therefore a process of preparing a layer in preparation for a transfer onto a substrate, this layer comprising a

surface topology, and therefore variations in altitude or level, in a direction perpendicular to a plane defined by the thin layer, this process comprising:

a) the formation, on the thin layer to be transferred, of a layer of adhesion material, the thickness E of which has a value making it possible to perform at least one (and possibly n, n being an integer, n>1, for example n = 2 or 3) step of levelling off and/or conditioning of the surface,

b) a step of levelling off (or planarization) and/or conditioning said surface,

c) a step of assembling, preferably by molecular bonding, the layer of adhesion material with the substrate; assembling is preferably made by molecular bonding;

d) a step of detecting defects on the bonding interface,

e) a step of separating the substrate at the bonding interface and the adhesive layer surface and a return to step b), when the presence of defects is detected at the bonding interface, or the end of the preparation method.

The second substrate, or final substrate, itself may carry a bonding or adhesive layer, which may also undergo the treatment described above.

The final substrate may comprise a surface topology, and therefore variations in altitude or level, in a direction perpendicular to a plane defined by the final substrate.

An adhesive layer on the final substrate may have a thickness making it possible to perform at least one step of levelling off (or planarization) and/or conditioning of its surface. In addition, before step c), a step of levelling off and/or conditioning of the surface of the adhesive layer on the final substrate may be performed.

Another object of the invention is a process of preparing a layer and a final substrate in preparation for a transfer of this layer onto this final substrate, this layer having a surface topology, and therefore variations in altitude or level, in a direction perpendicular to a plane defined by the thin layer, this process comprising:

a) the formation, on the thin layer to be transferred, of a layer of adhesion material and, on the final substrate, a layer of adhesion material whose thickness E has a value making it possible to perform at least one (and possibly n, n being an integer, n>1, n=2 or 3 for example) step of levelling off and/or conditioning the surface,

b) a step of levelling off (or planarization) and/or conditioning the said surface of the adhesive layer formed on the final substrate,

c) a step of assembling the layer of adhesion material formed on the thin layer, with the layer of adhesion material formed on the final substrate; assembling is preferably made by molecular bonding;

d) a step of detecting defects on the bonding interface,

e) a step of separating the layer of adhesion material formed on the final substrate and the adhesive layer surface formed on the thin layer, at the bonding interface, and a return to step b), when the presence of defects at the bonding interface is detected, or the end of the preparation method.

The final substrate may comprise a surface topology, and therefore variations in altitude or level, in a direction perpendicular to a plane defined by the final substrate.

In all cases it is therefore possible to detach the layer from the substrate in order to recondition the bonding surface or surfaces or layers in order to assemble them once again and to obtain, after one or more of the above cycles, a bonding interface of good quality. The initial wafer and/or the initial substrate, or their respective bonding layers, may be reworked in preparation for obtaining good surfaces for bonding.

If there are two bonding layers the wafer which has an added value, that is to say the thin layer if it comprises circuits, will preferably be reworked. The second support 8 may be a wafer without defect.

This separation of the substrate and bonding layer and the new polishing step may therefore be performed at least twice.

After each levelling off (or planarization) and/or conditioning step, enabling to remove all or part of the surface, and before bonding, a second surface treatment such as levelling (or planarization) and/or polishing can be applied, possibly followed by cleaning. This second surface treatment may be different from the first levelling off (or planarization) and/or conditioning step, through a shorter polishing duration, and/or a lower compression force applied, and/or the use of another consumable, such as another tissue or abrasive.

A process of transferring a layer onto a substrate, according to the invention, comprises a preparation process as disclosed above, the thin layer being initially on a support, this transfer process also comprising the removal of all or part of an initial support on which the thin layer was produced.

In any embodiment of the invention, an adhesive layer is selected in view of the bonding or of the assembly to be made. It is for example a layer of oxide, such as a silicon oxide (stoichiometric or not) or a silicon oxynitride.

In any embodiment of the invention the initial thickness of the adhesive layer can be selected so that n polishing steps, for example n = 2 or 3, will be able to be performed. Preferably each polishing step is able to remove at a maximum approximately 1 µm of material of the adhesive layer, for example 0.2 µm to 0.5 µm. Each polishing step is followed by assembly and checking of

the quality of the interface. Should the interface have defects, or a substantial number of defects, another polishing step can be carried out.

A process according to the invention can be stopped when the bonding interface is considered satisfactory or if no defects or only few defects are detected at the bonding interface.

In any embodiment of the invention it is possible to have a layer of adhesion material whose thickness E has a value making it possible to perform at least n (n being an integer, $n>1$, $n=2$ or 3 for example) steps of levelling off and/or conditioning the surface, whereas only n-1 or only n-2 or only n-p (p integer, $1 \leq p < n$) planarization and/or conditioning step and detection step are performed, the interface having no defects or very few defects after n-p planarization and/or conditioning step. Part of the initial adhesive layer remains on the thin layer to be transferred after the n levelling off and/or conditioning steps.

**BRIEF DESCRIPTION OF THE FIGURES**

- Figures 1A to 1D depict steps of a known simple transfer method,
- figures 2A and 2B illustrate the topology of the bonding surface and the problems that may stem from this,
- figure 3 depicts a situation of flexing of a wafer under an excessively great thickness of bonding material.

**DETAILED DISCLOSURE OF PARTICULAR EMBODIMENTS**

According to the invention, a structure of the same type as that in figure 2A is therefore considered, and therefore having, on a microscopic scale, a topology which may be very marked, as illustrated in figure 2B. This topology results, as has been seen, from the topology of the thin layer 5 containing the components 3, 6. The component or components 3, 6 of the thin layer 5 may be of the electronic and/or optical circuit type, and/or of the microsystem type, one or more of the functionalities of the component or components possibly being able to be controlled by contacts, not shown in the figure.

The topology is defined as differences in altitudes or levels between the elevated zones and the low zones of this thin layer (with reference to a direction perpendicular to a plane defined by the thin layer), which correspond for example to several levels of metal or, more generally, to several levels in different zones in which different materials can be stacked. This definition of the topology, through its amplitude, may possibly be supplemented by the surface distribution of the topology, and/or the frequency of the topology and/or ratio of the topology in relief to the whole of the surface.

The differences in level may attain a value (in a direction z perpendicular to a plane defined by the layer 5 and represented by a line AA' in figure 1A) of

around several µm, these are for example between 0.5 µm and a few µm, for example between 0.5 µm and 5 µm or between 0.5 µm and 10 µm.

This maximum difference in level reflects essentially the difference h between the highest point of the surface and the lowest point of the surface, of which it will be sought to take account in order to define the thickness of the adhesive layer 4, which will then be sought to be levelled off over its entire surface.

The initial thickness of this adhesive layer 4 of adhesion material is chosen so as to enable to perform a levelling off and/or conditioning step or a plurality of levelling off and/or conditioning steps on its surface, in order to eliminate any defect or "void" 24, 26, in preparation for an assembly by bonding of the molecular kind with the second substrate 8. Part of the initial adhesive layer 4 remains after the levelling off and/or conditioning step or the plurality of levelling off and/or conditioning steps.

A single levelling off or polishing step will enable to remove approximately 1 µm of thickness of the adhesive layer 4. This removal may vary according to the duration of the polishing step and the polishing process used, in particular the consumables, tissues, and abrasives used.

For example, the application of two polishing and conditioning steps allows the removal of a thickness of this adhesive layer 4 comprised between 1 µm and 5 µm.

The thicknesses to be removed are adapted according to the size of the topology defects to be eliminated.

In this example, an initial thickness of the adhesive layer 4 lying for example between 0.5 µm and 10 µm will therefore be chosen. Another aspect may have to be taken into account for choosing the thickness of the adhesive layer 4. This aspect will be explained in relation to figure 3, on which the reference 2 designates a global stack comprising, as in figure 1A, a treated thin layer 5 on a first substrate 1. As explained above, the front face of this thin layer 5 is intended to be bonded with a second wafer 8 by means of the layer 4 of adhesion material. The latter, as from a certain critical thickness, which may be situated at a maximum at approximately 10 µm or 12 µm, may give rise to stresses resulting in a deformation (of the bow or warp type) of the thin layer to be transferred. This deformation is shown in figure 3, in an exaggerated fashion.

This deformation is detrimental for obtaining good bonding for good alignment between the wafers 2, 8 to be assembled since it may cause the deformation of the transferred layer. Preferably, the thickness of the adhesive layer 4 is therefore limited to a value that does not risk causing this deformation of the wafer. A value of E below 10 µm or 12 µm corresponds to requirements in the field of treating semiconductor wafers.

The surface 4' of this adhesive layer 4 has a topology that reflects that of the thin layer 5, with

similar differences in level or amplitudes, for example between 0.5 µm and a few µm, for example between 0.5 µm and 5 µm or between 0.5 µm and 10 µm.

The invention can apply also to the case where the layers are structured but "homogeneous", for example in the case of a thin layer 5, without components 3, 6, having zones, none of which is metallic, these different zones having a surface topology and therefore variations in altitude as explained above, and in particular in the ranges indicated above.

The adhesive layer 4 of adhesion material is for example a layer of oxide, such as a silicon oxide (stoichiometric or not) or a silicon oxynitride.

The material of this adhesive layer 4 is chosen for its bonding qualities, which will be reinforced by preparation of the surface finish of this layer, such as a new surface activation step, for example a mechanical/chemical polishing.

After this step of preparing the surface finish, assembly with the final support 8 can be carried out, as illustrated in figure 1D.

This final support 8 can be subjected to a heat treatment step. Both the surface of the adhesion material and that of the oxide can be made hydrophilic, with a view to assembly by molecular adhesion.

After assembly, and before the application of any heat treatment for consolidating the bonding interface, it is possible to check the quality of the interface between the adhesive layer and the final

substrate 8. For this purpose, it is possible to use techniques such as for example acoustic microscopy or infrared imaging or microscopy, as described in the document WO2005/064320. The infrared technique has the advantage of being quicker than the acoustic microscopy technique, even if the resolution is worse.

If this identification step reveals bonding defects (due to surface defects or to "voids" 24, 26 on the surface of the assembled wafers and more probably on the surface of the flattened circuit wafer), the final substrate 8 is separated once again from the adhesive layer 4, and once again a step of levelling off and/or conditioning of the surface of the latter is carried out in order to eliminate a maximum number of defects.

The initial thickness of the adhesive layer 4 is therefore designed so that a plurality, for example two or three, or n (n>3) polishing steps will be able to be performed. Each step is followed, or can be followed, by assembly and checking of the quality of the interface. If said quality is not satisfactory, then the substrates are separated at the bonding interface as explained above and another polishing step is performed, and then the substrates are assembled again. A further detection step can also be performed. Preferably each step is able to remove at a maximum approximately 1 μm of material of the layer 4, more generally 0.2 μm to 0.5 μm.

After these various preparation steps, the final assembly with the final support 8 can be carried out, as illustrated in figure 1C. After this assembly

with the final support 8, all or part of the initial support 1 can be removed, giving access to the rear face 5'' of the thin layer 5 (figure 1D).

The final support 8 can be a solid substrate or a multilayer structure. It may also correspond to a substrate having a surface topology, for example on or in which some circuits are already present. This substrate can be subjected to the same levelling off treatment as the wafer 2 according to the present invention.

If there is also a bonding layer on the substrate 8, the interface after separation will be situated between the two adhesive layers.

In a variant, it is the layer 10 on the substrate 8 that undergoes a treatment according to the invention, and which has a thickness E making it possible to perform at least one step of levelling off and/or conditioning of the surface of this layer 10. The thickness E can in particular be chosen in ranges or limits indicated above, so as to allow one or more or n (n>1) polishing and/or conditioning steps. The other steps already described above are implemented: assembly, fault detection, separation and, once again, polishing and/or conditioning of the surface of the layer 10, several times if necessary.

In general terms, the separation occurs at the bonding interface since this has not yet been subjected to heat treatment to reinforce the bonding energy and therefore can be dismantled. Thus, in the case in figure

2B, the separation occurs at the surface 4' of the adhesive layer.

This assembly can then be subjected to a heat treatment step, after, or preferably before, the removal of the initial support 1, in order to reinforce the bonding between the adhesive layer 4 and the final substrate 8. Both the surface 4' of the adhesion material and that of the oxide 10 of the final substrate 8 will preferably have undergone cleaning steps after the levelling off in preparation for a molecular assembly.

**CLAIMS**

1.Process of preparing a layer (5) in preparation for a transfer onto a substrate (8), this layer comprising a surface topology, and therefore variations in altitude or level, in a direction perpendicular to a plane defined by the thin layer, this process comprising:

a) the formation, on the thin layer (5) to be transferred, of a layer of adhesion material, or adhesive layer (4) , the thickness E of which has a value enabling to perform several steps of levelling off and/or conditioning of the surface,

b) a step of levelling off and/or conditioning said surface,

c) a step of assembling the layer of adhesion material (4) with the substrate (8),

d) a step of detecting defects (24, 26) on the bonding interface,

e) a step of separating the substrate (8) at the bonding interface and the adhesive layer surface (4) and a return to step b) , when the presence of defects (24, 26) is detected at the bonding interface, or the end of the preparation method.

2. Process according to claim 1, the final substrate (8) also comprising an adhesive layer.

3. Process according to claim 2, the final substrate (8) having a surface topology, and therefore variations in altitude or level, in a direction perpendicular to a plane defined by the final substrate.

4. Process according to claim 2 or 3, the adhesive layer (10) on the final substrate (8) having a thickness making it possible to perform at least one step of levelling and/or conditioning its surface.

5. Process according to claim 4, also comprising, before step c), a step of levelling and/or conditioning of the surface of the adhesive layer on the final substrate.

6. Process of preparing a layer (5) and final substrate (8) in preparation for a transfer of this layer onto this final substrate, this layer having a surface topology, and therefore variations in altitude or level, in a direction perpendicular to a plane defined by the thin layer, this process comprising:

a) the formation, on the thin layer (5) to be transferred, of a layer of adhesion material, or adhesive layer (4) and, on the final substrate (8), a layer of adhesion material (10) whose thickness E has a value making it possible to perform several steps of levelling off and/or conditioning the surface,

b) a step of levelling off and/or conditioning the said surface of the adhesive layer (10) formed on the final substrate (8),

c) a step of assembling the layer of adhesion material formed on the thin layer (4), with the layer of adhesion material (10) formed on the final substrate (8),

d) a step of detecting defects (24, 26) on the bonding interface,

e) a step of separating the layer of adhesion material (10) formed on the final substrate (8) and the adhesive layer surface (4) formed on the thin layer, at the bonding interface, and a return to step b), when the presence of defects (24, 26) at the bonding interface is detected, or the end of the preparation method.

7. Process according to claim 6, the final substrate (8) having a surface topology, and therefore variations in altitude or level, in a direction perpendicular to a plane defined by the final substrate.

8. Process according to one of claims 1 to 7, step e) and the return to step b) being performed at least twice.

9. Process according to one of claims 1 to 8, the initial thickness E being less than 10 μm.

10. Process according to one of claims 1 to 9, the initial thickness E being greater than 0.5 μm.

11. Process according to one of claims 1 to 10, step d) being performed by acoustic microscopy or infrared microscopy.

12. Process of transferring a layer (5) onto a final substrate (8), comprising a preparation process according to one of claims 1 to 11, the thin layer (5) being initially on a support (1), this transfer process also comprising the removal of all or part of this initial support (1).

13. Process according to one of claims 1 to 12, step c) being a bonding via molecular adhesion.

14. Process according to one of claims 1 to 13, the adhesive layer or layers (4, 10) being made from an oxide.

15. Process according to claim 14, the adhesive layer or layers (4, 10) being a silicon oxide ($SiO_x$) or a silicon oxynitride ($SiO_xN_y$).

16. Process according to one of claims 1 to 15, the initial topology of the layer (5) to be transferred to the circuit having a maximum amplitude of less than 10 µm.

17. Process according to claim 16, the initial topology of the thin layer (5) to be transferred from the circuit having a maximum amplitude of between 1 µm and 5 µm.

18. Process according to one of claims 1 to 17, the thin layer (5) comprising components (3, 6).

19. Process according to claim 18, the components being of the electronic and/or optical circuit type, and/or of the microsystem type.

20. Process according to one of claims 1 to 19, comprising, after at least one step b) of levelling of one of the adhesive layers, and before the following step c), a polishing and/or conditioning of the surface of this adhesive layer followed by a cleaning of this same surface.