BALL GRID ARRAY INTERPOSER, PACKAGES AND METHODS

TECHNICAL FIELD

The present invention relates generally to packaged semiconductor devices with ball grid array (BGA) connection patterns and, more specifically, to packages having thicknesses that are only slightly greater than the thickness of their associated interposers. Particularly, the present invention relates to package interposers with receptacles formed therein that extend substantially through the thicknesses of the interposers and that are configured to receive semiconductor devices in such a manner that active surfaces of the semiconductor devices are located in or below substantially the same planes as the corresponding upper surfaces of the interposers.

BACKGROUND

The dimensions of many different types of state of the art electronic devices are ever decreasing. To reduce the dimensions of electronic devices, the structures by which the microprocessors, memory devices, other semiconductor devices, and other electronic componentry of these devices are packaged and assembled with circuit boards must become more compact.

One approach to reducing the sizes of assemblies of semiconductor devices and circuit boards has been to minimize the profiles of the semiconductor devices and other electronic components upon carrier substrates (e.g., circuit boards) so as to reduce the distances the semiconductor devices protrude from the carrier substrates. Various types of packaging technologies have been developed to facilitate orientation of semiconductor devices upon carrier substrates in this manner.

Some semiconductor device packages are configured to be oriented substantially parallel to a plane of a carrier substrate, such as a circuit board. Conventionally, semiconductor device packages included several layers stacked one on top of another (e.g., a bottom layer of encapsulant material, a die-attach paddle of a lead frame, a semiconductor die, and a top layer of encapsulant material). In addition, the leads or pins of conventional semiconductor device packages, which electrically connect such packages to carrier substrates, as well as provide support for the packages, are sometimes configured to space the semiconductor device packages apart from a carrier substrate. As a result, the overall thicknesses of these semiconductor device packages and the distances the packages protrude from carrier substrates are larger than is often desired for use in state-of-the-art electronic devices.

"Flip-chip" technology, or controlled collapse chip connection (C-4), is another example of an assembly and packaging technology that results in a semiconductor device being oriented substantially parallel to a carrier substrate, such as a circuit board. In flip-chip technology, the bond pads or contact pads of a semiconductor device are arranged in an array over a major surface of the semiconductor device. Flip-chip techniques are applicable to both bare and packaged semiconductor devices. A packaged flip-chip type semiconductor device, which typically has a ball grid array connection pattern, typically includes a semiconductor die and a substrate, which is typically termed an "interposer". The interposer may be disposed over either the backside of the semiconductor die or the front (active) surface thereof.

When the interposer is positioned adjacent the backside of the semiconductor die, the bond pads of the semiconductor die are typically electrically connected by way of wire bonds or other intermediate conductive elements to corresponding contact areas on a top side of the interposer. These contact areas communicate with corresponding bumped contact pads on the backside of the interposer. This type of flip-chip assembly is positioned adjacent a carrier substrate with the backside of the interposer facing the carrier substrate.

If the interposer is positioned adjacent the active surface of the semiconductor die, the bond pads of the semiconductor die may be electrically connected to corresponding contact areas on an opposite, top surface of the interposer by way of intermediate conductive elements that extend through one or more holes formed in the interposer. Again, the contact areas communicate with corresponding contact pads on the interposer. In this type of flip-chip semiconductor device assembly, however, the contact pads are also typically located on the top surface of the interposer. Accordingly, this type of flip-chip assembly is positioned adjacent a carrier substrate by orienting the interposer with the top surface facing the carrier substrate.

In each of the foregoing types of flip-chip semiconductor devices, the contact pads of the interposer are disposed in an array that has a footprint that mirrors an arrangement of corresponding terminals formed on a carrier substrate. Each of the bond (on bare flip-chip semiconductor dice) or contact (on flip-chip packages) pads and its corresponding terminal may be electrically connected to one another by way of a conductive structure, such as a solder ball, that also spaces the interposer some distance away from the carrier substrate.

The space between the interposer and the carrier substrate may be left open or filled with a so-called "underfill" dielectric material that provides additional electrical insulation between the semiconductor device and the carrier substrate. In addition, each of the foregoing types of flip-

chip type semiconductor devices may include an encapsulant material covering portions or substantially all of the interposer and/or the semiconductor die.

The thicknesses of conventional flip-chip type packages having ball grid array connection patterns are defined by the combined thicknesses of the semiconductor die, the interposer, and the conductive structures (e.g., solder balls) that protrude above the interposer or the semiconductor die. As with the flat packages, conventional flip-chip type packages are often undesirably thick for use in small, thin, state of the art electronic devices.

Thinner, or low-profile, flip-chip type packages have been developed which include recesses that are configured to at least partially receive semiconductor devices. While interposers that include recesses for partially receiving semiconductor devices faciliate the fabrication of thinner flip-chip type packages, the semiconductor dice of these packages, as well as intermediate conductive elements that protrude beyond the outer surfaces of either the semiconductor dice or the interposers, undesirably add to the thicknesses of these packages.

U.S. Patent 5,639,695, issued to Jones et al. (hereinafter "the '695 Patent") discloses another type of flip-chip type package, which includes an interposer with a semiconductor die receptacle extending completely therethrough. The '695 Patent teaches that the package may be formed by securing the semiconductor die directly to a carrier substrate and electrically connecting the interposer to the carrier substrate before the semiconductor die is electrically connected to the interposer. The semiconductor die, intermediate conductive elements that connect bond pads of the semiconductor die to corresponding contact areas on the interposer, and regions of the interposer adjacent the receptacle may then be encapsulated. While this method results in a very low-profile flip-chip type package, the package cannot be tested separately from the carrier substrate. As a result, if the package is unreliable, it may also be necessary to discard the carrier substrate and any other components thereon. Moreover, the packaging method of the '695 Patent complicates the process of connecting semiconductor devices and other electronic componentry to a carrier substrate.

Thus, there is a need for low-profile flip-chip type packages that may be tested prior to their assembly with a carrier substrate and without adding complexity to the process of assembling electronic components to the carrier substrate. A method for fabricating such low-profile flip-chip type packages is also needed.

DISCLOSURE OF INVENTION

The present invention includes a flip-chip type package interposer having a ball grid array connection pattern, packages including the interposer, and methods for assembling and packaging one or more semiconductor devices with the interposer.

The package interposer of the present invention includes a substantially planar substrate with a receptacle formed therein and extending substantially through a thickness thereof. The receptacle is configured to receive one or more semiconductor devices (e.g., dice) in such a manner that the active surface of each semiconductor device positioned within the receptacle is located in or positioned below a plane in which an associated upper surface of the interposer is located. In addition, the interposer includes contact areas, which are preferably located proximate to the periphery of the receptacle, each contact area corresponding to a bond pad of a semiconductor device positioned within the receptacle. Conductive traces extend from the conductive areas, on or through the substrate, to corresponding terminals arranged in an array over a surface of the interposer. The terminals may be located on the same surface of the interposers as the conductive areas or on the opposite surface of the interposer.

If the receptacle of the interposer extends completely through the substrate, a film may be positioned over the surface of the interposer opposite that on which the contact areas are located so as to close a bottom end of the receptacle and to facilitate the positioning of one or more semiconductor devices within the receptacle. The film may be removably secured to the interposer, thereby facilitating the removal of the film and, thus, a further reduction in the thickness of the interposer and a package including the interposer.

One or more semiconductor devices may be assembled with the interposer by positioning each semiconductor device within the receptacle. When the bottom end of the receptacle is enclosed, each semiconductor device positioned therein may be secured to the tape or other member covering the bottom end to fix the position of each semiconductor device relative the substrate of the interposer. Each bond pad of a semiconductor device located within the receptacle of the interposer may be electrically connected with a corresponding contact area of the interposer by use of known intermediate conductive elements, such as bond wires.

A semiconductor device package incorporating teachings of the present invention includes the interposer-semiconductor device assembly, with each semiconductor device positioned within the receptacle being held into position by an encapsulant material extending between an outer periphery of that semiconductor device and a periphery of the receptacle. The encapsulant material may also cover intermediate conductive elements that extend between the bond pads of

each semiconductor device and their corresponding contact areas on a surface of the interposer. If the encapsulant material extends above the surface of the interposer, it is preferred that the distance the encapsulant material protrudes from that surface is less than the distance the interposer will be spaced apart from the carrier substrate when conductive structures, such as solder balls or other discrete conductive elements, are secured to any terminals on that surface and connected to corresponding terminals of the carrier substrate. As the encapsulant material holds the one or more semiconductor devices within the receptacle, tape or any other structure that was previously used to maintain the position of each semiconductor device within the receptacle may be removed. Thus, the overall thickness of a package incorporating teachings of the present invention is substantially equal to the thickness of the interposer and the distances that conductive structures may protrude above a surface of the interposer.

An exemplary method for assembling a semiconductor device package in accordance with teachings of the present invention includes providing an interposer with a receptacle formed completely therethrough, positioning a film or tape over a bottom end of the receptacle, and removably securing the film or tape to a surface of the interposer to enclose the bottom end of the receptacle. One or more semiconductor devices are then positioned within the receptacle and secured to the film or tape enclosing the bottom end thereof. The bond pads of each semiconductor device located within the receptacle and their corresponding contact areas on the interposer are electrically connected to one another. An encapsulant material is introduced into the receptacle to extend laterally between the outer periphery of each semiconductor device within the receptacle and the inner periphery of the receptacle. The encapsulant material may also be disposed over the active surface of each semiconductor device located within the receptacle, as well as over intermediate conductive elements that connect the bond pads to their corresponding conductive areas on a surface of the interposer and adjacent portions of that surface of the interposer. Once each semiconductor device is held in place within the receptacle by encapsulant material, the tape or film that previously held the one or more semiconductor devices in place may be removed.

In the inventive packaging method, conductive structures, such as solder balls or other discrete conductive elements, may also be positioned on terminals which are arranged in an array over a surface of the interposer, each terminal corresponding to and in communication with a conductive area of the interposer and, thus, with the bond pad of a semiconductor device positioned within the receptacle.

The present invention also includes multi-chip assemblies of semiconductor device packages incorporating teachings of the present invention. These assemblies, which may be referred to as multi-chip modules (MCMs), may include two or more of the inventive semiconductor device packages in a stacked arrangement. Adjacent packages may be electrically connected to one another by connecting the conductive structures protruding from terminals of a first semiconductor device package to corresponding secondary terminals located on a back side of an adjacent, second semiconductor device package. Of course, at least some of the secondary terminals of a semiconductor device package incorporating teachings of the present invention may be electrically connected to bond pads of a semiconductor device of the semiconductor device package.

Other features and advantages of the present invention will become apparent to those of ordinary skill in the art through consideration of the ensuing description, the accompanying drawings, and the appended claims.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

In the drawings, which illustrate exemplary embodiments for carrying out the invention:

FIG. 1 is a top view of a semiconductor device package interposer and a semiconductor device package incorporating teachings of the present invention;

FIG. 2 is a cross-section taken along line 2–2 of FIG. 1;

FIG. 2A is a cross-sectional representation of the package of FIG. 2 with a heat sink attached thereto.

FIGs. 2B and 2C are cross-sectional representations of variations of the interposer illustrated in FIGs. 1 and 2, which variations include interposers with terminals on both surfaces thereof;

FIG. 2D is a cross-sectional representation of a package including the interposer of FIG. 2C;

FIG. 3 is a top view of another embodiment of interposer according to the present invention;

FIG. 4 is a top view of an assembly including an interposer of the present invention and multiple semiconductor devices within the receptacle of the interposer;

FIGs. 5-10A illustrate an exemplary embodiment of an assembly and packaging method of the present invention; and

FIG. 11 is a cross-sectional representation of a multi-chip module including semiconductor device packages according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIGs. 1 and 2, a flip-chip type semiconductor device package 100 according to the present invention is illustrated. Package 100 includes an interposer 20 with a substantially planar substrate 8 and a receptacle 18 formed in and extending substantially through substrate 8. Package 100 also includes a semiconductor device 6 positioned within the receptacle 18 and encapsulant material 4 extending between semiconductor device 6 and a peripheral edge 19 of receptacle 18.

The substrate 8 of interposer 20 may be formed from either a rigid or flexible material. For example, the substrate 8 may be formed from silicon or another semiconductive material (e.g., gallium arsenide, indium phosphide, etc.), with at least some surfaces thereof being lined with an electrically insulative material to prevent shorting of the various electrical circuits running thereacross. Alternatively, other suitable interposer substrate materials may be used to form the substrate 8, including, without limitation, FR-4 resin, ceramic, and polyimide.

The receptacle 18 is formed somewhat centrally within and laterally confined by the material of the substrate 8. The receptacle 18 extends into the top surface 32 of the substrate 8 a sufficient distance that the receptacle 18 is configured to receive one or more (FIG. 4) semiconductor devices 6 (e.g., dice) in such a manner that the active surface 22 of each semiconductor device 6 positioned within the receptacle 18 is located in or positioned below the plane in which the top surface 32 of the substrate 8 is located, as shown in FIG. 2. Optionally, as shown in FIG. 3, an interposer 120 incorporating teachings of the present invention may include more than one receptacle 118 formed within a single substrate 108 thereof.

The height of the receptacle 18 may be substantially equal to a thickness of the substrate 8 and, as indicated above, preferably exceeds a thickness of a semiconductor device 6 to be positioned therein. When the receptacle 18 extends completely through the substrate 8, a thin film 28 (e.g., tape) may be positioned to enclose, or substantially cover, a bottom end 24 of the receptacle 18 to facilitate the placement of one or more semiconductor devices 6 in fixed positions therein. Such a film 28 may be secured to a bottom surface 34 of the substrate 8. Preferably, the film 28 is removably secured to the bottom surface 34 the substrate 8, facilitating the subsequent removal of the film 28 and, thus, further reducing the thickness of a package 100

including the interposer 20. For example, an adhesive material (e.g., a pressure-sensitive adhesive material) may be used to secure the film 28 to the bottom surface 34 of the substrate 8.

The backside 26 (i.e., the side opposite the active surface 22) of each semiconductor device 6 of a package 100 may also be removably secured to the film 28, such as with an adhesive material. When the film 28 is removed from the substrate 8, the backside 26 of each semiconductor device 6 positioned thereon may be exposed.

If the receptacle 18 does not extend completely through the substrate 8, one or more semiconductor devices 6 may be positioned upon and secured (e.g., with an adhesive material) to a bottom surface (not shown) of the receptacle 18.

The interposer 20 also includes contact areas 36 (e.g., contact pads) formed on the top surface 32 thereof, adjacent the receptacle 18. Each contact area 36 corresponds with and is configured to be electrically connected to, via intermediate conductive elements 10, a bond pad 12 of a semiconductor device 6 positioned within the receptacle 18. The intermediate conductive elements 10 may comprise, for example, aluminum wire, gold, silver, conductive alloys, tape automated bonding (TAB) connections, or the like.

Conductive traces 38 extend substantially laterally from each contact area 36, on or through the substrate 8, to corresponding terminals 40 arranged in an array over the top surface 32 the substrate 8. Thus, each terminal 40 corresponds to, and is in communication with, a contact area 36 of the interposer 20. Consequently, when each contact area 36 and its corresponding bond pads 12 are electrically connected to one another by way of an intermediate conductive element 10, each terminal 40 communicates with a corresponding bond pad 12 of a semiconductor device 6 positioned within the receptacle 18.

As depicted in FIG. 2B, some conductive traces 38 of an interposer 20′ incorporating teachings of the present invention may extend to an electrically conductive via 39 that extends from the top surface 32′ to the bottom surface 34′ of the substrate 8′ rather than to a terminal 40. Each such electrically conductive via 39, in turn, communicates with another terminal 42, which may be formed directly on the electrically conductive via 39 or communicate therewith by way of a conductive trace 38 that either extends across the bottom surface 34 of the substrate 8′ or internally through the substrate 8′, near the bottom surface 34′ thereof.

Alternatively, as shown in FIG. 2C, at least some contact areas 36 of an interposer 20″ incorporating teachings of the present invention may comprise electrically conductive vias 39 that extend through the substrate 8″, from the top surface 32″ thereof to the bottom surface 34″

thereof. Again, each of these contact areas 36 may communicate with a terminal 42 formed on the bottom surface 34″ of the substrate 8″, either directly, or by way of a substantially laterally extending conductive trace 38.

Referring to FIGs. 1, 2, and 2D, conductive structures 2, such as balls, bumps, columns, pillars, or other structures formed from a conductive material, such as solder, metal, or z-axis conductive elastomer, may be secured to terminals 40, 42 to facilitate communication between the one or more semiconductor devices of the semiconductor device package 100, 100″ and a carrier substrate or another package 100′ (FIG. 11).

Package 100 also includes a quantity of dielectric encapsulant material 4 within each receptacle 18 of the interposer 20. The encapsulant material 4 extends laterally between at least portions of an outer periphery 7 of each semiconductor device 6 positioned within the receptacle 18 and a peripheral edge 19 of the receptacle 18. The encapsulant material 4 at least partially secures and laterally confines each semiconductor device 6 within the receptacle 18. As shown in FIG. 1, the encapsulant material 4 may substantially fill the receptacle 18 and may also at least partially cover the active surface 22 of the semiconductor device 6, as well as the intermediate conductive elements 10 and portions of the top surface 32 of the substrate 8 over which the intermediate conductive elements 10 extend. If the encapsulant material 4 protrudes above a plane in which the top surface 32 of the substrate 8 is located, the distance the encapsulant material 4 protrudes from the top surface 32 is less than the distance the top surface 32 will be spaced apart from a carrier substrate or another semiconductor device package 100′ (FIG. 11) by conductive structures 2 when the package 100 is electrically connected to the carrier substrate or other package 100′.

Preferably, the package 100 of the present invention has a total thickness of less than about 1 mm, making the package 100 suitable for use in compact electronic devices, such as cellular telephones, handheld computers, and portable computers, where such low profile packages are required or desired.

As illustrated in FIG. 2A, if desired, the package 100 may have a heat sink 60 attached thereto, as known in the art, to improve its thermal performance.

FIGs. 5-10A illustrate an exemplary method for assembling a package incorporating teachings of the present invention.

FIGs. 5 and 5A illustrate interposer strips 50, each of which includes a plurality of physically connected interposers 20 formed thereon. Each interposer 20 of strip 50 includes a

receptacle 18 formed therethrough, as well as contact areas 36 positioned on a top surface 32 of substrate 8. Although not illustrated in FIGs. 5 and 5A, each interposer 20 may also include terminals 40, 42 (FIGs. 1-2B) corresponding to and in communication with the contact areas 36 of that interposer 20.

As the receptacle 18 extends completely through the substrate 8 of each interposer 20, a film 28 (e.g., tape) is positioned over a bottom end 24 of the receptacle 18 to cover at least a portion of the bottom end 24. The film 28 may comprise either a single strip or several smaller pieces.

FIGs. 6 and 6A illustrate the positioning of a semiconductor device 6 within the receptacle 18 of each interposer 20. Each semiconductor device 6 may be secured into position within its corresponding receptacle by securing the backside 26 thereof to a surface of the film 28 exposed to the receptacle 18, such as with a suitable adhesive material. Although FIG. 7 depicts two semiconductor devices 6 within each receptacle 18, any number of semiconductor devices 6 may be positioned within a receptacle 18.

Once the semiconductor devices 6 have been positioned within their corresponding receptacles 18, the bond pads 12 (FIG. 2) of each semiconductor device 6 may be electrically connected with corresponding contact areas 36 of the corresponding interposer 20 by use of known types of intermediate conductive elements 10, such as bond wires, tape-automated bonds ("TABs"), or bonded leads, as illustrated in FIGs. 7 and 7A. Intermediate conductive elements 10 may be positioned or formed between each bond pad 12 and its corresponding contact area 36 and respective ends thereof bonded to the bond pad 12 and the contact area 36, as known in the art.

Turning now to FIGs. 8 and 8A, a suitable, known type of encapsulant material 4 (e.g., a filled polymer transfer molding compound or a silicone or epoxy type glob-top type encapsulant material) is introduced into the receptacle 18 of each interposer 20 of the interposer strip 50. The encapsulant material 4 extends laterally between at least portions of the outer periphery 7 of each semiconductor device 6 within the receptacle 18 and a peripheral edge 19 of the receptacle 18. The encapsulant material 4 may also substantially cover the intermediate conductive elements 10 that extend between the bond pads 12 of each semiconductor device 6 and the contact areas 36 of the interposer 20. Accordingly, the encapsulant material 4 may substantially fill the receptacle 18 and at least partially cover the active surface 22 of each semiconductor device 6, as well as the regions of the top surface 32 of the interposer 20 at which the contact areas 36 are located.

Once the encapsulant material 4 has been introduced into the receptacle 18, it is permitted to harden, set, or cure. For example, if a thermoplastic resin is used as the encapsulant material 4, the encapsulant material will harden upon cooling of the same. If a transfer molding compound or other thermosetting resin is used as the encapsulant material 4, the encapsulant material 4 may be cured by applying heat and/or pressure to the same. If the encapsulant material 4 is a photoimageable polymer, the encapsulant material 4 may be set or cured by exposing the same to an appropriate wavelength of radiation.

As depicted in FIG. 9, when encapsulant material 4 has hardened, set, or cured, the encapsulant material 4 holds the one or more semiconductor devices 6 within the receptacle 18. Accordingly, the film 28 (FIG. 8A) may be removed from the bottom surface 34 of each interposer 20, with each semiconductor device 6 being suspended in the receptacle 18 of that interposer 20 and the backside 26 of each semiconductor device 6 within the receptacle 18 being exposed.

FIGs. 10 and 10A illustrate that conductive structures 2 may be secured to terminals 40, 42 (FIGs. 2A and 2B) mounted on the top surface 32 of the substrate 8 to allow connection to another package 100 (FIG. 11) or carrier substrate, as known in the art. The package 100 may be mounted with conductive structures 2 in either a dual-in line matrix, a peripheral matrix, or another array pattern. If a substrate strip 50 is used to fabricate the packages 100, adjacent packages 100 may be separated from one another after fabrication by known techniques, such as by use of a wafer saw or otherwise, as known in the art.

The overall thickness of the resulting semiconductor device package 100 is substantially equal to the combined thicknesses of the interposer 20 and the distances that conductive structures 2 protrude above a surface of the interposer 20.

While FIGs. 5-10A depict the inventive process using a substrate strip 50 having plurality of physically connected interposers 20, each interposer 20 having a single receptacle with multiple semiconductor devices 6 mounted therein, it will be understood that the process is applicable to any interposer 20 with a receptacle 18 extending substantially therethrough, including a single interposer 20 and an interposer 20 having more than one receptacle 18.

As depicted in FIG. 11, the present invention also includes stacked assemblies of semiconductor device packages 100, 100′ incorporating teachings of the present invention, which assemblies are typically referred to as multi-chip modules ("MCMs") 200. Adjacent packages 100, 100′ may be electrically connected to one another by connecting the conductive

structures 2 protruding from terminals 40 of a first package 100 to corresponding terminals 42 located on the bottom surface 34′ (shown on top as the package 100′ is in an inverted orientation) of an interposer substrate 8′ of an adjacent, second package 100′. While FIG. 11 depicts a multi-chip module 200 including two packages 100, 100′, it will be understood that a multi-chip module incorporating teachings of the present invention may include than two packages.

Although the foregoing description contains many specifics, these should not be construed as limiting the scope of the present invention, but merely as providing illustrations of some exemplary embodiments. Similarly, other embodiments of the invention may be devised which do not depart from the spirit or scope of the present invention. Features from different embodiments may be employed in combination. The scope of the invention is, therefore, indicated and limited only by the appended claims and their legal equivalents, rather than by the foregoing description. All additions, deletions, and modifications to the invention, as disclosed herein, which fall within the meaning and scope of the claims are to be embraced thereby.

CLAIMS

What is claimed is:

1. An interposer for use in a ball grid array-type semiconductor device package, comprising:

a substantially planar substrate comprising a semiconductor material;

a receptacle formed within and laterally confined by said substrate, said receptacle having a height that is substantially equal to a thickness of said substrate; and

a film at least partially covering an end of said receptacle.

2. The interposer of claim 1, wherein said receptacle is configured to receive at least one semiconductor device.

3. The interposer of claim 2, wherein said height of said receptacle exceeds a thickness of said at least one semiconductor device.

4. The interposer of claim 2, wherein said substrate includes at least one contact area positioned on a first surface thereof, adjacent said receptacle, said at least one contact area corresponding to a bond pad of said at least one semiconductor device.

5. The interposer of claim 4, further comprising at least one terminal in communication with said at least one contact area.

6. The interposer of claim 5, wherein said at least one terminal is positioned on said first surface.

7. The interposer of claim 5, wherein said at least one terminal is positioned on a second surface of said substrate.

8. The interposer of claim 5, further comprising at least one secondary terminal positioned on an opposite surface of said substrate from said at least one terminal, said at least one secondary terminal in communication with another conductive area on said substrate.

9. The interposer of claim 1, wherein said film substantially covers said end of said receptacle.

10. The interposer of claim 1, wherein said film is secured to a surface of said substrate.

11. The interposer of claim 10, wherein said film is removably secured to said surface.

12. The interposer of claim 1, wherein at least a portion of said film within said receptacle has an adhesive material thereon.

13. The interposer of claim 12, wherein said adhesive material comprises a pressure sensitive adhesive material.

14. The interposer of claim 1, wherein said receptacle extends completely through said substrate.

15. A ball grid array-type semiconductor device package, comprising:
an interposer including:
a substrate; and
a receptacle formed within said substrate, said receptacle having a height that is substantially the same as a thickness of said substrate;
a semiconductor device positioned within said receptacle, at least a portion of a back side of said semiconductor device being exposed through said interposer; and
a quantity of encapsulant material extending laterally between at least a portion of an outer periphery of said semiconductor device and a periphery of said receptacle, said quantity of encapsulant material at least partially securing said semiconductor device within said receptacle.

16. The semiconductor device package of claim 15, wherein said receptacle extends substantially through said substrate.

17. The semiconductor device package of claim 15, wherein said interposer comprises a thin film at least partially covering a bottom end of said receptacle.

18. The semiconductor device package of claim 17, wherein said thin film is secured to a surface of said substrate.

19. The semiconductor device package of claim 18, wherein said thin film is removably secured to a surface of said substrate.

20. The semiconductor device package of claim 17, wherein at least portions of said thin film exposed within said receptacle have adhesive material thereon.

21. The semiconductor device package of claim 20, wherein said adhesive material comprises a pressure sensitive adhesive material.

22. The semiconductor device package of claim 17, wherein said thin film is located adjacent a backside of said semiconductor device.

23. The semiconductor device package of claim 15, wherein said interposer further includes at least one contact area on a first surface thereof, proximate said receptacle, said at least one contact area corresponding to at least one bond pad of said semiconductor device.

24. The semiconductor device package of claim 23, wherein said interposer further includes at least one terminal on said first surface and in communication with said at least one contact area.

25. The semiconductor device package of claim 24, wherein said interposer includes a plurality of contact areas and corresponding terminals, said terminals being arranged over said first surface in an array.

26. The semiconductor device package of claim 24, wherein said interposer further includes at least one secondary terminal on a second surface of said substrate, opposite said first surface, said at least one secondary terminal corresponding to at least one other contact area on said first surface.

27. The semiconductor device package of claim 24, further comprising at least one conductive structure secured to and protruding from said at least one terminal.

28. The semiconductor device package of claim 23, further comprising at least one intermediate conductive element electrically connecting said at least one bond pad to said at least one contact area.

29. The semiconductor device package of claim 28, wherein said quantity of encapsulant material encapsulates said at least one intermediate conductive element.

30. The semiconductor device package of claim 15, wherein said quantity of encapsulant material substantially fills said receptacle.

31. The semiconductor device package of claim 15, wherein said quantity of encapsulant material at least partially covers said active surface of said semiconductor device.

32. The semiconductor device package of claim 15, wherein said quantity of encapsulant material laterally confines said semiconductor device within said receptacle.

33. A method for assembling a ball grid array-type semiconductor device package, comprising:

providing an interposer with a substantially planar substrate, a receptacle formed substantially through said substantially planar substrate, and a temporary support element located over at least a portion of one opening of the receptacle;

positioning at least one semiconductor device within said receptacle, with a back side of the at least one semiconductor device contacting said temporary support element;

electrically connecting said at least one semiconductor device to said interposer;

introducing encapsulant material into said receptacle so as to extend laterally between at least a portion of an outer periphery of said at least one semiconductor device and a periphery of said receptacle, said encapsulant material at least laterally confining said at least one semiconductor device within said receptacle; and

removing the temporary support element so as to expose at least a portion of a back side of said at least one semiconductor device.

34. The method of claim 33, wherein said introducing comprises substantially filling said receptacle with encapsulant material.

35. The method of claim 33, wherein said introducing includes introducing encapsulant material over at least a portion of an active surface of said at least one semiconductor device.

36. The method of claim 33, wherein said providing comprises providing an interposer with a thin film covering at least a portion of a bottom end of said receptacle.

37. The method of claim 36, wherein said positioning comprises positioning said at least one semiconductor device on said thin film.

38. The method of claim 37, wherein said positioning comprises positioning a back side of said semiconductor device against said thin film.

39. The method of claim 37, wherein said positioning comprises securing said at least one semiconductor device to said thin film.

40. The method of claim 36, further comprising removing said thin film following said introducing.

41. The method of claim 33, wherein said positioning comprising positioning a plurality of semiconductor devices within said receptacle.

42. The method of claim 33, wherein said electrically connecting comprises positioning an intermediate conductive element between at least one bond pad of said at least one semiconductor device and a corresponding contact area of said interposer.

43. The method of claim 42, wherein said positioning said intermediate conductive element comprises connecting a bond wire between said at least one bond pad and said corresponding contact area.

44. The method of claim 33, further comprising placing a conductive structure on at least one terminal of said interposer.

45. A ball grid array-type semiconductor device package, comprising:
an interposer including:
a substrate; and
a receptacle formed substantially through said substrate, said substrate substantially completely laterally confining said receptacle;
at least one semiconductor device positioned within said receptacle, at least a portion of a back side of said at least one semiconductor device being exposed through the interposer; and
at least one intermediate conductive element electrically connecting at least one bond pad of said at least one semiconductor device to a corresponding contact area of said interposer.

46. The semiconductor device package of claim 45, further comprising at least one contact pad in communication with said at least one contact area.

47. The semiconductor device package of claim 46, further comprising at least one conductive structure secured to and protruding from said at least one contact pad.

48. A ball grip array-type semiconductor device package, comprising:
an interposer including:
a substrate; and
a receptacle formed within said substrate, said receptacle extending substantially through a thickness of said substrate; and
a semiconductor device suspended with said receptacle and including a back side exposed to an exterior of the semiconductor device package.

49. The semiconductor device package of claim 48, further comprising a quantity of encapsulant material extending laterally between at least a portion of an outer periphery of said semiconductor device and a periphery of said receptacle, said quantity of encapsulant material at least partially retaining said semiconductor device within said receptacle.

50. The semiconductor device package of claim 48, wherein said interposer further includes at least one contact area on a first surface thereof, proximate said receptacle, said at least one contact area corresponding to at least one bond pad of said semiconductor device.

51. The semiconductor device package of claim 50, wherein said interposer further includes at least one terminal on said first surface and in communication with said at least one contact area.

52. The semiconductor device package of claim 51, wherein said interposer includes a plurality of contact areas and corresponding terminals, said terminals being arranged over said first surface in an array.

53. The semiconductor device package of claim 51, wherein said interposer further includes at least one secondary terminal on a second surface of said substrate, opposite said first

surface, said at least one secondary terminal corresponding to at least one other contact area on said first surface.

54. The semiconductor device package of claim 51, further comprising at least one conductive surface secured to and protruding from said at least one terminal.

55. The semiconductor device package of claim 50, further comprising at least one intermediate conductive element electrically connecting said at least one bond pad to said at least one contact area.

56. The semiconductor device package of claim 55, wherein said at least one intermediate conductive element is encapsulated.

57. The semiconductor device package of claim 49, wherein said quantity of encapsulant material substantially fills said receptacle.

58. The semiconductor device package of claim 49, wherein said quantity of encapsulant material at least partially covers said active surface of said semiconductor device.