WHAT IS CLAIMED IS:

1. A method of fabricating a memory device, comprising:

providing a substrate;

forming a memory cell material stack over the substrate, the memory cell including a first active material and a second active material over the first active material, wherein one of the first and second active materials comprises a storage material and the other of the first and second active materials comprises a selector material;

patterning the memory cell material stack, wherein patterning includes:

etching through the one of the first and second active materials of the memory cell material stack,

forming protective liners on sidewalls of the at least one of the first and second active materials after etching through the one of the first and second active materials, and

further etching through the other of the first and second active materials of the memory cell material stack after forming the protective liners.

2. The method of Claim 1, wherein forming the protective liners comprises forming liners formed of fluorocarbons.

3. The method of Claim 1, wherein forming the protective liners comprises depositing fluorocarbons using plasma and fluorocarbon reactants including C and F.

4. The method of Claim 1, wherein forming the protective liners comprises depositing and etching fluorocarbons using plasma to form a spacer structure.

5. The method of Claim 1, wherein forming the protective liners comprises depositing in a dry etch chamber using plasma.

6. The method of Claim 5, wherein depositing the protective liners is performed without applying an external bias to the substrate.

7. The method of Claim 5, wherein etching through the at least one of the first and second active materials and forming the protective liners are performed in-situ in the dry etch chamber.

8. The method of Claim 7, wherein further etching through the other of the first and second active materials is performed in-situ in the dry etch chamber.

9. The method of Claim 1, wherein etching through the at least one of first and second active material defines a plurality of partially etched lines, and forming the protective liners comprises depositing a thickness between about 5% and about 25% of a width of the partially etched lines at the same vertical height.

10. The method of Claim 1, wherein further etching through the other of the first and second active materials comprises spacer-etching the protective liners to leave protective liner spacers on the side walls of the one of first and second active materials.

11. The method of Claim 1, further comprising, after further etching the memory cell material stack, removing the protective liners from the sidewalls of the one of first and second active materials.

12. The method of Claim 11, further comprising, after further etching the memory cell material stack, forming a dielectric sealing liner on sidewalls of the one of first and second active materials and on sidewalls of the other of the first and second active materials.

13. The method of Claim 1, further comprising, after further etching the memory cell material stack, filling a gap adjacent the memory cell material stack with a gap fill dielectric.

14. The method of Claim 1, wherein the memory device is a phase change memory device, and wherein the first active material comprises a first chalcogenide composition and the second active material comprises a second chalcogenide composition.

15. The method of Claim 14, wherein the one of first and second active materials comprises the storage element and the other of the first and second active materials comprises the selector element, wherein the selector element comprises at least one of As and Se.

16. The method of Claim 1,

wherein the memory cell material stack further includes a lower electrode material, a middle electrode material, and an upper electrode material, wherein the first active material is interposed between the upper electrode material and the middle electrode material, and wherein the second active material is interposed between the lower electrode material and the middle electrode material,

wherein etching through the at least at least one of the first and second active materials further includes stopping in the middle electrode material to expose at least a portion of sidewalls of the middle electrode material,

wherein forming protective liners further includes forming the protective liners on the at least a portion of sidewalls of the middle electrode material, and

wherein further etching further includes etching a remaining portion of the middle electrode material after forming the protective liners and further includes etching the lower electrode material after etching through the other of the first and second active materials and stopping on a conductive material.

17. The method of Claim 1, wherein patterning the memory cell stack comprises forming a lower line stack extending in a first direction, the lower line stack comprising a first active material line over the substrate and a second active material line over the first material line.

18. The method of Claim 17, further comprising:

after further etching though the other of the first and second active materials to form the lower line stack, further patterning the memory cell material stack to form an upper wall structure extending in a second direction crossing the first direction, further patterning comprising:

etching through the one of the first and second active material lines of the lower line stack,

forming second protective liners on sidewalls of the at least one of the first and second active material lines after etching through the one of the first and second active material lines, and

further etching through the other of the first and second active material lines of the memory cell material stack after forming the second protective liners.

19. A method of fabricating a memory device, comprising:

providing a substrate;

forming a memory cell material stack;

patterning the memory cell material stack to form a memory cell structure stack, comprising:

partially etching the memory cell material stack to form a shallow trench separating upper portions of the memory cell material stack,

forming a protective liner material on sidewall and bottom surfaces of the shallow trench,

anisotropically etching the protective liner material to remove the protective liner material from the bottom surface of the shallow trench to form a protective liner spacer on sidewall surfaces of the upper portion, and

further etching the memory cell material stack to separate the memory cell material stack into memory cell line stacks after forming the protective liner spacer.

20. The method of Claim 19, wherein forming the memory cell material stack comprises:

forming a conductive material over the substrate;

forming a selector material over the conductive material; and

forming a storage material over the selector material,

wherein partially etching etches through the storage material without etching through the conductive material, and further etching etches through the conductive material.

21. The method of Claim 20, wherein partially etching etches stops on or in an electrode material separating the selector material from the storage material; and further etching etches through a remainder of the electrode material and the selector material.

22. The method of Claim 20, wherein patterning the memory cell material stack includes patterning a cell material line stack extending in a first direction, the method further comprising further patterning the memory stack to form a wall structure extending in a second direction crossing the first direction, the wall structure including a column line above the storage material.

23. The method of Claim 22, wherein further patterning comprises:

partially etching the cell material line stack to form a second shallow trench separating upper portions of the wall structure,

forming a protective liner material on sidewall and bottom surfaces of the second shallow trench,

anisotropically etching the protective liner material to remove the protective liner material from the bottom surface of the second shallow trench to form a second protective liner spacer on sidewall surfaces of the upper portion, and

further etching the cell material line stack to separate the memory cell material stack into a memory cell pillar stack after forming the second protective liner spacer.

24. A memory device, comprising:

a substrate;

a lower conductive line disposed above the substrate and extending in a first direction and an upper conductive line disposed above the lower conductive line and extending in the second direction crossing the first direction; and

a memory cell stack interposed between the lower and upper conductive lines, the memory cell stack comprising an upper active element and a lower active element, wherein the memory cell stack includes lateral plateau regions when viewed in the first direction such that a width of the memory cell stack immediately below the plateau regions are between about 10% and 50% wider than a width of the memory cell stack immediately above the plateau regions.

25. The memory device of Claim 24, wherein the memory cell stack further comprises an upper electrode between the upper active element and the upper conductive line, a middle electrode between the upper and lower active elements, and a lower electrode between the lower active element and the lower conductive line.

26. The memory device of Claim 25, wherein the lateral plateau regions are formed below the upper active element.

27. The memory device of Claim 25, wherein the lateral plateau regions are formed below the lower active element and above the lower conductive line.

28. The memory device of Claim 26, further comprising a second lateral plateau region formed between the upper active element and the lower active element.

WHAT IS CLAIMED IS:

1. A method of fabricating a memory device, comprising:

providing a substrate;

forming a memory cell material stack over the substrate, the memory cell including a first active material and a second active material over the first active material, wherein one of the first and second active materials comprises a storage material and the other of the first and second active materials comprises a selector material;

patterning the memory cell material stack, wherein patterning includes:

etching through the one of the first and second active materials of the memory cell material stack;

forming protective liners on sidewalls of the at least one of the first and second active materials after etching through the one of the first and second active materials, wherein the protective liners comprise a conformal liner material deposited on the sidewalls, and

further etching through the other of the first and second active materials of the memory cell material stack after forming the protective liners,

wherein patterning the memory cell stack comprises forming a lower line stack extending in a first direction, the lower line stack comprising a first active material line over the substrate and a second active material line over the first material line.

2. The method of Claim 1, wherein forming the protective liners comprises forming liners formed of fluorocarbons.

3. The method of Claim 1, wherein forming the protective liners comprises depositing fluorocarbons using plasma and fluorocarbon reactants including C and F.

4. The method of Claim 1, wherein forming the protective liners comprises depositing and etching fluorocarbons using plasma to form a spacer structure.

5. The method of Claim 1, wherein forming the protective liners comprises depositing in a dry etch chamber using plasma.

6. The method of Claim 5, wherein depositing the protective liners is performed without applying an external bias to the substrate.

7. The method of Claim 5, wherein etching through the at least one of the first and second active materials and forming the protective liners are performed in-situ in the dry etch chamber.

8. The method of Claim 7, wherein further etching through the other of the first and second active materials is performed in-situ in the dry etch chamber.

9. A method of fabricating a memory device, comprising:

providing a substrate;

forming a memory cell material stack over the substrate, the memory cell including a first active material and a second active material over the first active material, wherein one of the first and second active materials comprises a storage material and the other of the first and second active materials comprises a selector material;

patterning the memory cell material stack, wherein patterning includes:

etching through the one of the first and second active materials of the memory cell material stack;

forming protective liners on sidewalls of the at least one of the first and second active materials after etching through the one of the first and second active materials, and

further etching through the other of the first and second active materials of the memory cell material stack after forming the protective liners,

wherein etching through the at least one of first and second active material defines a plurality of partially etched lines, and forming the protective liners comprises depositing a thickness between about 5% and about 25% of a width of the partially etched lines at the same vertical height.

10. The method of Claim 1, wherein further etching through the other of the first and second active materials comprises spacer-etching the protective liners to leave protective liner spacers on the side walls of the one of first and second active materials.

11. The method of Claim 1, further comprising, after further etching the memory cell material stack, removing the protective liners from the sidewalls of the one of first and second active materials.

12. The method of Claim 11, further comprising, after further etching the memory cell material stack, forming a dielectric sealing liner on sidewalls of the one of first and second active materials and on sidewalls of the other of the first and second active materials.

13. The method of Claim 1, further comprising, after further etching the memory cell material stack, filling a gap adjacent the memory cell material stack with a gap fill dielectric.

14. The method of Claim 1, wherein the memory device is a phase change memory device, and wherein the first active material comprises a first chalcogenide composition and the second active material comprises a second chalcogenide composition.

15. The method of Claim 14, wherein the one of first and second active materials comprises the storage element and the other of the first and second active materials comprises the selector element, wherein the selector element comprises at least one of As and Se.

16. The method of Claim 1,

wherein the memory cell material stack further includes a lower electrode material, a middle electrode material, and an upper electrode material, wherein the first active material is interposed between the lower electrode material and the middle electrode material, and wherein the second active material is interposed between the upper electrode material and the middle electrode material,

wherein etching through the at least one of the first and second active materials further includes stopping in the middle electrode material to expose at least a portion of sidewalls of the middle electrode material,

wherein forming protective liners further includes forming the protective liners on the at least a portion of sidewalls of the middle electrode material, and

wherein further etching further includes etching a remaining portion of the middle electrode material after forming the protective liners and further includes etching the lower electrode material after etching through the other of the first and second active materials and stopping on a conductive material.

17. The method of Claim 1, further comprising:

after further etching through the other of the first and second active materials to form the lower line stack, further patterning the memory cell material stack to form an upper wall structure extending in a second direction crossing the first direction, further patterning comprising:

etching through the one of the first and second active material lines of the lower line stack,

forming second protective liners on sidewalls of the at least one of the first and second active material lines after etching through the one of the first and second active material lines, and

further etching through the other of the first and second active material lines of the memory cell material stack after forming the second protective liners.

18. A method of fabricating a memory device, comprising:

providing a substrate;

forming a memory cell material stack;

patterning the memory cell material stack to form a memory cell structure stack, comprising:

partially etching the memory cell material stack to form a shallow trench separating upper portions of the memory cell material stack,

forming a protective liner material on sidewall and bottom surfaces of the shallow trench, wherein the protective liner material comprises a conformal liner material deposited on the sidewall and the bottom surfaces of the shallow trench,

anisotropically etching the protective liner material to remove the protective liner material from the bottom surface of the shallow trench to form a protective liner spacer on sidewall surfaces of the upper portion, and

further etching the memory cell material stack to separate the memory cell material stack into memory cell line stacks after forming the protective liner spacer.

19. The method of Claim 18, wherein forming the memory cell material stack comprises:

forming a conductive material over the substrate;

forming a selector material over the conductive material; and

forming a storage material over the selector material,

wherein partially etching etches through the storage material without etching through the conductive material, and further etching etches through the conductive material.

20. The method of Claim 19, wherein partially etching etches stops on or in an electrode material separating the selector material from the storage material; and further etching etches through a remainder of the electrode material and the selector material.

21. The method of Claim 19, wherein patterning the memory cell material stack includes patterning a cell material line stack extending in a first direction, the method further comprising further patterning the memory stack to form a wall structure extending in a second direction crossing the first direction, the wall structure including a column line above the storage material.

22. The method of Claim 21, wherein further patterning comprises:

partially etching the cell material line stack to form a second shallow trench separating upper portions of the wall structure,

forming a protective liner material on sidewall and bottom surfaces of the second shallow trench,

anisotropically etching the protective liner material to remove the protective liner material from the bottom surf ace of the second shallow trench to form a second protective liner spacer on sidewall surfaces of the upper portion, and

further etching the cell material line stack to separate the memory cell material stack into a memory cell pillar stack after forming the second protective liner spacer.

23. A memory device, comprising:

a substrate;

a lower conductive line disposed above the substrate and extending in a first direction and an upper conductive line disposed above the lower conductive line and extending in the second direction crossing the first direction; and

a memory cell stack interposed between the lower and upper conductive lines, the memory cell stack comprising an upper active element and a lower active element, wherein the memory cell stack includes lateral plateau regions when viewed in the first direction such that a width of the memory ceil stack immediately below the plateau regions are between about 10% and 50% wider than a width of the memory cell stack immediately above the plateau regions.

24. The memory device of Claim 23, wherein the memory cell stack further comprises an upper electrode between the upper active element and the upper conductive line, a middle electrode between the upper and lower active elements, and a lower electrode between the lower active element and the lower conductive line.

25. The memory device of Claim 24, wherein the lateral plateau regions are formed below the upper active element.

26. The memory device of Claim 24, wherein the lateral plateau regions are formed below the lower active element and above the lower conductive line.

27. The memory device of Claim 25, further comprising a second lateral plateau region formed between the upper active element and the lower active element.