

DESCRIPTION

**HOLDING CIRCUIT, DRIVING METHOD OF THE HOLDING CIRCUIT, AND
SEMICONDUCTOR DEVICE INCLUDING THE HOLDING CIRCUIT**

5

TECHNICAL FIELD

[0001]

One embodiment of the present invention relates to a holding circuit, a sequential circuit, and other semiconductor devices capable of holding a state or data, a driving method thereof, a manufacturing method thereof, and the like.

[0002]

One embodiment of the present invention is not limited to the above technical field. The technical field of one embodiment of the invention disclosed in the specification, the drawings, and the claims (hereinafter referred to as "this specification and the like") relates to an object, a method, or a manufacturing method. One embodiment of the present invention relates to a process, a machine, manufacture, or a composition of matter. Examples of the technical field of one embodiment of the present invention disclosed in this specification include a semiconductor device, a display device, a liquid crystal display device, a light-emitting device, a lighting device, a power storage device, a memory device, a processing device, a method for driving any of them, and a method for manufacturing any of them.

BACKGROUND ART

[0003]

To reduce the power consumption of a semiconductor device, unnecessary operation of circuits is stopped by power gating or clock gating. A flip-flop circuit (FF) is a sequential circuit (memory circuit that holds a state) included a lot in a semiconductor device. Thus, a reduction in power consumption of the FF leads to a reduction in power consumption of the whole semiconductor device incorporating the FF. When a general FF is simply powered off, a state (data) held therein is lost.

[0004]

By taking advantage of an extremely low off-state current of a transistor whose

semiconductor region is formed using an oxide semiconductor layer (hereinafter, such a transistor may be referred to as an OS transistor), a holding circuit capable of holding a state (data) even when powered off has been proposed. According to Patent Documents 1 to 3, for example, an FF incorporates a holding circuit including an OS transistor, leading to power gating of the FF.

[Reference]

[Patent Document]

[0005]

[Patent Document 1] Japanese Published Patent Application No. 2012-257192

10 [Patent Document 2] Japanese Published Patent Application No. 2013-009297

[Patent Document 3] Japanese Published Patent Application No. 2013-175708

DISCLOSURE OF INVENTION

[0006]

15 An object of one embodiment of the present invention is to provide a novel holding circuit, a novel sequential circuit, another novel semiconductor device, a novel driving method thereof, or a novel manufacturing method thereof. An object of one embodiment is, for example, to provide a semiconductor device whose power consumption can be reduced or a semiconductor device whose overhead can be prevented from being increased.

[0007]

Objects other than the above objects will be apparent from the description in this specification and the like, and other objects of embodiments of the present invention can be extracted. In the descriptions of a plurality of objects, one object does not preclude the existence of another object. In addition, there is no need for one embodiment of the present invention to achieve all the objects.

[0008]

One embodiment of the present invention is a holding circuit including a first input terminal, a second input terminal, a third input terminal, a first output terminal, a first switch, a second switch, a third switch, a capacitor, and a first node. The first switch controls conduction between the first node and the first input terminal. The second switch controls conduction between the first node and the first output terminal.

The third switch controls conduction between the second input terminal and the first output terminal. A first terminal of the capacitor is electrically connected to the first node. A second terminal of the capacitor is electrically connected to the third input terminal. The first and second switches are each a transistor whose semiconductor region is formed using an oxide semiconductor layer.

[0009]

In the above structure, the third switch may be a transistor whose semiconductor region is formed using an oxide semiconductor layer. In that case, the oxide semiconductor layer preferably includes a crystal part with c-axis alignment.

[0010]

In this specification and the like, ordinal numbers such as first, second, and third are used to avoid confusion among components, and the terms do not limit the components numerically.

[0011]

In this specification and the like, a semiconductor device refers to a device that utilizes semiconductor characteristics, and means a circuit including a semiconductor element (e.g., a transistor or a diode), a device including the circuit, and the like. The semiconductor device also means any device that can function by utilizing semiconductor characteristics. For example, an integrated circuit and a chip including an integrated circuit are all semiconductor devices. Moreover, a memory device, a display device, a light-emitting device, a lighting device, an electronic device, and the like themselves might be semiconductor devices, or might each include a semiconductor device.

[0012]

A transistor includes three terminals called a gate, a source, and a drain. The gate serves as a control terminal for controlling the on/off of the transistor. A pair of terminals other than the gate serves as input and output terminals of the transistor; one serves as a source and the other serves as a drain depending on the conductivity type of the transistor and potentials applied to the three terminals of the transistor. In general, in an n-channel transistor, a terminal to which a lower potential is applied is called a source, and a terminal to which a higher potential is applied is called a drain. In contrast, in a p-channel transistor, a terminal to which a lower potential is applied is

called a drain, and a terminal to which a higher potential is applied is called a source. Thus, the functions of two terminals other than the gate might interchange depending on the potentials input to the three terminals of the transistor. For this reason, in this specification and the like, one of two terminals serving as a source and a drain of a transistor is called a first terminal and the other is called a second terminal, in some cases.

[0013]

In this specification, to clarify a circuit configuration and circuit operation, one of input and output terminals of a transistor is fixed as a source and the other is fixed as a drain in some cases. It is needless to say that, depending on a driving method, the magnitude relationship between potentials applied to three terminals of the transistor might be changed, and the source and the drain might be interchanged. Thus, in one embodiment of the present invention, the distinction between the source and drain of the transistor is not limited to that described in this specification and the drawings.

[0014]

One embodiment of the present invention can provide a novel holding circuit, a novel sequential circuit, another novel semiconductor device, a novel driving method thereof, or a novel manufacturing method thereof. As a result, for example, power consumption of a semiconductor device can be reduced. Alternatively, area overhead and performance overhead due to addition of a function of holding data in power gating can be reduced. For example, area overhead or performance overhead can be zero.

[0015]

The description of these effects does not preclude the existence of other effects. In one embodiment of the present invention, there is no need to achieve all the effects. Furthermore, one embodiment of the present invention is not limited by these effects. For example, depending on circumstances or conditions, one embodiment of the present invention might not produce these effects or might produce an effect other than these effects. In one embodiment of the present invention, an object other than the above objects, an effect other than the above effects, and a novel structure will be apparent from the description in the specification and the like.

BRIEF DESCRIPTION OF DRAWINGS

[0016]

FIG. 1 is a block diagram illustrating a configuration example of a semiconductor device.

FIG. 2 is a circuit diagram illustrating a configuration example of a semiconductor device.

FIG. 3 is a timing chart showing an example of a method for driving a semiconductor device.

FIG. 4 is a timing chart showing an example of a method for driving a semiconductor device.

FIG. 5 is a block diagram illustrating a configuration example of a semiconductor device.

FIGS. 6A and 6B are each a block diagram illustrating a configuration example of a semiconductor device.

FIG. 7 is a block diagram illustrating a configuration example of a semiconductor device.

FIGS. 8A to 8D illustrate a structure example of an OS transistor; FIG. 8A is a top view, FIG. 8B is a cross-sectional view taken along line y1-y2, FIG. 8C is a cross-sectional view taken along line x1-x2, and FIG. 8D is a cross-sectional view taken along line x3-x4.

FIGS. 9A to 9D illustrate a structure example of an OS transistor; FIG. 9A is a top view, FIG. 9B is a cross-sectional view taken along line y1-y2, FIG. 9C is a cross-sectional view taken along line x1-x2, and FIG. 9D is a cross-sectional view taken along line x3-x4.

FIGS. 10A and 10B are a partial enlarged view of FIG. 8B and an energy band diagram of an OS transistor, respectively.

FIG. 11 is a cross-sectional view illustrating a structure example of a semiconductor device.

FIG. 12 is a block diagram illustrating an example of a processing unit (CPU).

FIGS. 13A and 13B are a flow chart showing an example of a method for manufacturing an electronic component and a diagram illustrating a structure example of an electronic component, respectively.

FIGS. 14A to 14F each illustrate a structure example of an electronic device.

BEST MODE FOR CARRYING OUT THE INVENTION

[0017]

Embodiments of the present invention will be described in detail with reference to drawings. Note that the present invention is not limited to the following descriptions and it will be readily appreciated by those skilled in the art that modes and details can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the present invention should not be construed as being limited to the descriptions of the embodiments below.

[0018]

In addition, the same portions or portions having similar functions in the drawings used for the description of embodiments of the present invention are denoted by the same reference numerals, and the description thereof is not repeated in some cases.

[0019]

In this specification, for example, clock signal CLK is abbreviated to a "signal CLK", "CLK", or the like in some cases. The same applies to other components (e.g., signal, voltage, potential, circuit, element, electrode, and wiring).

[0020]

Some embodiments will be described below. A structure described in one embodiment can be combined with any of those described in the other embodiments as appropriate. In addition, in the case where some structure examples are described in one embodiment, any of the structure examples can be combined as appropriate.

[0021]

(Embodiment 1)

<<Configuration Example 1 of Semiconductor Device>>

FIG. 1 is a block diagram illustrating a configuration example of a semiconductor device. A semiconductor device 100 includes an input terminal INa, an input terminal INb, an output terminal OUTa, a circuit 10, and a circuit RC1. The terminals INa and INb can input a data signal to be processed by the semiconductor device 100. The terminal OUTa outputs a data signal processed by the semiconductor device 100 (the circuit 10).

[0022]

<Circuit 10>

The circuit 10 includes a circuit 20 and a circuit 30. The circuit 10 is a semiconductor device that can serve as a logic circuit. A control signal such as a clock signal CLK, a high power supply potential VDD, and a low power supply potential VSS are input to the circuit 10. The circuit 10 is a circuit block that can use clock gating and power gating. The supply of the clock signal CLK is controlled by a clock gating circuit of a semiconductor device in which the semiconductor device 100 is incorporated, and the supply of the power supply potential VDD is controlled by a power gating circuit of the semiconductor device.

[0023]

The circuit 20 can serve as a selection circuit, and has a function of selecting one of an input signal from an input terminal a20 and an input signal from an input terminal a21 to output from an output terminal b20. The terminal a20 is electrically connected to the terminal INa, the terminal a21 is electrically connected to an output terminal b1 of the circuit RC1, and the terminal b20 is electrically connected to an input terminal a30 of the circuit 30. An output terminal b30 of the circuit 30 is electrically connected to the terminal OUTa.

[0024]

The circuit 30 can be a circuit capable of holding data (state). A typical example of the circuit 30 is a sequential circuit. In that case, a logic level of a data signal output from the terminal b30 is determined by a data signal input to the terminal a30 or by the data signal and data (state) held in the circuit 30. The circuit 30 can be, for example, a sequential circuit such as a latch circuit, a flip-flop circuit, a shift register, a counter circuit, or a divider circuit.

[0025]

<Circuit RC1>

The circuit RC1 serves as a holding circuit capable of holding data (state). The circuit RC1 includes a node FN1, an input terminal a1, an input terminal a2, an input terminal c1, the output terminal b1, a switch SW1, a switch SW2, a switch SW3, and a capacitor CP1.

[0026]

The node FN1 is provided such that it can be electrically floating, and is a node serving as a data (state) holding portion of the circuit RC1. The terminal a1 is electrically connected to the terminal INa and the terminal a2 is electrically connected to the terminal INb.

5 [0027]

The switch SW1 can control conduction between the node FN1 and the terminal a1. The switch SW2 can control conduction between the node FN1 and the terminal b1. The switch SW3 can control conduction between the terminal a2 and the terminal b1. A first terminal and a second terminal of the capacitor CP1 are
10 electrically connected to the node FN1 and the terminal c1, respectively. The node FN1 and the terminal c1 are capacitively coupled by the capacitor CP1. Thus, the potential of the node FN1 can be controlled by the potential of the terminal c1. When the node FN1 is electrically floating, for example, an increase in the potential of the terminal c1 can boost the potential of the node FN1.

15 [0028]

The circuit RC1 has a function of selecting one of data input from the terminal a1 and data input from the terminal a2 and holding the selected data in the node FN1, and a function of outputting data held in the node FN1 from the terminal b1. For writing of data input from the terminal a1, the switch SW1 is turned on and the switches
20 SW2 and SW3 are turned off. For writing of data input from the terminal a2, the switches SW2 and SW3 are turned on and the switch SW1 is turned off. For data reading, the switch SW2 is turned on and the switches SW1 and SW3 are turned off. For data holding, the switches SW1 and SW2 are turned off and the node FN1 is made electrically floating.

25 [0029]

The electrostatic capacitance of the capacitor CP1 is set considering the load of a node (node corresponding to the terminal a30 in the case of FIG. 1) to which data held in the RC1 is written.

[0030]

30 The circuit RC1 can serve as a backup memory circuit for data held in the circuit 10. For this reason, the circuit RC1 has retention characteristics such that stored data can be held while powered off. To hold data in the RC1 for a long time, a

potential change (in particular, a potential drop) of the electrically floating node FN1 is preferably reduced as much as possible. A means of achieving this is to use a transistor with extremely low drain current in an off state (off-state current) as each of the switches SW1 and SW2.

5 [0031]

To reduce off-state current of a transistor, a semiconductor region contains a semiconductor with a wide energy gap, for example. In that case, the energy gap of the semiconductor is preferably greater than or equal to 2.5 eV, greater than or equal to 2.7 eV, or greater than or equal to 3 eV. An example of such a semiconductor is an
10 oxide semiconductor. The switches SW1 and SW2 are each a transistor (OS transistor) whose semiconductor region is formed using an oxide semiconductor layer, for example. The leakage current of an OS transistor normalized on the channel width can be, for example, lower than or equal to 10×10^{-21} A/ μ m (10 zA/ μ m) with a source-drain voltage of 10 V at room temperature (approximately 25 °C). It is preferred that the
15 leakage current of the OS transistor used as each of the switches SW1 and SW2 be lower than or equal to 1×10^{-18} A, lower than or equal to 1×10^{-21} A, or lower than or equal to 1×10^{-24} A at room temperature (approximately 25 °C). Alternatively, the leakage current is preferably lower than or equal to 1×10^{-15} A, lower than or equal to 1×10^{-18} A, or lower than or equal to 1×10^{-21} A at 85 °C.

20 [0032]

Avalanche breakdown or the like is less likely to occur in some cases in an OS transistor than in a general transistor including silicon or the like, because an oxide semiconductor has a wide energy gap and thus electrons are less likely to be excited, and the effective mass of a hole is large. Since hot-carrier degradation or the like due
25 to the avalanche breakdown is inhibited, the OS transistor has high drain withstand voltage and can be driven at high drain voltage. Accordingly, the use of the OS transistor in the circuit RC1 can leave a wide margin for driving conditions such as the potential level of a signal and input timing. The circuit RC1 can be driven such that the potential of the node FN1 is high when data is held, for example.

30 [0033]

Furthermore, the OS transistor can have excellent off-state current

characteristics and subthreshold characteristics even with a gate insulating layer with an equivalent oxide thickness of about 11 nm and a short channel length of 50 nm. Since a gate insulating layer in the OS transistor can be thicker than that in a Si transistor generally used in a logic circuit, leakage current through the gate insulating layer can be reduced and a variation in electric characteristics due to a variation in the thickness of the gate insulating layer can be suppressed. The details of the OS transistor will be described in Embodiment 2.

[0034]

There is no particular limitation on the switch SW3 and a transistor included in the circuit 10, and a general transistor included in a logic circuit can be used; for example, a transistor whose semiconductor region contains a Group 4 element (Si, Ge, or C) can be used. A typical example of the transistor in the circuit 10 is a transistor whose semiconductor region contains silicon (Si transistor). For the purpose of improving the mobility of the Si transistor or for other purposes, a distortion transistor obtained by addition of Ge to a semiconductor region of a Si transistor may be used.

[0035]

The switch SW3 may be an OS transistor like the switches SW1 and SW2, or a switch circuit such as an analog switch. When an OS transistor is used as the switch SW3, area overhead of the semiconductor device 100 due to addition of the circuit RC1 can be zero as described below. In contrast, when an analog switch is used as the switch SW3, a Si transistor is used for a p-channel transistor, an OS transistor is used for an n-channel transistor, and the n-channel transistor is stacked over the p-channel transistor, in which case the area of the semiconductor device 100 can be reduced as compared to the case where the switch SW3 is formed using only Si transistors.

[0036]

In the semiconductor device 100, a change in the circuit configuration of the circuits 20 and 30 due to the provision of the circuit RC1 is unnecessary. Furthermore, a general selection circuit such as a selector or a multiplexer can be used as the circuit 20. In addition, a general sequential circuit such as a latch circuit or a flip-flop circuit can be used as the circuit 30. Since the circuit RC1 can be stacked over the circuits 20 and 30, the circuit RC1 can be provided almost without a layout change of the circuits 20 and 30. In this embodiment, a circuit block including an OS transistor is stacked

over a circuit block including a selection circuit and a sequential circuit, whereby area overhead due to the addition of the circuit block including an OS transistor and a performance penalty during normal operation of the selection circuit and the sequential circuit can be zero.

5 [0037]

Examples of specific circuit configuration and a driving method of the semiconductor device 100 will be described below.

[0038]

<<Configuration Example 2 of Semiconductor Device>>

10 FIG. 2 is a circuit diagram illustrating a configuration example of a semiconductor device. FIG. 3 and FIG. 4 are each a timing chart showing examples of a driving method of the semiconductor device illustrated in FIG. 2. The circuit diagram in FIG. 2 is a specific example of the semiconductor device 100 illustrated in FIG. 1. A semiconductor device 101 illustrated in FIG. 2 includes a circuit 11 and a
15 circuit RC2.

[0039]

The circuit 11 is a circuit block corresponding to the circuit 10 in FIG. 1. The circuit 11 includes a circuit SELC1 and a flip-flop circuit (FF) 31.

[0040]

20 The SELC1 can serve as a selection circuit and includes one inverter (NOT gate) circuit and two analog switch circuits. To the SELC1, a signal SEL as a control signal and power supply potentials VDD and VSS are input.

[0041]

To the FF 31, a clock signal CLK and a reset signal RESET are input as control
25 signals and VDD and VSS are input as power supply potentials. A signal CLKB is an inverted signal of CLK and is generated from CLK by an inverter circuit or the like provided in the circuit 11. In FIG. 2, the FF 31 is a master-slave FF and includes two latch circuits (LATA and LATb). The LATA includes one analog switch, one NAND gate circuit, and one clocked inverter circuit. The LATb includes one analog switch,
30 one inverter circuit, and one clocked NAND gate circuit. In the FF 31, one analog switch and one inverter circuit may be provided instead of the clocked inverter circuit, and one analog switch and a NAND gate circuit may be provided instead of the clocked

NAND gate circuit.

[0042]

The circuit RC2 corresponds to the circuit RC1 in FIG. 1. A transistor Mos1, a transistor Mos2, and a transistor Mos3 serving as SW1, SW2, and SW3, respectively, are n-channel transistors and OS transistors. Signals OG1 to OG3 are control signals for controlling on/off of the transistors Mos1 to Mos3. A signal CSB is input to a second terminal of the capacitor CP1.

[0043]

The semiconductor device 101 illustrated in FIG. 2 can serve as a scan flip-flop circuit, for example, and a plurality of semiconductor devices 101 can form a scan chain. In that case, the terminal INa is used as a data input terminal for normal operation and the terminal INb is used as an input portion of the scan chain. To form a scan chain, the input terminal INb of one of adjacent two semiconductor devices 101 is electrically connected to the output terminal OUTa of the other semiconductor device 101. The input terminal INa of each of the plurality of semiconductor devices 101 is connected to an output terminal of a combinational circuit.

[0044]

The semiconductor device 101 can be used as, for example, a logic element of a programmable logic device (PLD) such as an FPGA. A circuit block having a register included in the logic element and a selection circuit for selecting an input signal of the register may be formed using the circuit 11. In that case, a plurality of semiconductor devices 101 can form a register chain having a backup function.

[0045]

The semiconductor device 101 can use clock gating and power gating; thus, supply of CLK and VDD to the circuit 11 can be stopped for a period during the operation of the circuit 11 is unnecessary for the semiconductor device in which the circuit 11 is incorporated. As a result, dynamic power consumption of the semiconductor device 101 can be reduced. Hereinafter, examples of a driving method of the semiconductor device 101 will be described with reference to FIG. 3 and FIG. 4.

[0046]

FIG. 3 and FIG. 4 show waveforms of control signals OG1 to OG3, CSB, CLK, RESET, and SEL, input signals D0 and SC, and an output signal Q0; a potential change

of the node FN1; and a potential change of an input terminal for the power supply potential VDD of the circuit 11. For the signals OG1 to OG3, CSB, CLK, RESET, SEL, D0, and SC input to the semiconductor device 101, a high (H) level potential is VDD and a low (L) level potential is VSS in the examples in FIG. 3 and FIG. 4.

5 [0047]

<<Example 1 of Driving Method of Semiconductor Device>>

FIG. 3 shows an example of a method for controlling clock gating and power gating.

[0048]

10 <Period T1>

In Period T1, the semiconductor device 101 operates in a normal operation mode. In the normal operation, the semiconductor device 101 (circuit 11) operates as a flip-flop circuit. In the example shown in FIG. 3, the semiconductor device 101 in the normal operation operates so that the state of the signal D0 is held in the FF 31.

15 [0049]

Note that VDD and CLK are supplied to the circuit 11. Since the potential of the signal SEL is at an L level, conduction between the terminal INa and the input terminal a30 of the FF 31 are established through the SELC1. The state of the FF 31 (output signal Q0) changes depending on the signal CLK and the signal D0 input from the terminal a30.

20

[0050]

In the normal operation, the potential of the node FN1 is held at a potential at which a logic level becomes "L". Here, the logic level of the node FN1 is held at "L" utilizing the signal SC input from the terminal INb. Specifically, the potential of SC is set at an L level (VSS) and the transistors Mos2 and Mos3 are turned on. Accordingly, the potential of the node FN1 becomes VSS. That is, in the normal operation, the node FN1 is precharged using the signal SC. Note that the L level potential of SC is not limited to VSS; however, when the L level potential of SC is VSS, the signal SC can be generated without increasing the number of kinds of power supply potentials to be used.

25

30 [0051]

<Period T2>

In Period T2, VDD is supplied but CLK is not supplied, whereby the

semiconductor device 101 is in a standby state. The RC2 backs up the state of the FF 31. Specifically, the logic level of the data signal D0 input to the FF 31 is written to the RC2.

[0052]

5 First, the transistors Mos2 and Mos3 are turned off to make the node FN1 electrically floating and the signal CSB is set at an H level, so that the potential of the node FN1 is boosted to a potential at which the logic level becomes "H". Then, the transistor Mos1 is turned on so that the signal D0 is input to the node FN1. When the logic level of the signal D0 is "L", the charge of the node FN1 is extracted to the
10 terminal INa; thus, the potential of the node FN1 drops and the logic level of the node FN1 becomes "L". When the logic level of the signal D0 is "H", the charge of the node FN1 is stored and the logic level of the node FN1 is kept "H".

[0053]

As described above, the charge of the node FN1 moves during the backup
15 operation of the RC2 because of precharge operation for making the logic level of the node FN1 "L" and boosting operation of the node FN1 due to capacitive coupling only when data L is written. Thus, the backup operation can be carried out at high speed, which enables supply of VDD to be stopped in a short time after supply of CLK is stopped. In addition, a voltage drop of the node FN1 due to the threshold voltage of
20 the transistor Mos1 does not occur in the case of writing data H. As a result, the H level potential of the control signal OG1 of the transistor Mos1 needs not to be set higher than VDD.

[0054]

After the transistor Mos1 is turned on for a certain period, the transistor Mos1
25 is turned off to make the node FN1 electrically floating. In this manner, backup of the FF 31 is completed.

[0055]

In the example shown in FIG. 3, OG1 is set at an H level after CSB. However, CSB and OG1 may be changed to an H level concurrently, for example, in which case
30 the time necessary for the backup operation can be reduced.

[0056]

<Period T3>

In Period T3, supply of VDD is stopped and the semiconductor device 101 is stopped. After OG1 and RESET are set at L levels, supply of VDD is stopped.

[0057]

<Period T4>

5 To make the semiconductor device 101 in the normal operation again, first, supply of VDD is resumed. When supply of VDD is resumed, conduction between the terminal a20 and the terminal a30 are established through the SELC1.

[0058]

<Period T5>

10 The FF 31 is restored to a state before supply of CLK is stopped. Specifically, data held in the RC2 is written to the FF 31. First, SEL and OG3 are set at H levels so that conduction between the terminal INb and the input terminal a30 of the FF 31 are established, and the signal SC is set at an H level. Accordingly, the logic level of the terminal a30 becomes "H". Next, the transistor Mos2 is turned on so that conduction
15 between the node FN1 and the terminal a30 are established. When the logic level of the node FN1 is "L", the potential of the terminal a30 becomes at an L level; thus, the logic level of the terminal a30 becomes "L". When the logic level of the node FN1 is "H", the potential of the terminal a30 hardly changes; thus, the logic level of the terminal a30 is kept "H". In the above manner, the state of the FF 31 can be set to a
20 state held in the node FN1. This means that the FF 31 can be restored to a state just before supply of CLK is stopped.

[0059]

As described above, since data held in the RC2 is written to the FF 31 after the logic level of the terminal a30 is set "H" during the restoration operation of the RC2, the
25 charge of the node FN1 moves only when data L is written to the FF 31. As a result, the restoration operation can be carried out at high speed, which enables the semiconductor device 101 to operate normally in a short time after supply of VDD is resumed. In addition, a voltage drop of the terminal a30 due to the threshold voltage of the transistor Mos2 does not occur in the case of writing data H. Thus, the H level
30 potential of the control signal OG2 of the transistor Mos2 needs not to be set higher than VDD.

[0060]

Operation of setting the logic level of the terminal a30 to "H" is not affected by the circuit configuration of the FF 31 or a state at the time when power supply is stopped. This means that any of a variety of sequential circuits can be used as the circuit 11. As described above, the holding circuit of this embodiment can be widely
5 used; thus, a data holding function for power gating can be added to a variety of sequential circuits.

[0061]

<Period T6>

Supply of CLK is resumed so that the semiconductor device 101 operates
10 normally. In Period T5, which is before supply of CLK is resumed, the signal RESET is set at an H level. The driving method of the semiconductor device 101 in Period T6 is similar to that in Period T1; thus, the description is omitted.

[0062]

As described above, in the precharge operation of the node FN1, the storage
15 operation of the RC2, and the restoration operation of the RC2, the threshold voltages of the transistors Mos1 to Mos3 do not affect the logic level of data written to the RC2 or the FF 31. Thus, even when the transistors Mos1 to Mos3 are OS transistors, the H level potentials of the control signals OG1 to OG3 of these transistors can be the same potential as VDD of the circuit 11. In other words, even when the RC2 is provided in
20 the semiconductor device 101, the number of kinds of potentials necessary for operation is not increased.

[0063]

<<Example 2 of Driving Method of Semiconductor Device>>

In the example of a driving method shown in FIG. 3, the RC2 backs up the data
25 signal D0 input to the terminal INa. The RC2 can also back up the signal SC input to the terminal INb. FIG. 4 shows an example of such a driving method. In the example of a driving method in FIG. 4, the description of the same operation as the example of a driving method in FIG. 3 is omitted; thus, for the description, refer to the description for FIG. 3.

30 [0064]

<Period T11>

In Period T11, the semiconductor device 101 is in a normal operation mode.

Period T11 is different from Period T1 in FIG. 3 in that the logic level of the signal D0 remains "L". It is needless to say that the signal D0 in Period T11 can be a data signal whose logic level changes as shown in FIG. 3.

[0065]

5 <Period T12>

A data signal input to the terminal INb is backed up. After supply of CLK is stopped, first, the potential of the node FN1 is boosted so that the logic level of the node FN1 becomes "H". To achieve this, the transistors Mos1 to Mos3 are turned off and the signal CSB is set at an H level. Then, the transistors Mos2 and Mos3 are turned on and the signal SC is written to the node FN1.

[0066]

<Period T13>

In Period T13, the semiconductor device 101 operates in a manner similar to that in Period T3 in FIG. 3; the transistors Mos2 and Mos3 are turned off, and supply of VDD is stopped. The RC2 holds data input to the terminal INb in Period T12.

[0067]

<Period T14, Period T15>

The semiconductor device 101 operates in a manner similar to those in Periods T4 and T5 in FIG. 3; supply of VDD is resumed, data held in the RC2 is written to the input terminal a30 of the FF 31, and the state of the FF 31 is restored. Then, supply of CLK is resumed so that the semiconductor device 101 operates normally.

[0068]

<Period T16>

In Period T16, the semiconductor device 101 operates normally. Period T16 is different from Period T6 in FIG. 3 in that conduction between the terminal INb and the terminal a21 are established through the transistor Mos3, and the signal SEL is set at an H level so that conduction between the terminal a30 and the terminal a21 are established through the SELC1. Thus, a data signal (SC) input to the terminal INb is input to the FF 31.

[0069]

In the case where the semiconductor device 101 operates as a scan FF, for example, test data is input to the terminal INb in Period T12. Scan-in operation for

inputting a test pattern to the semiconductor device 101 (RC1) may be performed in Period T12 and shift operation may be performed in Period T16, for example. In that case, the semiconductor device 101 operates as shown in FIG. 4, so that whether data held in the RC2 is normal or not can be determined from the logical value of the output
5 signal Q0 of the circuit 11 (scan FF), and therefore whether the RC2 has a problem or not can be determined.

[0070]

The example of a circuit configuration in FIG. 2 shows that a general scan flip-flop circuit including a selection circuit and a flip-flop circuit can be used as the
10 circuit 11. The examples of a driving method in FIG. 3 and FIG. 4 show that the semiconductor device 101 can operate as a general scan FF.

[0071]

Thus, the semiconductor device 101 of this embodiment can be a semiconductor device including a scan FF (the circuit 11) and a holding circuit (OS
15 block) having an OS transistor. Since a general circuit can be used as the scan FF, changes in circuit configuration and layout due to addition of the OS block can be prevented. The OS block can be formed using an OS transistor and a capacitor and thus can be stacked over the scan FF. When the semiconductor device 101 has a
20 three-dimensional structure in which the OS block is stacked over the scan FF, layout area overhead due to the addition of the OS block and a performance penalty during normal operation can be zero.

[0072]

As described above, owing to the semiconductor device of this embodiment, dynamic power consumption of the semiconductor device 101 can be reduced by power
25 gating almost without performance overhead and area overhead even when an OS block is added.

[0073]

<<Modification Examples of Semiconductor Device>>

Some modification examples of the semiconductor device 100 (FIG. 1) will be
30 described below.

[0074]

<Configuration Example 3>

In FIG. 1, the input terminal a1 of the RC1 is electrically connected to the input terminal a20 (the input terminal INa) of the circuit 10. A connection node at which the terminal a1 is connected to the circuit 10 is not limited to the terminal a20 and can be, for example, the output terminal b20 of the circuit 20, the input terminal a30 of the circuit 30, the output terminal b30 of the circuit 30, or an internal node of the circuit 30. In this case, the internal node of the circuit 30 is a node on a transmission path of a data signal between the terminal a30 and the terminal b30. In the case where the FF 31 illustrated in FIG. 2 is used as the circuit 30, for example, the internal node is an output terminal of the clocked inverter circuit in the LATa, an output terminal of the NAND gate circuit in the LATa, or an output terminal of the inverter circuit in the LATb.

[0075]

A semiconductor device 111 illustrated in FIG. 5 is an example where the terminal a1 is electrically connected to the terminal b30. Also in this configuration example, a change in the configuration or layout of the circuit 10 is unnecessary as illustrated in FIG. 5.

[0076]

<Configuration Example 4>

The terminal a1 may be electrically connected to a buffer portion so as to compensate the logic level of a signal input to the terminal a1 of the RC1. The buffer portion can be one buffer circuit, cascaded buffer circuits, one inverter circuit, cascaded inverter circuits, or the like. In the case where data obtained by inverting the logic of the signal D0 needs to be held in the RC1 in FIG. 1 under constraints of the configuration of the circuit 10 and the like, an even number of inverter circuits are used as the buffer portion.

[0077]

The terminal b1 may also be electrically connected to the buffer portion so as to compensate the logic level of an output signal from the terminal b1 of the RC1 or to invert the logic of the output signal.

[0078]

A semiconductor device 112 illustrated in FIG. 6A is an example where the terminal a1 is electrically connected to one buffer circuit 52. A semiconductor device 113 illustrated in FIG. 6B is an example where the terminal b1 is electrically connected

to one inverter circuit 53.

[0079]

<Configuration Example 5>

Although the circuit RC1 illustrated in FIG. 1 can hold one state, a holding
5 circuit that can hold a plurality of states can be provided in the semiconductor device.
FIG. 7 illustrates such a configuration example. A semiconductor device 114
illustrated in FIG. 7 includes a circuit RC14 instead of the circuit RC1, as a backup
memory circuit for states.

[0080]

10 The RC14 corresponds to the RC1 additionally including two circuits (RC1c
and RC1d). Thus, the RC14 can hold three states. The RC1c and the RC1d have the
same configuration as the RC1, and can be driven in a manner similar to that of the RC1.
The RC1c and the RC1d can also hold data signals input from the terminals INa and
INb and can write their holding states to the circuit 10. A node FN1c and a node FN1d
15 are data holding nodes of the RC1c and the RC1d, respectively.

[0081]

Switches SW1, SW1c, SW1d, SW2, SW2c, SW2d, SW3, SW3c, and SW3d in
the RC14 are turned on/off independently. The switches SW1, SW1c, SW1d, SW2,
SW2c, and SW2d are OS transistors. The switches SW3c and SW3d each can be an
20 OS transistor or a switch circuit such as an analog switch like the SW3.

[0082]

The signal CSB is input to second terminals of capacitors CP1, CP1c, and
CP1d. Alternatively, different signals may be input to the second terminals of the
capacitors CP1, CP1c, and CP1d, so that the potentials of the nodes FN1, FN1c, and
25 FN1d can be boosted independently.

[0083]

In normal operation of the semiconductor device 114, the state of the circuit 30
can be written to one of the holding circuits RC1, RC1c, and RC1d in the RC14. In
other words, the RC14 can hold up to three states of the semiconductor device 114
30 (circuit 30) at a given period in normal operation.

[0084]

(Embodiment 2)

In this embodiment, an OS transistor will be described as an example of a semiconductor device.

[0085]

<<Structure Example 1 of OS Transistor>>

5 FIGS. 8A to 8D illustrate a structure example of an OS transistor. FIG. 8A is a top view illustrating a structure example of an OS transistor. FIG. 8B is a cross-sectional view taken along a line y1-y2, FIG. 8C is a cross-sectional view taken along a line x1-x2, and FIG. 8D is a cross-sectional view taken along a line x3-x4. To clarify the device structure, FIG. 8A does not illustrate some components. Here, in
10 some cases, the direction of the line y1-y2 is referred to as a channel length direction, and the direction of the line x1-x2 is referred to as a channel width direction. Accordingly, FIG. 8B illustrates a cross-sectional structure of the OS transistor in the channel length direction, and FIGS. 8C and 8D each illustrate a cross-sectional structure of the OS transistor in the channel width direction.

15 [0086]

As illustrated in FIGS. 8A to 8D, an OS transistor 600 is formed over a substrate 640 and is covered with an insulating layer 654 and an insulating layer 655. The OS transistor includes an insulating layer 652, a gate insulating layer 653, oxide semiconductor (OS) layers 661 to 663, an electrode 671, an electrode 672, and a gate
20 electrode 673. Here, the OS layers 661, 662, and 663 are collectively referred to as an OS layer 660.

[0087]

A stack including oxide semiconductor films in which the OS layer 661 and the OS layer 662 are stacked in this order is formed over the insulating layer 652. The
25 electrodes 671 and 672 are electrically connected to the stack. The electrodes 671 and 672 can serve as source and drain electrodes of the OS transistor 600. The OS layer 663 covers the OS layers 661 and 662 and the electrodes 671 and 672. The gate insulating layer 653 is stacked over the OS layer 663. The gate electrode 673 overlaps with a portion where the OS layers 661 to 663 are stacked with the gate insulating layer
30 653 provided therebetween and overlaps with the electrodes 671 and 672 with a stack including the gate insulating layer 653 and the OS layer 663 provided therebetween.

[0088]

<<Structure Example 2 of OS Transistor>>

FIGS. 9A to 9D illustrate another structure example of an OS transistor. FIG. 9A is a top view illustrating a structure example of an OS transistor. FIG. 9B is a cross-sectional view taken along a line y1-y2, FIG. 9C is a cross-sectional view taken along a line x1-x2, and FIG. 9D is a cross-sectional view taken along a line x3-x4. To clarify the device structure, FIG. 9A does not illustrate some components.

[0089]

An OS transistor 601 illustrated in FIGS. 9A to 9D corresponds to the OS transistor 600 having a second gate electrode. A conductive layer 674 is formed over the substrate 640 with an insulating layer 651 provided therebetween. The conductive layer 674 has a region serving as a gate electrode layer. The conductive layer 674 may be supplied with the same potential or signal as the gate electrode 673, or the potential of the conductive layer 674 may be controlled independently of the gate electrode 673. In the former, the gate electrode 673 may be electrically connected to the conductive layer 674.

[0090]

The three-dimensional device structure like the structures of the OS transistors 600 and 601 can provide an OS transistor with a 60-nm or 30-nm technology node, or with an even smaller technology node. The components of the OS transistors 600 and 601 will be described below.

[0091]

<<Oxide Semiconductor Layer>>

Typical examples of a semiconductor material for the OS layers 661 to 663 include an In-Ga oxide, an In-Zn oxide, and an In-*M*-Zn oxide (*M* is Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf). The OS layer 660 is preferably an In-*M*-Zn oxide film. It is needless to say that the OS layers 661 to 663 are not limited to oxide films containing indium. The OS layers 661 to 663 can be formed using, for example, a Zn-Sn oxide film or a Ga-Sn film.

[0092]

In the case where the OS layers 661 to 663 are each the In-*M*-Zn oxide film (*M* is Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf) formed by a sputtering method, it is preferred that the atomic ratio of metal elements of a target used for forming the In-*M*-Zn oxide

film satisfy $\text{In} \geq M$ and $\text{Zn} \geq M$. As the atomic ratio of metal elements of such a sputtering target, $\text{In:M:Zn} = 1:1:1$, $\text{In:M:Zn} = 1:1:1.2$, $\text{In:M:Zn} = 3:1:2$, and $\text{In:M:Zn} = 2:1:3$ are preferable. Note that the atomic ratios of metal elements in the oxide semiconductor film formed by a sputtering method vary from those in the sputtering target used, within an error range of $\pm 40\%$.

[0093]

For example, when In-Ga-Zn oxide films are formed as the OS layers 661 and 663 by a sputtering method, an In-Ga-Zn oxide target ($\text{In:Ga:Zn} = 1:3:2$ [atomic ratio]) can be used for the deposition of the oxide semiconductor films. The deposition conditions can be as follows: an argon gas (flow rate: 30 sccm) and an oxygen gas (flow rate: 15 sccm) are used as the deposition gas; the pressure is 0.4 Pa; the substrate temperature is 200 °C; and the DC power is 0.5 kW.

[0094]

In the case where an In-Ga-Zn oxide film is formed as the OS layer 662 by a sputtering method, a polycrystalline target containing an In-Ga-Zn oxide ($\text{In:Ga:Zn} = 1:1:1$ [atomic ratio]) is preferably used for the deposition of the oxide semiconductor film. With such a target, a CAAC-OS film that will be described later can be formed. The conditions of deposition using the target can be as follows, for example: an argon gas (flow rate: 30 sccm) and an oxygen gas (flow rate: 15 sccm) are used as the deposition gas; the pressure is 0.4 Pa; the substrate temperature is 300 °C; and the DC power is 0.5 kW. Alternatively, a polycrystalline In-Ga-Zn oxide ($\text{In:Ga:Zn} = 2:1:3$ [atomic ratio]) may be used as a target. Note that the CAAC-OS film is an oxide semiconductor film having a c-axis aligned crystal part, and is described later. An OS transistor whose semiconductor region is formed using a CAAC-OS film can have high reliability such as a small variation in electric characteristics due to irradiation of visible light or ultraviolet light.

[0095]

(Energy Band Diagram)

Next, a function and an effect of the OS layer 660 in which the OS layers 661 to 663 are stacked will be described with reference to an energy band diagram shown in FIG. 10B. FIG. 10A, which is a partial enlarged view of FIG. 8B, is an enlarged view

illustrating a channel of the OS transistor 600. FIG. 10B is an energy band diagram of a portion (channel of the OS transistor 600) along dotted line z1-z2 in FIG. 10A.

[0096]

In FIG. 10B, Ec652, Ec661, Ec662, Ec663, and Ec653 indicate the conduction band minimums of the insulating layer 652, the OS layer 661, the OS layer 662, the OS layer 663, and the gate insulating layer 653, respectively.

[0097]

A difference in energy between the vacuum level and the conduction band minimum (the difference is also referred to as electron affinity) corresponds to a value obtained by subtracting an energy gap from a difference in energy between the vacuum level and the valence band maximum (the difference is also referred to as ionization potential). The energy gap can be measured using a spectroscopic ellipsometer (UT-300 manufactured by HORIBA Jobin Yvon SAS). The energy difference between the vacuum level and the valence band maximum can be measured using an ultraviolet photoelectron spectroscopy (UPS) device (VersaProbe manufactured by ULVAC-PHI, Inc.).

[0098]

An In-Ga-Zn oxide formed using a sputtering target with an atomic ratio of In:Ga:Zn = 1:3:2 has, for example, an energy gap of approximately 3.5 eV and an electron affinity of approximately 4.5 eV. An In-Ga-Zn oxide formed using a sputtering target with an atomic ratio of In:Ga:Zn = 1:3:4 has an energy gap of approximately 3.4 eV and an electron affinity of approximately 4.5 eV. An In-Ga-Zn oxide formed using a sputtering target with an atomic ratio of In:Ga:Zn = 1:3:6 has an energy gap of approximately 3.3 eV and an electron affinity of approximately 4.5 eV. An In-Ga-Zn oxide formed using a sputtering target with an atomic ratio of In:Ga:Zn = 1:6:2 has an energy gap of approximately 3.9 eV and an electron affinity of approximately 4.3 eV. An In-Ga-Zn oxide formed using a sputtering target with an atomic ratio of In:Ga:Zn = 1:6:8 has an energy gap of approximately 3.5 eV and an electron affinity of approximately 4.4 eV. An In-Ga-Zn oxide which is formed using a sputtering target having an atomic ratio of In:Ga:Zn = 1:6:10 has an energy gap of approximately 3.5 eV and an electron affinity of approximately 4.5 eV. An In-Ga-Zn

oxide formed using a sputtering target with an atomic ratio of In:Ga:Zn = 1:1:1 has an energy gap of approximately 3.2 eV and an electron affinity of approximately 4.7 eV. An In-Ga-Zn oxide formed using a sputtering target with an atomic ratio of In:Ga:Zn = 3:1:2 has an energy gap of approximately 2.8 eV and an electron affinity of approximately 5.0 eV.

[0099]

Since the insulating layer 652 and the gate insulating layer 653 are insulators, Ec652 and Ec653 are closer to the vacuum level than Ec661, Ec662, and Ec663 (i.e., the insulating layer 652 and the gate insulating layer 653 have a smaller electron affinity than the OS layer 661, the OS layer 662, and the OS layer 663).

[0100]

Ec661 is closer to the vacuum level than Ec662. Specifically, Ec661 is preferably located closer to the vacuum level than Ec662 by 0.05 eV or more, 0.07 eV or more, 0.1 eV or more, or 0.15 eV or more and 2 eV or less, 1 eV or less, 0.5 eV or less, or 0.4 eV or less.

[0101]

Ec663 is closer to the vacuum level than Ec662. Specifically, Ec663 is preferably located closer to the vacuum level than Ec662 by 0.05 eV or more, 0.07 eV or more, 0.1 eV or more, or 0.15 eV or more and 2 eV or less, 1 eV or less, 0.5 eV or less, or 0.4 eV or less.

[0102]

Mixed regions are formed in the vicinity of the interface between the OS layer 661 and the OS layer 662 and the interface between the OS layer 662 and the OS layer 663; thus, the energy of the conduction band minimum changes continuously. In other words, no state or few states exist at these interfaces.

[0103]

Accordingly, electrons transfer mainly through the OS layer 662 in the stacked-layer structure having the above energy band. Therefore, even if an interface state exists between the OS layer 661 and the insulating layer 652 or between the OS layer 663 and the gate insulating layer 653, the interface state hardly influences the transfer of electrons. In addition, since no interface state or few interface states exist

between the OS layer 661 and the OS layer 662 and between the OS layer 662 and the OS layer 663, the transfer of electrons is not interrupted in the regions. Consequently, the OS transistor 600 including the above stacked oxide semiconductors can have high field-effect mobility.

5 [0104]

Although trap states Et600 due to impurities or defects might be formed in the vicinity of the interface between the OS layer 661 and the insulating layer 652 and the interface between the OS layer 663 and the gate insulating layer 653 as illustrated in FIG. 10B, the OS layer 662 can be separated from the trap states owing to the existence
10 of the OS layer 661 and the OS layer 663.

[0105]

In the OS transistor 600 described in this embodiment, in the channel width direction, the top surface and side surfaces of the OS layer 662 are in contact with the OS layer 663, and the bottom surface of the OS layer 662 is in contact with the OS layer
15 661 (see FIG. 8C). Surrounding the OS layer 662 by the OS layer 661 and the OS layer 663 in this manner can further reduce the influence of the trap states.

[0106]

However, when the energy difference between Ec662 and Ec661 or Ec663 is small, an electron in the OS layer 662 might reach the trap state by passing over the
20 energy difference. Since the electron is trapped at the trap state, a negative fixed charge is generated at the interface with the insulating film, causing the threshold voltage of the transistor to be shifted in the positive direction. Therefore, each of the energy gaps between Ec661 and Ec662 and between Ec662 and Ec663 is preferably 0.1 eV or more, further preferably 0.15 eV or more, in which case a change in the threshold
25 voltage of the transistor can be reduced and the transistor can have favorable electrical characteristics.

[0107]

The band gap of each of the OS layer 661 and the OS layer 663 is preferably wider than that of the OS layer 662.

30 [0108]

For the OS layer 661 and the OS layer 663, a material containing Al, Ti, Ga, Ge, Y, Zr, Sn, La, Ce, or Hf with a higher atomic ratio than that used for the OS layer 662

can be used, for example. Specifically, any of the above metal elements in an atomic ratio 1.5 times or more, preferably 2 times or more, further preferably 3 times or more as much as a metal element of the OS layer 662 is contained. Any of the above metal elements is strongly bonded to oxygen and thus has a function of preventing generation of oxygen vacancy in the oxide semiconductor. That is, an oxygen vacancy is less likely to be generated in the OS layer 661 and the OS layer 663 than in the OS layer 662.

[0109]

When each of the OS layer 661, the OS layer 662, and the OS layer 663 is an In-M-Zn oxide containing at least indium, zinc, and M (M is a metal such as Al, Ti, Ga, Ge, Y, Zr, Sn, La, Ce, or Hf) and the atomic ratio of In to M and Zn of the OS layer 661 is $x_1:y_1:z_1$, that of the OS layer 662 is $x_2:y_2:z_2$, and that of the OS layer 663 is $x_3:y_3:z_3$, each of y_1/x_1 and y_3/x_3 is preferably larger than y_2/x_2 . Each of y_1/x_1 and y_3/x_3 is one and a half times or more as large as y_2/x_2 , preferably twice or more as large as y_2/x_2 , more preferably three times or more as large as y_2/x_2 . In this case, the transistor can have stable electrical characteristics when y_2 is greater than or equal to x_2 in the OS layer 662. However, when y_2 is 3 times or more as large as x_2 , the field-effect mobility of the transistor is reduced; accordingly, y_2 is preferably smaller than 3 times x_2 .

[0110]

In the case where Zn and O are not taken into consideration, the proportion of In and the proportion of M in the OS layer 661 and the OS layer 663 are preferably lower than 50 atomic% and higher than or equal to 50 atomic%, respectively, and further preferably lower than 25 atomic% and higher than or equal to 75 atomic%, respectively. In the case where Zn and O are not taken into consideration, the proportion of In and the proportion of M in the OS layer 662 are preferably greater than or equal to 25 atomic% and less than 75 atomic%, respectively, and further preferably greater than or equal to 34 atomic% and less than 66 atomic%, respectively.

[0111]

The thickness of each of the OS layer 661 and the OS layer 663 ranges from 3 nm to 100 nm, preferably from 3 nm to 50 nm. The thickness of the OS layer 662 ranges from 3 nm to 200 nm, preferably from 3 nm to 100 nm, further preferably from 3

nm to 50 nm. The OS layer 662 is preferably thicker than the OS layer 661 and the OS layer 663.

[0112]

Note that stable electrical characteristics can be effectively imparted to an OS transistor in which an oxide semiconductor layer serves as a channel by reducing the concentration of impurities in the oxide semiconductor layer to make the oxide semiconductor layer intrinsic or substantially intrinsic. The term "substantially intrinsic" refers to the state where an oxide semiconductor layer has a carrier density lower than $1 \times 10^{17} / \text{cm}^3$, lower than $1 \times 10^{15} / \text{cm}^3$, or lower than $1 \times 10^{13} / \text{cm}^3$.

[0113]

In the oxide semiconductor, hydrogen, nitrogen, carbon, silicon, and a metal element other than a main component are impurities. For example, hydrogen and nitrogen form donor levels to increase the carrier density, and silicon forms impurity levels in the oxide semiconductor layer. Silicon in the oxide semiconductor forms an impurity level. The impurity levels serve as traps and might cause the electrical characteristics of the OS transistor to deteriorate. Therefore, it is preferable to reduce the concentration of the impurities in the OS layer 661, the OS layer 662, and the OS layer 663 and at interfaces between the layers.

[0114]

In order to make the oxide semiconductor intrinsic or substantially intrinsic, the concentration of silicon at a certain depth of the oxide semiconductor or in a region of the oxide semiconductor is preferably lower than $1 \times 10^{19} \text{ atoms/cm}^3$, lower than $5 \times 10^{18} \text{ atoms/cm}^3$, or lower than $1 \times 10^{18} \text{ atoms/cm}^3$. The concentration of hydrogen at a certain depth of the oxide semiconductor or in a region of the oxide semiconductor is preferably lower than or equal to $2 \times 10^{20} \text{ atoms/cm}^3$, lower than or equal to $5 \times 10^{19} \text{ atoms/cm}^3$, lower than or equal to $1 \times 10^{19} \text{ atoms/cm}^3$, or lower than or equal to $5 \times 10^{18} \text{ atoms/cm}^3$. The concentration of nitrogen at a certain depth of the oxide semiconductor or in a region of the oxide semiconductor is preferably lower than $5 \times 10^{19} \text{ atoms/cm}^3$, lower than or equal to $5 \times 10^{18} \text{ atoms/cm}^3$, lower than or equal to $1 \times 10^{18} \text{ atoms/cm}^3$, or lower than or equal to $5 \times 10^{17} \text{ atoms/cm}^3$.

[0115]

In the case where the oxide semiconductor includes a crystal part, high concentration of silicon or carbon might reduce the crystallinity of the oxide semiconductor. In order not to lower the crystallinity of the oxide semiconductor, the concentration of silicon at a certain depth of the oxide semiconductor or in a region of the oxide semiconductor is preferably lower than 1×10^{19} atoms/cm³, lower than 5×10^{18} atoms/cm³, or lower than 1×10^{18} atoms/cm³. Furthermore, the concentration of carbon at a certain depth of the oxide semiconductor or in a region of the oxide semiconductor is preferably lower than 1×10^{19} atoms/cm³, lower than 5×10^{18} atoms/cm³, or lower than 1×10^{18} atoms/cm³.

[0116]

The listed concentrations of the impurities such as oxygen and carbon are values obtained by secondary ion mass spectrometry (SIMS). With the use of such a highly purified oxide semiconductor, the off-state current of the OS transistor can be reduced. When the voltage between a source and a drain is approximately 0.1 V to 10 V, for example, the off-state current standardized on the channel width can be as low as several yoctoamperes per micrometer to several zeptoamperes per micrometer.

[0117]

In each of the OS transistors 600 and 601 described as examples in this embodiment, the gate electrode 673 is formed to electrically surround the OS layer 660 in the channel width direction; consequently, a gate electric field is applied to the OS layer 660 in the side surface direction in addition to the perpendicular direction (see FIG. 8C). In other words, a gate electric field is applied to the whole oxide semiconductor layer, so that current flows through the entire OS layer 662 serving as a channel, leading to a further increase in on-state current. The components of the OS transistors 600 and 601 will be described below.

[0118]

<<Crystal Structure of Oxide Semiconductor>>

First, a structure of an oxide semiconductor that forms the OS layer 660 will be described. In this specification, trigonal and rhombohedral crystal systems are included in a hexagonal crystal system.

[0119]

Oxide semiconductors are classified roughly into a single-crystal oxide semiconductor and a non-single-crystal oxide semiconductor. Examples of a non-single-crystal oxide semiconductor include a c-axis aligned crystalline oxide semiconductor (CAAC-OS), a polycrystalline oxide semiconductor, a microcrystalline
5 oxide semiconductor, a nanocrystalline oxide semiconductor (nc-OS), an amorphous-like oxide semiconductor (a-like OS), and an amorphous oxide semiconductor.

[0120]

It is known that an amorphous structure is generally defined as being
10 metastable and unfixed, and being isotropic and having no non-uniform structure. In other words, an amorphous structure has a flexible bond angle and a short-range order but does not have a long-range order.

[0121]

This means that an inherently stable oxide semiconductor cannot be regarded
15 as a completely amorphous oxide semiconductor. Moreover, an oxide semiconductor that is not isotropic (e.g., an oxide semiconductor film that has a periodic structure in a microscopic region) cannot be regarded as a completely amorphous oxide semiconductor. Note that an a-like OS has a periodic structure in a microscopic region, but at the same time has a void and has an unstable structure. For this reason, an a-like
20 OS has physical properties similar to those of an amorphous oxide semiconductor.

[0122]

<CAAC-OS>

A CAAC-OS is one of oxide semiconductors having a plurality of c-axis aligned crystal parts (also referred to as pellets). In a combined analysis image (also
25 referred to as a high-resolution TEM image) of a bright-field image and a diffraction pattern of a CAAC-OS, which is obtained using a transmission electron microscope (TEM), a plurality of crystal parts can be observed. However, in the high-resolution TEM image, a boundary between crystal parts, that is, a grain boundary is not clearly observed. Thus, in the CAAC-OS, a reduction in electron mobility due to the grain
30 boundary is less likely to occur.

[0123]

When the high-resolution TEM image of the CAAC-OS is observed in a

direction parallel to a sample surface, metal atoms are arranged in a layered manner in a crystal part. Each metal atom layer has a morphology reflecting the unevenness of a surface over which a CAAC-OS film is formed (hereinafter the surface is referred to as a formation surface) or a top surface of the CAAC-OS, and is arranged parallel to the formation surface or the top surface of the CAAC-OS.

[0124]

In this specification, the term "parallel" indicates that the angle formed between two straight lines is greater than or equal to -10° and less than or equal to 10° , and accordingly also includes the case where the angle is greater than or equal to -5° and less than or equal to 5° . The term "perpendicular" indicates that the angle formed between two straight lines is greater than or equal to 80° and less than or equal to 100° , and accordingly includes the case where the angle is greater than or equal to 85° and less than or equal to 95° .

[0125]

The high-resolution cross-sectional TEM image of the CAAC-OS revealed that the size of one crystal part of the CAAC-OS is 1 nm or greater or 3 nm or greater, and the size of a space caused by tilt of crystal parts is approximately 0.8 nm. Therefore, the crystal part can also be referred to as a nanocrystal (nc). Furthermore, the CAAC-OS can also be referred to as an oxide semiconductor including c-axis aligned nanocrystals (CANC).

[0126]

In the high-resolution planar TEM image of the CAAC-OS observed in a direction substantially perpendicular to the sample surface, metal atoms arranged in a triangular or hexagonal configuration are seen in the crystal parts. However, there is no regularity of arrangement of metal atoms between different crystal parts.

[0127]

A CAAC-OS is subjected to structural analysis with an X-ray diffraction (XRD) apparatus. When the CAAC-OS including an InGaZnO_4 crystal is analyzed by an out-of-plane method, for example, a peak appears frequently when the diffraction angle (2θ) is around 31° . This peak is derived from the (009) plane of the InGaZnO_4 crystal, which indicates that crystals in the CAAC-OS have c-axis alignment, and that

the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS.

[0128]

Note that when the CAAC-OS with an InGaZnO_4 crystal is analyzed by an out-of-plane method, a peak of 2θ may also be observed at around 36° , in addition to the peak of 2θ at around 31° . The peak of 2θ at around 36° indicates that a crystal having no c-axis alignment is included in part of the CAAC-OS. It is preferable that in the CAAC-OS, a peak of 2θ appear at around 31° and a peak of 2θ not appear at around 36° .

[0129]

The CAAC-OS is an oxide semiconductor film having low impurity concentration. The impurity is an element other than the main components of the oxide semiconductor, such as hydrogen, carbon, silicon, or a transition metal element. In particular, an element that has higher bonding strength to oxygen than a metal element included in the oxide semiconductor, such as silicon, disturbs the atomic arrangement of the oxide semiconductor by depriving the oxide semiconductor of oxygen and causes a decrease in crystallinity. Furthermore, a heavy metal such as iron or nickel, argon, carbon dioxide, or the like has a large atomic radius (or molecular radius), and thus disturbs the atomic arrangement of the oxide semiconductor film and causes a decrease in crystallinity when it is contained in the oxide semiconductor film. Note that the impurity contained in the oxide semiconductor might serve as a carrier trap or a carrier generation source.

[0130]

The CAAC-OS is an oxide semiconductor film having a low density of defect states. In some cases, oxygen vacancies in the oxide semiconductor serve as carrier traps or serve as carrier generation sources when hydrogen is captured therein.

[0131]

The state in which impurity concentration is low and density of defect states is low (the number of oxygen vacancies is small) is referred to as a "highly purified intrinsic" or "substantially highly purified intrinsic" state. A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor has few carrier generation

sources, and thus can have a low carrier density. Thus, a transistor including the oxide semiconductor rarely has negative threshold voltage (is rarely normally on). The highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor has few carrier traps. Accordingly, the transistor including the oxide semiconductor has little variation in electrical characteristics and high reliability. Electric charge trapped by the carrier traps in the oxide semiconductor takes a long time to be released, and might behave like fixed electric charge. Thus, the transistor which includes the oxide semiconductor having high impurity concentration and a high density of defect states has unstable electrical characteristics in some cases.

[0132]

<Microcrystalline Oxide Semiconductor, nc-OS>

An nc-OS has a region in which a crystal part is observed and a region in which a crystal part is not clearly observed in a high-resolution TEM image. In most cases, the size of a crystal part included in the nc-OS is greater than or equal to 1 nm and less than or equal to 10 nm, or greater than or equal to 1 nm and less than or equal to 3 nm. Note that an oxide semiconductor including a crystal part whose size is greater than 10 nm and less than or equal to 100 nm is sometimes referred to as a microcrystalline oxide semiconductor. In a high-resolution TEM image of the nc-OS, for example, a grain boundary is not clearly observed in some cases. Note that there is a possibility that the origin of the nanocrystal is the same as that of a pellet in a CAAC-OS. Therefore, a crystal part of the nc-OS may be referred to as a pellet in the following description.

[0133]

In the nc-OS, a microscopic region (e.g., a region with a size greater than or equal to 1 nm and less than or equal to 10 nm, in particular, a region with a size greater than or equal to 1 nm and less than or equal to 3 nm) has a periodic atomic arrangement. There is no regularity of crystal orientation between different crystal parts in the nc-OS. Thus, the orientation of the whole film is not observed. Accordingly, in some cases, the nc-OS cannot be distinguished from an a-like OS or an amorphous oxide semiconductor depending on an analysis method. For example, when the nc-OS is analyzed by an out-of-plane method with an XRD apparatus using an X-ray beam having a diameter larger than the size of a crystal part, a peak which shows a crystal

plane does not appear. Furthermore, a diffraction pattern like a halo pattern is observed when the nc-OS is subjected to electron diffraction using an electron beam with a probe diameter (e.g., 50 nm or larger) that is larger than the size of a crystal part. Meanwhile, spots appear in a nanobeam electron diffraction pattern of the nc-OS when
5 an electron beam having a probe diameter close to or smaller than the size of a crystal part is applied. Moreover, in a nanobeam electron diffraction pattern of the nc-OS, regions with high luminance in a circular (ring) pattern are shown in some cases. Also in a nanobeam electron diffraction pattern of the nc-OS, a plurality of spots is shown in a ring-like region in some cases.

10 [0134]

Since there is no regularity of crystal orientation between the pellets (nanocrystals) as mentioned above, the nc-OS can also be referred to as an oxide semiconductor including random aligned nanocrystals (RANC) or an oxide semiconductor including non-aligned nanocrystals (NANC).

15 [0135]

The nc-OS is an oxide semiconductor that has high regularity as compared with an amorphous oxide semiconductor. Therefore, the nc-OS is likely to have a lower density of defect states than an amorphous oxide semiconductor. Note that there is no regularity of crystal orientation between different crystal parts in the nc-OS. Therefore,
20 the nc-OS has a higher density of defect states than the CAAC-OS.

[0136]

<Amorphous Oxide Semiconductor>

The amorphous oxide semiconductor has disordered atomic arrangement and no crystal part. For example, the amorphous oxide semiconductor does not have a
25 specific state as in quartz.

[0137]

In the high-resolution TEM image of the amorphous oxide semiconductor, crystal parts cannot be found. When the amorphous oxide semiconductor is subjected to structural analysis by an out-of-plane method with an XRD apparatus, a peak
30 showing a crystal plane does not appear. A halo pattern is shown in an electron diffraction pattern of the amorphous oxide semiconductor. Furthermore, a halo pattern is shown but a spot is not shown in a nanobeam electron diffraction pattern of the

amorphous oxide semiconductor.

[0138]

<a-like OS>

An a-like OS has a structure intermediate between those of the nc-OS and the
5 amorphous oxide semiconductor. In a high-resolution TEM image of the a-like OS, a
void may be observed. Furthermore, in the high-resolution TEM image, there are a
region where a crystal part is clearly observed and a region where a crystal part is not
observed. The a-like OS has an unstable structure because it contains a void. In the
a-like OS, crystallization by a slight amount of electron beam used for TEM observation
10 occurs and growth of the crystal part is found sometimes. In contrast, crystallization
by a slight amount of electron beam used for TEM observation is less observed in the
nc-OS having good quality.

[0139]

Note that the crystal part size in the a-like OS and the nc-OS can be measured
15 using high-resolution TEM images. For example, an InGaZnO₄ crystal has a layered
structure in which two Ga-Zn-O layers are included between In-O layers. A unit cell
of the InGaZnO₄ crystal has a structure in which nine layers of three In-O layers and six
Ga-Zn-O layers are layered in the c-axis direction. Thus, the distance between the
adjacent layers is equivalent to the lattice spacing on the (009) plane (also referred to as
20 d value). The value is calculated to be 0.29 nm from crystal structural analysis. Thus,
each of the lattice fringes having a distance therebetween of from 0.28 nm to 0.30 nm
corresponds to the a-b plane of the InGaZnO₄ crystal, focusing on the lattice fringes in
the high-resolution TEM image.

[0140]

25 An oxide semiconductor may be a stack including two or more of an
amorphous oxide semiconductor, an a-like OS, a microcrystalline oxide semiconductor,
and a CAAC-OS, for example.

[0141]

<Substrate>

30 The substrate 640 is not limited to a simple supporting substrate and may be a
substrate where a device such as a transistor is formed. In that case, one of the gate
electrode 673, the electrode 671, and the electrode 672 of the OS transistor 600 may be

electrically connected to the device.

[0142]

<Base Insulating Film>

The insulating layer 652 can have a function of supplying oxygen to the OS
5 layer 660 as well as a function of preventing diffusion of impurities from the substrate
640. For this reason, the insulating layer 652 is preferably an insulating film
containing oxygen and more preferably an insulating film having an oxygen content
higher than that in the stoichiometric composition. For example, the insulating layer is
a film of which the amount of released oxygen when converted into oxygen atoms is 1.0
10 $\times 10^{19}$ atoms/cm³ or more in thermal desorption spectroscopy (TDS) analysis. Here,
the TDS analysis is conducted at a film surface temperature of higher than or equal to
100 °C and lower than or equal to 700 °C. When the substrate 640 is a substrate where
a device is formed as described above, the insulating layer 652 is preferably subjected to
planarization treatment such as chemical mechanical polishing (CMP) treatment so as to
15 have a flat surface.

[0143]

The insulating layer 652 can be formed using an oxide insulating film of
aluminum oxide, aluminum oxynitride, magnesium oxide, silicon oxide, silicon
oxynitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum
20 oxide, neodymium oxide, hafnium oxide, tantalum oxide, or the like, a nitride insulating
film of silicon nitride, silicon nitride oxide, aluminum nitride oxide, or the like, or a film
in which any of the above materials are mixed.

[0144]

<Gate Electrode>

25 The gate electrode 673 can be formed using, for example, a metal element
selected from chromium (Cr), copper (Cu), aluminum (Al), gold (Au), silver (Ag), zinc
(Zn), molybdenum (Mo), tantalum (Ta), titanium (Ti), tungsten (W), manganese (Mn),
nickel (Ni), iron (Fe), cobalt (Co), and ruthenium (Ru); or an alloy or a conductive
compound containing one or more of the metal elements. Examples of the conductive
30 compound are titanium nitride and nickel silicide.

[0145]

The gate electrode 673 may have a single-layer structure or a stacked-layer structure of two or more layers. For example, any of the following structures can be employed: a single-layer structure of an aluminum film containing silicon; a two-layer structure in which a titanium film is stacked over an aluminum film; a two-layer structure in which a titanium film is stacked over a titanium nitride film; a two-layer structure in which a tungsten film is stacked over a titanium nitride film; a two-layer structure in which a tungsten film is stacked over a tantalum nitride film or a tungsten nitride film; a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked in this order; a single-layer structure of a Cu-Mn alloy film; a two-layer structure in which a Cu film is stacked over a Cu-Mn alloy film; and a three-layer structure in which a Cu-Mn alloy film, a Cu film, and a Cu-Mn alloy film are stacked in this order. A Cu-Mn alloy film is preferably used because of its low electrical resistance and because it forms manganese oxide at the interface with an insulating film containing oxygen and manganese oxide can prevent Cu diffusion.

[0146]

A conductive film included in the gate electrode 673 can also be formed using a light-transmitting conductive material such as indium tin oxide, indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added. The gate electrode 673 may be formed of a stack formed using any of the above light-transmitting conductive materials and any of the above metal elements, for example.

[0147]

<Gate Insulating Layer>

The gate insulating layer 653 is formed using an insulating film having a single-layer structure or a stacked-layer structure. The insulating film may be formed using an insulating material such as aluminum oxide, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, or tantalum oxide. The gate insulating layer 653 may contain lanthanum (La), nitrogen, or zirconium (Zr) as an impurity. The insulating layer 651 can be formed in a manner similar to that for the gate insulating layer 653.

[0148]

The gate insulating layer 653 can be formed using, for example, a stack including a hafnium oxide film and a silicon oxide film or a stack including a hafnium oxide film and a silicon oxynitride film. Hafnium oxide has a higher dielectric constant than silicon oxide and silicon oxynitride. Therefore, the thickness can be made large as compared with silicon oxide; as a result, leakage current due to tunnel current can be low. That is, it is possible to provide a transistor with a low off-state current. Moreover, hafnium oxide with a crystalline structure has higher dielectric constant than hafnium oxide with an amorphous structure. Thus, to reduce off-state current of the OS transistor, the gate insulating layer 653 preferably contains hafnium oxide having a crystal structure. Examples of the crystalline structure include a monoclinic crystal structure and a cubic crystal structure. Note that one embodiment of the present invention is not limited to the above examples.

[0149]

<Source Electrode, Drain Electrode, Second Gate Electrode>

The electrodes 671 and 672 and the conductive layer 674 can be formed in a manner similar to that of the gate electrode 673. A Cu-Mn alloy film is preferably used for the electrodes 671 and 672 because it forms manganese oxide at the interface with the OS layer 660 and manganese oxide can prevent Cu diffusion.

[0150]

<Protective Insulating Film>

The insulating layer 654 has a function of blocking oxygen, hydrogen, water, alkali metal, alkaline earth metal, and the like. Providing the insulating layer 654 can prevent outward diffusion of oxygen from the OS layer 660 and entry of hydrogen, water, or the like into the OS layer 660 from the outside. The insulating layer 654 can be, for example, a nitride insulating film. Examples of the nitride insulating film include a silicon nitride film, a silicon nitride oxide film, an aluminum nitride film, and an aluminum nitride oxide film. Note that instead of the nitride insulating film having a blocking effect against oxygen, hydrogen, water, alkali metal, alkaline earth metal, and the like, an oxide insulating film having a blocking effect against oxygen, hydrogen, water, and the like, may be provided. As the oxide insulating film having a blocking effect against oxygen, hydrogen, water, and the like, an aluminum oxide film, an

aluminum oxynitride film, a gallium oxide film, a gallium oxynitride film, an yttrium oxide film, an yttrium oxynitride film, a hafnium oxide film, and a hafnium oxynitride film can be given.

[0151]

- 5 An aluminum oxide film is preferably used as the insulating layer 654 because it is highly effective in preventing transmission of both oxygen and impurities such as hydrogen and moisture. Thus, during and after the manufacturing process of the transistor, the aluminum oxide film can suitably serve as a protective film that has effects of preventing entry of impurities such as hydrogen and moisture, which cause
- 10 variations in the electrical characteristics of the transistor, into the OS layer 660, preventing release of oxygen, which is the main component of the OS layer 660, from the oxide semiconductor, and preventing unnecessary release of oxygen from the insulating layer 652. In addition, oxygen contained in the aluminum oxide film can be diffused into the oxide semiconductor.

15 [0152]

<Interlayer Insulating Film>

- The insulating layer 655 is preferably formed over the insulating layer 654. The insulating layer 655 can be formed using an insulating film with a single-layer structure or a layered structure. The insulating film can be formed using, for example,
- 20 a film containing aluminum oxide, aluminum oxynitride, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, tantalum oxide, or the like.

[0153]

- 25 <<Film Formation Method>>

- A sputtering method and a plasma CVD method are typical examples of a method of forming an insulating film, a conductive film, a semiconductor film, and the like. The insulating film, the conductive film, the semiconductor film, and the like may be formed by another method, for example, a thermal CVD method. A metal
- 30 organic chemical vapor deposition (MOCVD) method or an atomic layer deposition (ALD) method can be employed as a thermal CVD method, for example.

[0154]

Since plasma is not used for deposition, a thermal CVD method has an advantage that no defect due to plasma damage is generated. Deposition by a thermal CVD method may be performed in such a manner that a source gas and an oxidizer are supplied to a chamber at a time, the pressure in the chamber is set to an atmospheric pressure or a reduced pressure, and reaction is caused in the vicinity of or over a substrate.

[0155]

Deposition by an ALD method may be performed in such a manner that the pressure in a chamber is set to an atmospheric pressure or a reduced pressure, source gases for reaction are sequentially introduced into the chamber, and then the sequence of the gas introduction is repeated. For example, two or more kinds of source gases are sequentially supplied to the chamber by switching respective switching valves (also referred to as high-speed valves). In such a case, a first source gas is introduced, an inert gas (e.g., argon or nitrogen) or the like is introduced at the same time as or after the first source gas, and then a second source gas is introduced, whereby the source gases are not mixed. Note that in the case where the first source gas and the inert gas are introduced at a time, the inert gas serves as a carrier gas. The inert gas may also be introduced at the same time as the second source gas. Alternatively, the first source gas may be exhausted by vacuum evacuation instead of the introduction of the inert gas, and then the second source gas may be introduced. The first source gas is adsorbed on a surface of the substrate to form a first single-atomic layer and then, the second source gas is introduced to react with the first single-atomic layer; as a result, a second single-atomic layer is stacked over the first single-atomic layer, so that a thin film is formed. The sequence of the gas introduction is repeated plural times until a desired thickness is obtained, whereby a thin film with excellent step coverage can be formed. The thickness of the thin film can be adjusted by the number of repetition times of the sequence of the gas introduction. For this reason, an ALD method makes it possible to accurately adjust a thickness and thus is suitable for manufacturing a minute FET.

[0156]

The conductive film and the semiconductor film that are described in the above embodiment can be formed by a thermal CVD method such as a MOCVD method or an ALD method. For example, in the case where an InGaZnO_X ($X > 0$) film is formed,

trimethylindium, trimethylgallium, and diethylzinc are used. Note that the chemical formula of trimethylindium is $(\text{CH}_3)_3\text{In}$. The chemical formula of diethylzinc is $(\text{C}_2\text{H}_5)_2\text{Zn}$. Without limitation to the above combination, triethylgallium (chemical formula: $(\text{C}_2\text{H}_5)_3\text{Ga}$) can be used instead of trimethylgallium and dimethylzinc (chemical formula: $(\text{CH}_3)_2\text{Zn}$) can be used instead of diethylzinc.

[0157]

In the case where a tungsten film is formed using a deposition apparatus employing ALD, for example, a WF_6 gas and a B_2H_6 gas are sequentially introduced plural times to form an initial tungsten film, and then a WF_6 gas and an H_2 gas are introduced at a time, so that the tungsten film is formed. Note that an SiH_4 gas may be used instead of a B_2H_6 gas.

[0158]

In the case where an oxide semiconductor film, e.g., an InGaZnO_X ($X > 0$) film is formed using a deposition apparatus employing ALD, for example, an $(\text{CH}_3)_3\text{In}$ gas and an O_3 gas are sequentially introduced plural times to form an InO_2 layer, a $\text{Ga}(\text{CH}_3)_3$ gas and an O_3 gas are introduced at a time to form a GaO layer, and then a $\text{Zn}(\text{CH}_3)_2$ gas and an O_3 gas are introduced at a time to form a ZnO layer. Note that the order of these layers is not limited to this example. A mixed compound layer such as an InGaO_2 layer, an InZnO_2 layer, a GaInO layer, a ZnInO layer, or a GaZnO layer may be formed by mixing of these gases. Although an H_2O gas which is obtained by bubbling with an inert gas such as an Ar gas may be used instead of an O_3 gas, it is preferable to use an O_3 gas, which does not contain H. Instead of an $(\text{CH}_3)_3\text{In}$ gas, an $\text{In}(\text{C}_2\text{H}_5)_3$ gas may be used. Instead of a $\text{Ga}(\text{CH}_3)_3$ gas, a $(\text{C}_2\text{H}_5)_3\text{Ga}$ gas may be used. Furthermore, a $(\text{CH}_3)_2\text{Zn}$ gas may be used.

[0159]

(Embodiment 3)

A structure of the semiconductor device of Embodiment 1 is described. FIG. 11 is a cross-sectional view illustrating a structure example of a semiconductor device. In the semiconductor device illustrated in FIG. 11, a circuit block including an OS transistor and a capacitor is stacked over a circuit block including a Si transistor. FIG. 11 is a schematic cross-sectional view of an IC chip die of a semiconductor device. Note that FIG. 11 is not a diagram of the IC chip die taken along a specific line but a

diagram for illustrating a stacked-layer structure of the IC chip die.

[0160]

The semiconductor device illustrated in FIG. 11 includes a substrate 2201, a transistor 2301, a transistor 2302, and a capacitor 2303. The left side of FIG. 11 illustrates a cross section in a channel length direction of the transistors 2301 and 2302, and the right side of FIG. 11 illustrates a cross section in a channel width direction. It is needless to say that the channel length direction of the transistor 2301 does not necessarily agree with that of the transistor 2302 in an actual semiconductor device.

[0161]

The transistors 2301 and 2302 are electrically connected to each other through a plug 2011 and a plug 2012. The transistor 2302 and the capacitor 2303 are electrically connected to each other because one electrode of the transistor 2302 and one electrode of the capacitor 2303 are formed using the same conductive film.

[0162]

In FIG. 11, regions without reference numerals and hatch patterns represent regions formed of an insulator. The regions can be formed using an insulator containing at least one of aluminum oxide, aluminum nitride oxide, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, tantalum oxide, and the like. Alternatively, for the regions, an organic resin such as a polyimide resin, a polyamide resin, an acrylic resin, a siloxane resin, an epoxy resin, or a phenol resin can be used.

[0163]

The transistor 2301, a Si transistor here, has a semiconductor region containing a Group 14 element. The transistor 2302 is an OS transistor. In the case where the semiconductor device illustrated in FIG. 11 includes the semiconductor device 101 (FIG. 2), for example, the transistor 2301 is included in the circuit 11 and the transistor 2302 and the capacitor 2303 are included in the circuit RC2. Specifically, the transistor 2301 is included in an analog switch electrically connected to the terminal a20 of the circuit SELC1. The transistor 2302 and the capacitor 2303 correspond to any of the switches SW1, SW2, and SW3 in the circuit RC1 and the capacitor CP1, respectively.

[0164]

The Si transistor and the OS transistor are stacked as illustrated in FIG. 11, whereby circuits can be three-dimensionally integrated over the semiconductor substrate. For this reason, area overhead can be zero even when a circuit including an OS transistor is added to the semiconductor device.

5 [0165]

In the example in FIG. 11, the OS transistor 2302 and the capacitor 2303 are formed in the same element tier. However, the capacitor 2303 can be stacked over the OS transistor 2302, for example, in which case the electrostatic capacitance of the capacitor 2303 can be increased without increasing the circuit area.

10 [0166]

As the substrate 2201, a single crystal semiconductor substrate, a polycrystalline semiconductor substrate, a silicon on insulator (SOI) substrate, or the like made of silicon, silicon carbide, silicon germanium, or the like can be used. A transistor formed using a semiconductor substrate can easily operate at high speed. In the case of using a p-type single crystal silicon substrate as the substrate 2201, an impurity element imparting n-type conductivity may be added to part of the substrate 2201 to form an n-well, and a p-type transistor can be formed in a region where the n-well is formed. As the impurity element imparting n-type conductivity, phosphorus (P), arsenic (As), or the like can be used. As the impurity element imparting p-type conductivity, boron (B) or the like may be used.

[0167]

Alternatively, the substrate 2201 can be a conductor substrate or an insulating substrate provided with a semiconductor film. Examples of the conductor substrate include a metal substrate, a stainless steel substrate, a substrate including stainless steel foil, a tungsten substrate, and a substrate including tungsten foil. Examples of the insulating substrate include a glass substrate, a quartz substrate, a plastic substrate, a flexible substrate, an attachment film, paper including a fibrous material, and a base film. Examples of the glass substrate are a barium borosilicate glass substrate, an aluminoborosilicate glass substrate, and a soda lime glass substrate. Examples of the flexible substrate are flexible synthetic resin substrates such as substrates of plastics typified by polyethylene terephthalate (PET), polyethylene naphthalate (PEN), and polyether sulfone (PES) and an acrylic substrate. Examples of the attachment film are

attachment films formed using polypropylene, polyester, polyvinyl fluoride, polyvinyl chloride, and the like. Examples of the base film are base films formed using polyester, polyamide, polyimide, aramid, epoxy, an inorganic vapor deposition film, and paper.

[0168]

5 Here, a single crystal silicon substrate is used as the substrate 2201. Thus, the transistor 2301 is a Si transistor whose semiconductor region contains single crystal silicon. Hereinafter, the transistor 2301 is sometimes referred to as the Si transistor 2301 and the transistor 2302 is sometimes referred to as the OS transistor 2302.

[0169]

10 In FIG. 11, the reference numeral 2204 indicates an element isolation layer. The Si transistor 2301 includes an impurity region 2001, an impurity region 2002, a gate electrode 2003, a gate insulating film 2004, and a sidewall insulating layer 2005. The impurity region 2001 serves as a source region or a drain region. The impurity region 2002 serves as a lightly doped drain (LDD) region or an extension region.

15 [0170]

 Although the Si transistor 2301 is a planar type transistor in the example illustrated in FIG. 11, the Si transistor 2301 can be any of a variety of types of transistors instead of a planar type transistor. For example, a transistor whose semiconductor region has a three-dimensional structure, such as a FIN-type transistor or a tri-gate transistor can be used. The OS transistor 2302 in the example in FIG. 11 includes a back gate; however, a structure without a back gate may be employed.

[0171]

 Hydrogen in an insulating film provided in the vicinity of the semiconductor region of the Si transistor 2301 terminates dangling bonds of silicon; accordingly, the reliability of the Si transistor 2301 can be improved. On the other hand, hydrogen in the insulating film is a factor of generating carriers in an oxide semiconductor of an oxide semiconductor layer of the OS transistor 2302 provided in an upper tier. Thus, in the case where the OS transistor 2302 is stacked over the Si transistor 2301 as illustrated in FIG. 11, it is particularly effective that an insulating film 2207 having a function of preventing hydrogen diffusion is provided between the transistors 2301 and 2302. The insulating film 2207 can trap hydrogen in a lower tier (on the substrate 2201 side), which improves the reliability of both the Si transistor 2301 and the OS

transistor 2302.

[0172]

The insulating film 2207 can be formed using, for example, a film containing aluminum oxide, aluminum oxynitride, gallium oxide, gallium oxynitride, yttrium oxide, yttrium oxynitride, hafnium oxide, hafnium oxynitride, yttria-stabilized zirconia (YSZ), or the like, so as to serve as a film for preventing hydrogen diffusion.

[0173]

It is preferable that an insulating film 2208 that covers the OS transistor 2302 be also formed using an insulating film having a function of preventing hydrogen diffusion like the insulating film 2207. It is particularly preferable that an aluminum oxide film be used as the insulating film 2208. The aluminum oxide film has a high shielding (blocking) effect of preventing penetration of both oxygen and impurities such as hydrogen and moisture. Thus, when the OS transistor 2302 is covered with the aluminum oxide film, release of oxygen from the oxide semiconductor layer of the OS transistor 2302 and entry of water and hydrogen into the oxide semiconductor layer can be prevented. In the example in FIG. 11, the insulating film 2208 also serves as a dielectric of the capacitor 2303.

[0174]

(Embodiment 4)

A sequential circuit such as a flip-flop circuit are used for integrated circuits of electronic devices in a wide variety of fields, such as digital signal processing, software-defined radio systems, avionic systems (electronic devices used in aircraft, such as communication systems, navigation systems, autopilot systems, and flight management systems), ASIC prototyping, medical image processing, voice recognition, encryption, bioinformatics, emulators for mechanical systems, ICs for controlling and/or protecting batteries (second batteries), and radio telescopes in radio astronomy. In addition, the holding circuit described in Embodiment 1 can be used in a memory device that backs up the state (data) of the sequential circuit. Thus, the semiconductor device described in Embodiment 1 or the like can be incorporated in a variety of semiconductor devices. In this embodiment, a processing unit for processing data will be described as an example of such a semiconductor device.

[0175]

<<CPU>>

FIG. 12 illustrates a CPU configuration example. A CPU 300 illustrated in FIG. 12 includes a CPU core 301, a power management unit 321, and a peripheral circuit 322. The power management unit 321 includes a power controller 302 and a power switch 303. The peripheral circuit 322 includes a cache 304 including cache memory, a bus interface (BUS I/F) 305, and a debug interface (Debug I/F) 306. The CPU core 301 includes a data bus 323, a control unit 307, a program counter (PC) 308, a pipeline register 309, a pipeline register 310, an arithmetic logic unit (ALU) 311, and a register file 312. Data is transmitted between the CPU core 301 and the peripheral circuit 322 such as the cache 304 via the data bus 323.

[0176]

The control unit 307 has functions of decoding and executing instructions contained in a program such as inputted applications by controlling the overall operations of the PC 308, the pipeline registers 309 and 310, the ALU 311, the register file 312, the cache 304, the bus interface 305, the debug interface 306, and the power controller 302.

[0177]

The ALU 311 has a function of performing a variety of arithmetic operations such as four arithmetic operations and logic operations. The cache 304 has a function of temporarily storing frequently used data. The PC 308 is a register having a function of storing an address of an instruction to be executed next. Although not illustrated in FIG. 12, the cache 304 includes a cache controller for controlling the operation of the cache memory.

[0178]

The pipeline register 309 has a function of temporarily storing instruction data. The register file 312 includes a plurality of registers including a general purpose register and can store data that is read from the main memory, data obtained as a result of arithmetic operations in the ALU 311, or the like. The pipeline register 310 has a function of temporarily storing data used for arithmetic operations performed in the ALU 311, data obtained as a result of arithmetic operations in the ALU 311, or the like.

[0179]

The bus interface 305 serves as a path for data between the CPU 300 and

devices outside the CPU 300. The debug interface 306 serves as a path of a signal for inputting an instruction to control debugging to the CPU 300.

[0180]

The power switch 303 has a function of controlling supply of the power supply potential to circuits other than the power controller 302 in the CPU 300. These circuits belong to several different power domains. The power switch 303 controls whether the power supply potential is supplied to circuits in the same power domain. The power controller 302 has a function of controlling the operation of the power switch 303. The CPU 300 with such a configuration can use power gating. An example of a power gating control will be described.

[0181]

First, the CPU core 301 sets the timing for stopping the supply of the power supply potential in a register of the power controller 302. Next, an instruction to start power gating is sent from the CPU core 301 to the power controller 302. Then, the registers and the cache 304 in the CPU 300 start data storing. Subsequently, the power switch 303 stops the supply of the power supply potential to the circuits other than the power controller 302 in the CPU 300. Then, an interrupt signal is input to the power controller 302, thereby starting the supply of the power supply potential to the circuits included in the CPU 300. Note that a counter may be provided in the power controller 302 to be used to determine the timing of starting the supply of the power supply potential regardless of input of an interrupt signal. Next, the registers and the cache 304 start data restoration. After that, execution of an instruction is resumed in the control unit 307.

[0182]

This power gating can be used in the entire processing unit or one or more logic circuits included in the processing unit. The semiconductor device of Embodiment 1 or the like achieves power gating at a fine granularity in space or time, leading to a reduction in power consumption of the entire processing unit.

[0183]

Although a CPU is described here as the processing unit, the semiconductor device of one embodiment of the present invention can be applied to a variety of processing units. For example, the semiconductor device is applicable to an RFID tag,

a graphics processing unit (GPU), a programmable logic device (PLD), a digital signal processor (DSP), a microcontroller unit (MCU), a custom LSI, and the like.

[0184]

(Embodiment 5)

5 In this embodiment, an electronic component and electronic devices and the like including the electronic component will be described as examples of a semiconductor device.

[0185]

<Example of Manufacturing Method of Electronic Component>

10 FIG. 13A is a flow chart showing an example of a method for manufacturing an electronic component. The electronic component is also referred to as a semiconductor package or an IC package. This electronic component has a plurality of standards and names depending on a terminal extraction direction and a terminal shape. Thus, examples of the electronic component are described in this embodiment.

15 [0186]

A semiconductor device including a transistor can be completed after an assembly process (post-process) by using a plurality of components that can be detached and attached from and to a printed wiring board in combination. The post-process can be finished through each step in FIG. 13A. Specifically, after an
20 element substrate obtained in the preceding process is completed (Step S1), a rear surface of the substrate is ground (Step S2). By thinning the substrate at this stage, the warpage or the like of the substrate in the preceding process is reduced and the component is downsized.

[0187]

25 The rear surface of the substrate is ground so that the substrate is divided into a plurality of chips in a dicing process. Then, the divided chips are separately picked up to be mounted on and bonded to a lead frame in a die bonding process (Step S3). In this die bonding process, the chip is bonded to the lead frame by an appropriate method depending on a product, for example, bonding with a resin or a tape. Note that in the
30 die bonding process, the chip may be mounted on an interposer to be bonded.

[0188]

Then, wire bonding is performed to electrically connect lead of the lead frame

to an electrode on the chip with a metal fine line (wire) (Step S4). A silver line or a gold line can be used as the metal fine line. Ball bonding or wedge bonding can be used as the wire bonding.

[0189]

- 5 A molding process is performed to seal the wire bonded chip with an epoxy resin or the like (Step S5). With the molding process, the electronic component is filled with the resin, so that damage to a mounted circuit portion or wire due to mechanical external force can be reduced. Furthermore, deterioration in characteristics due to moisture or dust can be reduced.

10 [0190]

Next, plate processing is performed on the lead of the lead frame. After that, the lead is cut and processed (Step S6). This plate processing prevents rust of the lead and facilitates soldering at the time of mounting the chip on a printed wiring board in a later step.

15 [0191]

Next, printing (marking) is performed on a surface of the package (Step S7). Through the final inspection process (Step S8), the electronic component is completed (Step S9).

[0192]

- 20 The above electronic component can include the semiconductor device described in the above embodiment. Thus, the electronic component can consume less power and have smaller size.

[0193]

- FIG. 13B is a schematic perspective view of the completed electronic component. FIG. 13B illustrates a schematic perspective view of a quad flat package (QFP) as an example of the electronic component. As illustrated in FIG. 13B, an electronic component 700 includes a lead 701 and a circuit portion 703. The electronic component 700 is mounted on a printed wiring board 702, for example. When a plurality of electronic components 700 are used in combination and electrically connected to each other over the printed wiring board 702, the electronic components 700 can be mounted on an electronic device. A completed circuit board 704 is provided in the electronic device or the like. The electronic component 700 can be
- 25
- 30

used as, for example, a random access memory that stores data or a processing unit that executes a variety of types of processing, such as a microcontroller unit (MCU) or an RFID tag.

[0194]

5 The electronic component 700 can be used as electronic component (an IC chip) of electronic devices in a wide variety of fields, such as digital signal processing, software-defined radio systems, avionic systems (electronic devices used in aircraft, such as communication systems, navigation systems, autopilot systems, and flight management systems), ASIC prototyping, medical image processing, voice recognition, encryption, bioinformatics, emulators for mechanical systems, and radio telescopes in radio astronomy. Such an electric device can be used for display devices, personal computers (PCs), or image reproducing devices provided with recording media (typically, devices which reproduce the content of recording media such as digital versatile discs (DVDs) and have displays for displaying the reproduced images).

10 Other examples of electronic appliances that can be equipped with the semiconductor device of one embodiment of the present invention are mobile phones, game machines including portable game machines, portable data appliances, e-book readers, cameras (e.g., video cameras and digital still cameras), wearable display devices (e.g., head mounted display devices, goggle-type display devices, glasses-type display devices, armband display devices, bracelet-type display devices, and necklace-type display devices), navigation systems, audio reproducing devices (e.g., car audio systems and digital audio players), copiers, facsimiles, printers, multifunction printers, automated teller machines (ATM), and vending machines. FIGS. 14A to 14F illustrate specific examples of these electronic devices.

25 [0195]

 A portable game machine 900 illustrated in FIG. 14A includes a housing 901, a housing 902, a display portion 903, a display portion 904, a microphone 905, a speaker 906, an operation key 907, a stylus 908, and the like.

[0196]

30 The portable information terminal 910 illustrated in FIG. 14B includes a housing 911, a housing 912, a display portion 913, a display portion 914, a joint 915, an operation key 916, and the like. The display portion 913 is provided in the housing

911, and the display portion 914 is provided in the housing 912. The housings 911 and 912 are connected to each other with the joint 915, and an angle between the housings 911 and 912 can be changed with the joint 915. An image on the display portion 913 may be switched depending on the angle between the housings 911 and 912 at the joint 915. A display device with a touch panel may be used as the display portion 913 and/or the display portion 914.

[0197]

A notebook PC 920 illustrated in FIG. 14C includes a housing 921, a display portion 922, a keyboard 923, a pointing device 924, and the like.

[0198]

An electric refrigerator-freezer 930 illustrated in FIG. 14D includes a housing 931, a refrigerator door 932, a freezer door 933, and the like.

[0199]

A video camera 940 illustrated in FIG. 14E includes a housing 941, a housing 942, a display portion 943, operation keys 944, a lens 945, a joint 946, and the like. The operation keys 944 and the lens 945 are provided in the housing 941, and the display portion 943 is provided in the housing 942. The housings 941 and 942 are connected to each other with the joint 946, and an angle between the housings 941 and 942 can be changed with the joint 946. The direction of an image on the display portion 943 may be changed and display and non-display of an image may be switched depending on the angle between the housings 941 and 942.

[0200]

FIG. 14F is an external view illustrating a structure example of a motor vehicle. A motor vehicle 950 includes a car body 951, wheels 952, a dashboard 953, lights 954, and the like.

[0201]

An electronic component including the semiconductor device described in the above embodiment is provided in each of the electronic devices described in this embodiment. Thus, an electronic device that consumes less power and has smaller size can be provided.

[0202]

In this specification, for example, any of the following expressions can be used

for the case where a source (or a first terminal or the like) of a transistor is electrically connected to X through (or not through) $Z1$ and a drain (or a second terminal or the like) of the transistor is electrically connected to Y through (or not through) $Z2$, or the case where a source (or a first terminal or the like) of a transistor is directly connected to one part of $Z1$ and another part of $Z1$ is directly connected to X while a drain (or a second terminal or the like) of the transistor is directly connected to one part of $Z2$ and another part of $Z2$ is directly connected to Y .

[0203]

Examples of the expressions include, " X , Y , a source (or a first terminal or the like) of a transistor, and a drain (or a second terminal or the like) of the transistor are electrically connected to each other, and X , the source (or the first terminal or the like) of the transistor, the drain (or the second terminal or the like) of the transistor, and Y are electrically connected to each other in this order", "a source (or a first terminal or the like) of a transistor is electrically connected to X , a drain (or a second terminal or the like) of the transistor is electrically connected to Y , and X , the source (or the first terminal or the like) of the transistor, the drain (or the second terminal or the like) of the transistor, and Y are electrically connected to each other in this order", and " X is electrically connected to Y through a source (or a first terminal or the like) and a drain (or a second terminal or the like) of a transistor, and X , the source (or the first terminal or the like) of the transistor, the drain (or the second terminal or the like) of the transistor, and Y are provided to be connected in this order". When the connection order in a circuit structure is defined by an expression similar to the above examples, a source (or a first terminal or the like) and a drain (or a second terminal or the like) of a transistor can be distinguished from each other to specify the technical scope. Note that one embodiment of the present invention is not limited to these expressions that are just examples. Here, X , Y , $Z1$, and $Z2$ each denote an object (e.g., a device, an element, a circuit, a wiring, an electrode, a terminal, a conductive film, a layer, or the like).

[0204]

Note that in this specification and the like, it might be possible for those skilled in the art to constitute one embodiment of the invention even when portions to which all the terminals of an active element (e.g., a transistor or a diode), a passive element (e.g., a capacitor or a resistor), or the like are connected are not specified. In other words,

one embodiment of the invention is clear even when connection portions are not specified. Furthermore, in the case where a connection portion is disclosed in this specification and the like, it can be determined that one embodiment of the invention in which a connection portion is not specified is disclosed in this specification and the like, in some cases. In particular, in the case where the number of portions to which the terminal is connected is plural, it is not necessary to specify the portions to which the terminal is connected. Therefore, it might be possible to constitute one embodiment of the invention by specifying only portions to which some of terminals of an active element (e.g., a transistor or a diode), a passive element (e.g., a capacitor or a resistor), or the like are connected.

[0205]

Note that in this specification and the like, it might be possible for those skilled in the art to specify the invention when at least the connection portion of a circuit is specified. Alternatively, it might be possible for those skilled in the art to specify the invention when at least the function of a circuit is specified. In other words, one embodiment of the present invention is clear when the function of a circuit is specified. Furthermore, it can be determined that one embodiment of the present invention in which a function is specified is disclosed in this specification and the like in some cases. Thus, when the connection portion of a circuit is specified, the circuit is disclosed as one embodiment of the invention even if a function is not specified, and one embodiment of the invention can be constituted. Alternatively, when the function of a circuit is specified, the circuit is disclosed as one embodiment of the invention even when a connection portion is not specified, and one embodiment of the invention can be constituted.

EXPLANATION OF REFERENCE

[0206]

100: semiconductor device, 101: semiconductor device, 111: semiconductor device, 112: semiconductor device, 113: semiconductor device, 114: semiconductor device, 10: circuit, 20: circuit, 30: circuit, and RC1: circuit.

This application is based on Japanese Patent Application serial no.

2014-081831 filed with Japan Patent Office on April 11, 2014, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A holding circuit comprising:

a first input terminal;

a second input terminal;

a third input terminal;

a first output terminal;

a first switch;

a second switch;

a third switch;

a capacitor; and

a node,

wherein the first switch is configured to control conduction between the node and the first input terminal,

wherein the second switch is configured to control conduction between the node and the first output terminal,

wherein the third switch is configured to control conduction between the second input terminal and the first output terminal,

wherein a first terminal of the capacitor is electrically connected to the node,

wherein a second terminal of the capacitor is electrically connected to the third input terminal, and

wherein the first switch and the second switch are each a transistor comprising an oxide semiconductor layer.

2. The holding circuit according to claim 1, wherein the third switch is a transistor comprising an oxide semiconductor layer.

3. The holding circuit according to claim 1, wherein the oxide semiconductor layer comprises indium, gallium, and zinc.

4. The holding circuit according to claim 1, wherein the oxide semiconductor layer has a crystal part with c-axis alignment.

5. A semiconductor device comprising:
the holding circuit according to claim 1; and
a circuit comprising:

- a fourth input terminal;
- a fifth input terminal;
- a second output terminal;
- a selection circuit; and
- a sequential circuit,

wherein the selection circuit is configured to control conduction between an input terminal of the sequential circuit and one of the fourth input terminal and the fifth input terminal,

wherein the second output terminal is electrically connected to an output terminal of the sequential circuit,

wherein the first output terminal of the holding circuit is electrically connected to the fifth input terminal, and

wherein the first input terminal of the holding circuit is electrically connected to the fourth input terminal, the second output terminal, or an internal node of the sequential circuit.

6. The semiconductor device according to claim 5, wherein one of the first input terminal and the first output terminal is electrically connected to one of a buffer circuit and an inverter circuit.

7. The semiconductor device according to claim 5, wherein the circuit comprises a transistor comprising silicon.

8. The semiconductor device according to claim 5 comprising:
a CPU core.

9. An electronic device comprising:

the semiconductor device according to claim 5; and

one of a housing, a microphone, a speaker, a display portion, and an operation key.

10. A method for driving a holding circuit comprising a first input terminal, a second input terminal, a third input terminal, an output terminal, a first switch, a second switch, a third switch, a capacitor, and a node, comprising a first processing comprising the steps of:

turning off the first switch and turning on the second switch and the third switch;

inputting a first potential to the second input terminal; and

inputting a second potential to the third input terminal,

wherein a first terminal of the first switch is electrically connected to the first input terminal,

wherein a second terminal of the first switch is electrically connected to the node,

wherein a first terminal of the second switch is electrically connected to the node,

wherein a second terminal of the second switch is electrically connected to the output terminal,

wherein a first terminal of the third switch is electrically connected to the second input terminal,

wherein a second terminal of the third switch is electrically connected to the output terminal,

wherein a first terminal of the capacitor is electrically connected to the node,

wherein a second terminal of the capacitor is electrically connected to the third input terminal, and

wherein the first switch and the second switch are each a transistor comprising an oxide semiconductor layer.

11. The method according to claim 10, wherein the third switch is a transistor comprising an oxide semiconductor layer.

12. The method according to claim 10, wherein the oxide semiconductor layer has a crystal part with c-axis alignment.

13. The method according to claim 10, wherein the oxide semiconductor layer comprises indium, gallium, and zinc.

14. The method according to claim 10, wherein the first potential is capable of making a logic level of the node low.

15. The method according to claim 10 comprising:
a second processing after the first processing; and
a third processing after the second processing,
wherein the second processing comprises the steps of:
turning on the first switch and turning off the second switch and the third switch;
and
inputting a third potential that is higher than the second potential to the third input terminal, and
wherein the third processing comprises the steps of:
turning off the first switch, the second switch, and the third switch; and
inputting the third potential to the third input terminal.

16. The method according to claim 10 comprising:
a second processing after the first processing; and
a third processing after the second processing,
wherein the second processing comprises the steps of:
turning off the first switch and turning on the second switch and the third switch;
and
inputting a third potential that is higher than the second potential to the third input terminal, and
wherein the third processing comprises the steps of:
turning off the first switch, the second switch, and the third switch; and
inputting the third potential to the third input terminal.

17. The method according to claim 16 comprising:

a fourth processing after the third processing,

wherein the fourth processing comprises the steps of:

turning off the first switch and the third switch;

turning on the second switch; and

inputting the third potential to the third input terminal.

18. A semiconductor device comprising:

a holding circuit comprising:

a first switch;

a second switch;

a third switch;

a capacitor; and

a node,

a circuit, an input terminal of the circuit being electrically connected to an output terminal of the holding circuit, comprising:

a sequential circuit; and

a selection circuit electrically connected between the input terminal of the circuit and the sequential circuit,

wherein a first terminal of the first switch is electrically connected to a first input terminal of the holding circuit,

wherein a second terminal of the first switch is electrically connected to the node,

wherein a first terminal of the second switch is electrically connected to the node,

wherein a second terminal of the second switch is electrically connected to the output terminal,

wherein a first terminal of the third switch is electrically connected to a second input terminal of the holding circuit,

wherein a second terminal of the third switch is electrically connected to the output terminal,

wherein a first terminal of the capacitor is electrically connected to the node,

wherein a second terminal of the capacitor is electrically connected to a third input terminal of the holding circuit, and

wherein the first switch and the second switch are each a transistor comprising an oxide semiconductor layer.

19. The semiconductor device according to claim 18, wherein the third switch is a transistor comprising an oxide semiconductor layer.

20. The semiconductor device according to claim 18, wherein the oxide semiconductor layer comprises indium, gallium, and zinc.

21. The semiconductor device according to claim 18, wherein the oxide semiconductor layer has a crystal part with c-axis alignment.

22. The semiconductor device according to claim 18, wherein the circuit comprises a transistor comprising silicon.

23. The semiconductor device according to claim 18, wherein the first input terminal of the holding circuit is electrically connected to the input terminal of the circuit, an output terminal of the circuit, or an internal node of the sequential circuit.

24. The semiconductor device according to claim 18, wherein one of the first input terminal and the output terminal is electrically connected to one of a buffer circuit and an inverter circuit.

25. The semiconductor device according to claim 18 comprising:
a CPU core.

26. An electronic device comprising:
the semiconductor device according to claim 18; and
one of a housing, a microphone, a speaker, a display portion, and an operation key.