

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:
a substrate including active regions;
word lines in the substrate, each of the word lines extending in a first direction parallel to an upper surface of the substrate;
bit line structures connected to the active regions, respectively, and each of the bit line structures extending in a second direction crossing the first direction; and
spacer structures on sidewalls of respective ones of the bit line structures,
each of the spacer structures including a first spacer, a second spacer, and a third spacer,
the second spacer being disposed between the first spacer and the third spacer,
the second spacer including at least one void defined by an inner surface of the second spacer, the at least one void being spaced apart from the first spacer and the third spacer by a portion of the second spacer, and
a height of the second spacer being greater than a height of the at least one void with respect to the upper surface of the substrate.
2. The semiconductor memory device according to claim 1, wherein
a thickness of the second spacer is greater than a thickness of the first spacer, and
the thickness of the second spacer is greater than the thickness of the third spacer.
3. The semiconductor memory device according to claim 1, wherein

the height of the at least one void corresponds to a major axis of the at least one void, and the major axis of the at least one void extends in a third direction perpendicular to the upper surface of the substrate.

4. The semiconductor memory device according to claim 1, further comprising:
contact plugs between each of the bit line structures, the contact plugs being connected to the active regions, respectively;
connection pads on the contact plugs, respectively; and
a separation layer between each of the connection pads.

5. The semiconductor memory device according to claim 4, wherein a lowermost surface of the separation layer is higher than an uppermost surface of the second spacer with respect to the upper surface of the substrate.

6. The semiconductor memory device according to claim 5, wherein
an upper surface of the third spacer is lower than an upper surface of the first spacer with respect to the upper surface of the substrate,
an upper surface of the second spacer is lower than the upper surface of the third spacer with respect to the upper surface of the substrate, and
each of the spacer structures further include a fourth spacer on a sidewall of the first spacer and on the upper surface of the second spacer.

7. The semiconductor memory device according to claim 4, wherein a lowermost surface of the separation layer contacts an uppermost surface of the second spacer.

8. The semiconductor memory device according to claim 7, further comprising:
fence insulating patterns between each of the contact plugs, wherein
the second spacer includes first portions and second portions,
the first portions of the second spacer are between each of the contact plugs and each
of the bit line structures,
the second portions of the second spacer are between the each of the fence insulating
patterns and each of the bit line structures, and
the separation layer contacts at least one of the first portions of the second spacer or
the second portions of the second spacer.

9. The semiconductor memory device according to claim 8, wherein upper
surface of the first portions of the second spacer are positioned at a level different from upper
surfaces of the second portions of the second spacer with respect to the upper surface of the
substrate.

10. A semiconductor memory device comprising:
a substrate including an active region;
a bit line structure on the substrate, the bit line structure being connected to the active
regions; and
a spacer structure on a sidewall of the bit line structure,
the spacer structure including a first spacer, a second spacer, and a third spacer
that are sequentially disposed on the sidewall of the bit line structure,
the second spacer including a void defined by an inner surface of the second
spacer, the void being spaced apart from the first spacer and the third spacer by a portion of
the second spacer, and

an upper surface of the third spacer being lower than an upper surface of the first spacer with respect to an upper surface of the substrate.

11. The semiconductor memory device according to claim 10, wherein the first spacer extends below the second spacer.

12. The semiconductor memory device according to claim 10, further comprising:
contact plugs connected to the active region, respectively;
connection pads on the contact plugs, respectively; and
a separation insulation layer between the connection pads,
wherein an upper surface of the second spacer is spaced apart from a lower surface of the separation insulation layer.

13. A method of manufacturing a semiconductor memory device, comprising:
forming active regions in a substrate;
forming bit line structures on the substrate, the bit line structures crossing the active regions;
forming spacer structures on sidewalls of the bit line structures, respectively, the forming the spacer structures including,
sequentially forming a first spacer, a sacrificial spacer, and a third spacer on each of the sidewalls of the bit line structures,
removing the sacrificial spacer to form a gap region, and

forming a second spacer in the gap region, an inner surface of the second spacer defining a void that is surrounded by a portion of the second spacer, the void being spaced apart from the first spacer and the third spacer by the portion of the second spacer;

forming contact plugs between each of the bit line structures, the contact plugs for connecting to the active regions, respectively.

14. The method according to claim 13, further comprising:

forming connection pads on the contact plugs, respectively, after the forming the second spacer.

15. The method according to claim 14, further comprising:

forming fence insulating patterns crossing the bit line structures, the forming fence insulating patterns including defining contact regions facing sidewalls of adjacent ones of the bit line structures and facing sidewalls of adjacent ones of the fence insulating patterns,

the forming contact plugs includes forming the contact plugs in lower portions of the contact regions, respectively,

the removing the sacrificial spacer is performed after the forming the contact plugs in lower portions of the contact regions, respectively, and

the sacrificial spacer is removed through the contact regions.

16. The method according to claim 13, further comprising:

forming connection pads on the contact plugs, respectively,

wherein the forming connection pads is performed before the forming of the second spacer.

17. The method according to claim 16, wherein
the forming of the connection pads includes forming a metal layer, and forming a separation region by patterning the metal layer, and
the removing the sacrificial spacer includes removing the sacrificial spacer through the separation region.

18. The method according to claim 17, further comprising:
forming fence insulating patterns on the substrate, the fencing insulating patterns crossing the bit line structures, wherein
the separation region exposes at least one of,
first portions of the sacrificial spacer between each of the contact plugs and each of the bit line structures, or
second portions of the sacrificial spacer between each of the fence insulating patterns and each of the bit line structures.

19. The method according to claim 13, wherein the first spacer and the second spacer include a material having an etch selectivity with respect to the sacrificial spacer.

20. The method according to claim 13, wherein the removing the sacrificial spacer includes reducing a thickness of the first spacer and a thickness of the third spacer.