CLAIMS

1. A method for fabricating a semiconductor wafer for use as a solar collector, the method comprising the steps of:

a. providing a molten semiconductor material, having a surface;

b. providing a mold, comprising a forming surface, the mold also comprising a primary dopant relative to the semiconductor material;

c. contacting the forming surface to the molten material such that dopant migrates from the mold into the molten semiconductor material; and

d. maintaining conditions such that a body of semiconductor material in the form of a wafer solidifies upon the forming surface, with a first surface contacting the forming surface, the wafer having a profile of dopant concentration, there being a larger concentration of dopant at the first surface of the wafer, and a lesser concentration of dopant at a second surface of the wafer.

2. The method of claim 1, further comprising the step of detaching the solidified wafer from the forming surface.

3. The method of claim 1, the mold comprising a coating on one surface, which coating contains the primary dopant.

4. The method of claim 1, the mold further comprising a body, wherein the primary dopant is distributed within the mold body.

5. The method of claim 1, the mold further comprising a body, wherein the primary dopant is within the mold body at a higher concentration near one surface.

6. The method of claim 1, the primary dopant comprising a charge carrier of one type only of a donor and an acceptor type, further comprising;

conducting steps a, b, c, and d (of claim 1) at least two times;

providing in the molten material, a quantity of compensating dopant of an opposite charge carrier donor/acceptor type to the primary dopant.

7. The method of claim 6, further comprising, the step of providing in the molten material, a quantity of counter compensating dopant of an opposite charge carrier donor/acceptor type to the compensating dopant.

8. The method of claim 7, the compensating and the counter compensating dopants each having an equilibrium segregation coefficient, the equilibrium segregation coefficient of the counter compensating dopant being equal to or less than the equilibrium segregation coefficient of the compensating dopant.

9. The method of claim 6 where the step of providing a quantity of compensating dopant is accomplished by providing the compensating dopant in the melt at a concentration C_{cd} according to the following relation:

C_{cd} approximately equals $C_{md}*(k_{md}/k_{cd})$ where:

C_{md} is the melt concentration of the primary dopant;

C_{cd} is the melt concentration of the compensating dopant;

k_{md} is the effective segregation coefficient of the primary dopant; and

k_{cd} is the effective segregation coefficient of the compensating dopant.

10. The method of claim 1, the primary dopant concentration being less than or equal to 1 x 10^{20} N_x/cm^3 at the first surface of the wafer and greater than or equal to about 1 x 10^{15} N_x/cm^3 at the second surface of the wafer, where N_x means for a charge carrier acceptor dopant, the number of charge carrier acceptors N_a and, for a charge carrier donor dopant, the number of charge carrier donors N_d.

11. The method of claim 1, the primary dopant concentration being less than or equal to 1 x 10^{19} N_x/cm^3 at the first surface of the wafer and greater than or equal to about 1 x 10^{17} N_x/cm^3 at the second surface of the wafer, where N_x means for a charge carrier acceptor dopant, the number of charge carrier acceptors N_a and, for a charge carrier donor dopant, the number of charge carrier donors N_d.

12. The method of claim 1, the semiconductor comprising a p-type semiconductor, the primary dopant being chosen from the group consisting of: boron, aluminum, gallium and indium.

13. The method of claim 1, the semiconductor comprising an n-type semiconductor, the primary dopant being chosen from the group consisting of: phosphorous, arsenic, Antimony (Sb) and bismuth.

14. The method of claim 6, the semiconductor comprising a p-type semiconductor, the compensating dopant being chosen from the group consisting of: phosphorous, arsenic, antimony (Sb) and Bismuth.

15. The method of claim 6, the semiconductor comprising an n-type semiconductor, the compensating dopant being chosen from the group consisting of boron, aluminum, gallium and indium.

16. The method of claim 14, further comprising the step of providing in the molten material, a counter compensating dopant selected from the group consisting of: aluminum, gallium and Indium.

17. The method of claim 15, further comprising the step of providing in the molten material, a counter compensating dopant selected from the group consisting of: arsenic, antimony and bismuth.

18. The method of claim 1, the molten material comprising silicon and the primary dopant comprising a compound selected from the group consisting of a carbide, an oxide, a nitride and a silicide, or an element selected from the group consisting of: boron, aluminum, gallium, indium, phosphorous, arsenic, antimony and bismuth.

19. The method of claim 1, the step of maintaining being conducted so as to provide a concentration of primary dopant at the first surface of the wafer sufficiently high so as to establish a back surface field in a wafer used as a solar collector.

20. The method of claim 1, the profile of dopant concentration having a shape that will give rise to a drift electric field within the wafer body directed to urge charge carriers in a preferred direction.

21. A semiconductor wafer for use as a solar collector, the wafer comprising a body having a first and a second surface, the body having a dopant concentration profile, there being a larger concentration of dopant at a first surface of the wafer, and a continuous transition to a lesser concentration of dopant at a second surface of the wafer, the larger concentration being at least three times the lesser concentration.

22. The semiconductor wafer of claim 21, the semiconductor comprising silicon, and the dopant comprising boron.

23. The semiconductor wafer of claim 21, the semiconductor comprising silicon and the dopant being selected from the group consisting of: boron, aluminum, gallium and indium.

24. The semiconductor wafer of claim 21, the semiconductor comprising a p-type semiconductor and the dopant being selected from the group consisting of: boron, aluminum, gallium and indium.

25. The semiconductor wafer of claim 21, the semiconductor comprising an n-type semiconductor and the dopant being selected from the group consisting of: phosphorous, arsenic, Antimony (Sb) and bismuth.

26. The semiconductor wafer of claim 21, the dopant concentration being less than or equal to 1×10^{20} N_x/cm^3 at the first surface of the wafer and greater than or equal to about 1×10^{15} N_x/cm^3 at the second surface of the wafer, where N_x means, for a charge carrier acceptor dopant, the number of charge carrier acceptors N_a and, for a charge carrier donor dopant, the number of charge carrier donors N_d.

27. The semiconductor wafer claim 21, the concentration of primary dopant at the first surface of the wafer being sufficiently high so as to establish a back surface field in a wafer used as a solar collector.

28. The semiconductor wafer of claim 21, the profile of dopant concentration having a shape that will give rise to a drift electric field within the wafer body directed to urge charge carriers in a preferred direction.

29. A solar collector comprising a plurality of semiconductor wafers, each wafer comprising a body having a first and a second surface, the body having a dopant concentration profile, there being a larger concentration of dopant at a first surface of the wafer, and a continuous transition to a lesser concentration of dopant at a second surface of the wafer, the larger concentration being at least three times the lesser concentration, further, where any metallic impurities that are present in the body are present at the first surface to a degree less than ten times the degree of metallic impurities that are present at the second surface.

30. A solar collector comprising a plurality of semiconductor wafers, each wafer comprising a body having a first and a second surface, the body having a profile of resistivity, there being a relatively lesser resistivity at a first surface of the wafer, and a continuous transition to a relatively larger resistivity at a second surface of the wafer, further, where any metallic impurities that are present in the body are present at the first surface to a degree less than ten times the degree of metallic impurities that are present at the second surface.