What is Claimed is:

1. An integrated circuit semiconductor device comprising:

a nanosheet provided on a substrate, the nanosheet extending in a first horizontal direction;

a gate electrode comprising a first gate electrode portion provided on an upper side of the nanosheet and a second gate electrode portion provided on a lower side of the nanosheet, the gate electrode extending in a second horizontal direction that is perpendicular to the first horizontal direction;

a gate insulating layer provided between the gate electrode and the nanosheet;

a first source/drain region provided on a first side of the nanosheet corresponding to the gate electrode; and

a second source/drain region provided on a second side of the nanosheet corresponding to the gate electrode,

wherein the first source/drain region comprises:

first silicide layers comprising a first upper silicide layer provided on the nanosheet and extending inward from an upper surface of the nanosheet, and a first lower silicide layer on provided the nanosheet and extending inward from a lower surface of the nanosheet,

a first upper metal layer provided on the first upper silicide layer and a first lower metal layer provided on the first lower silicide layer, and

a first nanosheet region provided between the first upper silicide layer and the first lower silicide layer,

wherein the second source/drain region comprises:

second silicide layers comprising a second upper silicide layer provided on the nanosheet and extending inward from the upper surface of the nanosheet, and a second

lower silicide layer provided on the nanosheet and extending inward from the lower surface of the nanosheet,

a second upper metal layer provided on the second upper silicide layer and a second lower metal layer provided on the second lower silicide layer, and

a second nanosheet region provided between the second upper silicide layer and the second lower silicide layer.

2. The integrated circuit semiconductor device of claim 1, wherein the nanosheet comprises a single layer which continuously extends in the first horizontal direction.

3. The integrated circuit semiconductor device of claim 1 or claim 2, wherein the nanosheet is spaced apart from a surface of the substrate, and a thickness of the nanosheet in a first vertical direction is greater than a thickness of the nanosheet in the second horizontal direction, the first vertical direction being perpendicular to the first and second horizontal directions.

4. The integrated circuit semiconductor device of any one of claims 1 to 3, wherein the nanosheet has a first thickness in a first region between the first gate electrode portion and the second gate electrode portion and a second thickness in a second region between the first upper silicide layer and the first lower silicide layer or between the second upper silicide layer and the second lower silicide layer, the first thickness being different from the second thickness.

5. The integrated circuit semiconductor device of any one of claims 1 to 4, wherein the first source/drain region further comprises first metal liner layers provided on the first

silicide layers, and the second source/drain region further comprises second metal liner layers provided on the second silicide layers.

6. The integrated circuit semiconductor device of any one of claims 1 to 5, further comprising:

a first through-electrode provided in the substrate and electrically connected to the first source/drain region,

a second through-electrode provided in the substrate and electrically connected to the second source/drain region,

a first backside power rail provided in a back surface of the substrate electrically connected to the first through-electrode, and

a second backside power rail provided in the back surface of the substrate electrically connected to the second through-electrode.

7. An integrated circuit semiconductor device comprising:

a plurality of nanosheets provided on a substrate, the plurality of nanosheets extending in a first horizontal direction and being spaced apart from a surface of the substrate and spaced apart from each other in a first vertical direction that is perpendicular to the first horizontal direction;

a gate electrode comprising a plurality of gate electrode portions provided on the plurality of nanosheets, the gate electrode extending in a second horizontal direction that is perpendicular to the first horizontal direction;

a plurality of gate insulating layers provided between the plurality of gate electrode portions and the plurality of nanosheets;

a first source/drain region provided on a first side of the plurality of nanosheets corresponding to the gate electrode; and

a second source/drain region provided on a second side of the plurality of nanosheets corresponding to the gate electrode,

wherein the first source/drain region comprises:

first silicide layers comprising a first upper silicide layer provided on a first nanosheet, among the plurality of nanosheets, and extending inward from an upper surface of the first nanosheet, and a first lower silicide layer on provided the first nanosheet and extending inward from a lower surface of the first nanosheet,

a first upper metal layer provided on the first upper silicide layer,

a first lower metal layer provided on the first lower silicide layer, and

a first nanosheet region provided between the first upper silicide layer and the first lower silicide layer, and

wherein the second source/drain region comprises:

second silicide layers comprising a second upper silicide layer provided on the first nanosheet and extending inward from the upper surface of the first nanosheet, and a second lower silicide layer provided on the first nanosheet and extending inward from the lower surface of the first nanosheet,

a second upper metal layer provided on the second upper silicide layer,

a second lower metal layer provided on the second lower silicide layer, and

a second nanosheet region provided between the second upper silicide layer and the second lower silicide layer.

8. The integrated circuit semiconductor device of claim 7, wherein each of the plurality of nanosheets comprises a single layer continuously extending from the gate electrode

to the first source/drain region in the first horizontal direction and continuously extending from the gate electrode to the second source/drain region in a first reverse horizontal direction.

9. An integrated circuit semiconductor device comprising:

a lower nanosheet provided on a substrate, the lower nanosheet extending in a first horizontal direction;

an upper nanosheet provided on the substrate, the upper nanosheet extending in the first horizontal direction and being apart from a surface of the substrate in a first vertical direction that is perpendicular to the first horizontal direction;

an isolation-insulating layer configured to insulate the lower nanosheet and the upper nanosheet from each other;

a gate electrode comprising a plurality of gate electrode portions provided on the upper and lower nanosheets, the gate electrode extending in a second horizontal direction perpendicular to the first horizontal direction;

a first source/drain region provided on a first side of the lower and upper nanosheets corresponding to the gate electrode; and

a second source/drain region formed on a second side of the lower and upper nanosheets with corresponding to the gate electrode,

wherein the first source/drain region comprises:

first silicide layers comprising a first upper silicide layer provided on the lower nanosheet and upper nanosheet and extending inward from an upper surface of the lower nanosheet and upper nanosheet, and a first lower silicide layer on provided the lower nanosheet and upper nanosheet and extending inward from a lower surface of the lower nanosheet and upper nanosheet,

a first upper metal layer provided on the first upper silicide layer,

a first lower metal layer provided on the first lower silicide layer, and

a first nanosheet region provided between the first upper silicide layer and the first lower silicide layer, and

wherein the second source/drain region comprises:

second silicide layers comprising a second upper silicide layer provided on the lower nanosheet and upper nanosheet and extending inward from the upper surface of the lower nanosheet and upper nanosheet, and a second lower silicide layer provided on the lower nanosheet and upper nanosheet and extending inward from the lower surface of the lower nanosheet and upper nanosheet,

a second upper metal layer provided on the second upper silicide layer,

a second lower metal layer provided on the second lower silicide layer, and

a second nanosheet region provided between the second upper silicide layer and the second lower silicide layer.

10. The integrated circuit semiconductor device of claim 9, further comprising:

a first spacer provided between the gate electrode and the first source/drain region;

a second spacer provided between the gate electrode and the second source/drain region,

wherein the isolation-insulating layer divides the plurality of gate electrode portions in the first vertical direction into first gate electrode portions corresponding to the lower nanosheet and second gate electrode portions corresponding to the upper nanosheet, and

wherein the isolation-insulating layer separates the first upper and lower metal layers and the second upper and lower metal layers.