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(54) IMPROVEMENTS IN OR RELATING TO SEMICONDUCTOR DEVICES

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195 Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices and has for its object the provision of a device in which information is storable in the form of electrical charge carriers.

According to this invention a semiconductor device comprises a semiconductive, electroluminescent, charge carrier storage medium, first means for storing or for permitting the storage of, when energised, electrical charge carriers at a first discrete site at or near a surface of said medium, and second means for transferring, when energised, said charge carriers through said medium to a second discrete site at or near said surface, said device being such that, in operation, a detectable radiative output is produced on recombination of said charge carriers with bulk carriers of said medium.

At least a portion of said surface may be covered with an insulating layer, and said first and second means may comprise respectively first and second electrodes on said layer.

There may be provided a plurality of said second electrodes on said layer defining a path along said surface.

In one embodiment of the invention a semiconductor device comprises an electroluminescent, semiconductive, medium of a first conductivity type, first means for storing or for permitting the storage of, when energised, electrical charge carriers of opposite type to the bulk carriers of said medium at a first discrete site at or near a surface of said medium, a plurality of spaced localised zones of opposite type conductivity disposed adjacent said surface of and forming a corresponding plurality of p—n junctions with said medium, and insulating layer disposed over said surface covering said plurality of zones, a plurality of localised conductive electrodes for transferring, when energised, said charge carriers from said site to a said zone and from zone to zone, each of said plurality of electrodes being disposed over said insulating layer and registered in one-to-one correspondence with said plurality of zones and delimited in lateral extent so as to extend only over substantially all of the space between a pair of said zones and over a portion of one zone of the pair of zones, each said portion being sufficiently large that the capacitance between the electrode and said one zone is substantially larger than the capacitance between the electrode and the other zone of said pair of zones, said device being such that, in operation, a detectable radiative output is produced on recombination of said charge carriers with bulk carriers of said medium. Said first means may comprise a zone of said opposite conductivity type disposed adjacent said surface and forming with said medium a p—n junction, and a conductive electrode contacting said zone.

There may be provided apparatus including a device in accordance with the invention, means for energising said first means to store said charge carriers at said first site, means for energising said second means or said

plurality of electrodes to transfer said charge carriers to said or a said second site or zone, and means for permitting or causing said charge carriers to recombine with the bulk carriers in said medium.

The apparatus may include means for detecting said radiative output, e.g. a photocathode. There may be provided display means for producing a visible display in response to electrons incident thereon and means for focussing the electron image emitted by said photocathode in response to said radiative output onto said display means.

The apparatus may include means coupled to said device for taking off an electrical output signal representative of said charge carriers (if any) at an output position in said medium, and said means for energising said first means may include means for coupling said signal or a signal derived therefrom to said first means.

The invention will now be described and explained with reference to the accompanying drawings, in which:

Figs. 1a to 1d are schematic diagrams illustrating the charge translating mechanism;

Fig. 2 is a front sectional view, partly schematic, of a shift register;

Fig. 3 is a pulse program for the shift register of Fig. 2;

Fig. 4 is a front sectional view, partly schematic, illustrating a preferred method of charge translation;

Figs. 5a, 5b and 5c are schematic representations of means for detecting the prsence or absence of charge at an output position;

Figs. 6a and 6b are schematic representations provided to explain enhancement of charge translation;

Fig. 7 is a plan view of a multichannel shift register, an elaboration of that of Fig. 2;

Fig. 8 is a front section, largely schematic, of an image detection device;

Fig. 9 shows a front sectional view of a device in accordance with the invention;

Fig. 10 shows a front sectional view of another device in accordance with the invention;

Fig. 11 is a schematic diagram for recirculating video information and useful in connection with the device of Fig. 9; and

Fig. 12 is a schematic diagram of a display apparatus embodying the invention.

The charge transfer mechanism will first be described with reference to Figs. 1a to 1d. In Fig. 1a a semiconductor substrate 10 is covered with a thin insulating film 11 and two metal electrodes 12 and 13 which form part of an array. As shown, electrode 12 is biased while electrode 13 is not and a depletion region or potential well 14 forms under electrode 12. In Fig. 1b, minority charges 15, created by, for example, hole-electron pair generation from photon absorption, are shown migrating to the depletion region 14 and stored there. When electrode 13 is biased simultaneously with electrode 12, the depletion region extends continuously below both electrodes as shown in Fig. 1c and the charge redistributes across the enlarged layer. As the bias on electrode 12 is removed, as shown in Fig. 1d, the portion of the depletion region under electrode 12 collapses shifting all the charge to the potential well 14′ that is now associated with electrode 13. In a like manner the charge entity represented in Fig. 1d can be shifted stepwise to any location in the semiconductor. It will be recognised that the substrate 10 of Figs 1a to 1d can be P-type and the charges reversed in sign.

This translating mechanism is illustrated in connection with the shift register of Fig. 2 the structure of which is similar to that of Figs. 1a to 1d. A semiconductor substrate 20 is covered with dielectric layer 21 on which is formed a sequence of electrodes 22 to 24 in triplets designated *a* and *b* to *n* (being part of a series terminating with 24*n*). Conductors designated 22′, 23′ and 24′ join each third electrode. The input or generating stage 25 is an MIS device driven to avalanche condition. The charge generated at 25 migrates as shown to the potential well 27*a*.

The shift register can be operated in a recirculating mode either for increasing the storage duration, or for regenerating the signal to overcome noise or charge losses, by simply connecting the output signal back to the input stage through an appropriate regeneration circuit 33. Clearly also the shift register finds application in information or signal delay. By sequentially biasing conductors 23′, 24′ and 22′, the charge will shift into pocket 27*b*. In a like manner the charge is translated into pocket 27*n* and then into the depletion region 28 accompanying the p—n junction 29 of the output stage. A pulse output is then detected across load 30 as shown. A bias source 31 is connected to electrode 32 to bias the junction. An equally effective detector is a Schottky barrier device which may be as described in The Bell System Technical Journal, Vol. XLIV, No. 7, Sept. 1965 at pp. 1525—1528.

An exemplary pulse program for the shift register of Fig. 2 is shown in Fig. 3 which illustrates transmission of the binary code 1101. It is clear from Fig. 2 that each element 22*a* to 22*n* is simultaneously pulsed via conductor 22′; likewise for conductors 23′ and 24′. The pulses on each element are timed such that the time period between the initiation of sequential pulses, Δt, is less than three times the pulse width, t_p. This ensures that the pulse on each sequential stage overlaps both the former and the subsequent stage. Otherwise one potential may well collapse

before the next one is accessible to its charge.

Referring back to Fig. 1c, it will be appreciated that the charge transfer time for that portion of charge situated under electrode 12 will be equal to the fall time of the pulse in Fig. 3. Experimental evidence indicates that the transfer time under the conditions outlined is quite fast. However, if the pulse program of Fig. 3 is comparably fast, it may be advantageous to use a pulse shape that gives a longer fall time, e.g. a sine wave.

Preferably a continuous uniform bias is applied to all conductors so as to maintain at least a shallow depletion layer over the entire surface of the device. This bias should be at least equal to the threshold voltage for producing inversion under steady state conditions. In this way troublesome surface states, which are inevitably present at semiconductor-insulator interfaces (and which cause adverse surface recombination), can be maintained relatively free of majority carriers. Thus by isolating the bulk of the majority carriers from the interface via a space-charge layer, the carriers in the surface states, having once recombined with minority carriers, cannot then be replenished. A prebias on every metal contact or on the substrate, ensures a long lifetime for the minority carriers constituting the signal. In a device having many stages this expedient may be essential.

This is illustrated in Fig. 4 in which the device shown corresponds to a middle portion of the shift register of Fig. 2. The semiconductor base layer 40, which again is n-type, the insulating layer 41, and metal contacts 42*a*, 43*a*, 44*a*, 42*b*, 43*b* and 44*b* and the associated conductors 42′, 43′, and 44′ correspond to similar elements in Fig. 2. A continuous bias voltage V′ on all conductors forms a uniform depletion region 45 over the entire device. Potential wells 46 are formed under contacts 42*a* and 42*b* as the result of the pulse voltage V_p superimposed on the bias voltage V′.

Although the shift register of Fig. 2 was described as having an avalanche device for creating charge at the input location 25, there are several alternative methods for creating minority charge carriers. For example, if the input stage comprises a p—n junction, minority charge carriers can be injected into the bulk region of the semiconductor by forward bias pulses corresponding to the desired input signal. Alternatively carriers can be injected by MIS surface avalanching as described in Journal of Applied Physics, Vol. 9, No. 12, p. 444. A hybrid structure employing a metal-oxide surface contact on a p—n junction is effective for the same purpose. Another alternative is to generate hole electron pairs by photon absorption or absorption of other ionising radiation as described in copending U.K. application No. 25936/69 (serial no. 1,241,379). The minority charge carriers will diffuse to a nearby depletion region which in the case of the shift register of Fig. 2 is the first stage 27*a*. A means for achieving this is shown in dotted lines at 33 in Fig. 2. The element 33 is a light source—in this case, a schematic representation of an electroluminescent diode.

The output stage can also assume a variety of forms. Figs. 5a to 5c illustrate a few alternatives. These figures show the terminal section of the device of Fig. 2 including the last transfer stage 24*n*. Each of these detectors is a charge detection device constructed according to known principles. In Fig. 5a the detector is an MIS device and is therefore especially convenient, from a processing standpoint, where an MIS array comprises the transfer stages. With the semiconductor depleted, the capacitance associated with detector electrode 50 will indicate the presence or absence of externally introduced charge in the depleted region 51. The capacity across the MIS detector is measured by a standard capacitive bridge as shown and the value indicated by a detector 52. The bias source 53 is arranged via switch 54 to intermittently bias that portion of the semiconductor below electrode 50 first to establish the depletion region for attracting the charge to be detected, and then to collapse the depleted region to recombine the charge which may have accumulated.

In the detection stage of Fig. 5b an alternating current source 55 is connected to two adjacent field plates 56 and 57, the latter again comprising MIS devices with semiconductor 20 and insulating layer 21. A bias source 58 maintains a depletion region 59 beneath both electrodes 56 and 57. If charge is present in the terminal transfer stage 24*n* it is transferred to the potential well accompanying plate 56 on its negative half cycle and then towards the well of electrode 57 on the latter's negative half cycle. This transfer of charge back and forth beneath electrodes 56 and 57 changes the a.c. impedance of the circuit from its value without charge in the depletion regon. The presence or absence of charge is thus detectable across impedance 60 by potentiometer 61. The switch 62 functions to erase the charge in the manner of switch 54 of Fig. 5a. The speed of erase can be enhanced by providing a switching network to reverse the d.c. bias rather than merely removing the bias.

The detection stage of Fig. 5c relies on a direct voltage measurement to detect interface charge Q_I accumulated between semiconductor 20 and insulator 21. An electrode 63 is biased negatively via a source 64 connected in series with a blocking capacitance which is shown as a capacitor 65, but may alternatively be a diode. A change in the charge level Q_I is reflected by a change in the equivalent capacitance of the MIS device. This affects

the capacitive division between that element and the capacitor 65 resulting in a change in V_D. The voltage V_D can be measured in various ways, e.g. at the gate of a field-effect transistor shown integrated with the semiconductor base 20 of the storage device. A p-region 20A is shown representing isolation according to known integrated circuit techniques. The voltage V_D being measured is connected to the gate electrode 66. The insulating layer for the gate is shown as an extension of insulating layer 21. Source and drain regions 67 and 68 are diffused through windows formed in this layer. Source and drain electrodes 69 and 70 are connected through load 71 to bias source 72. Detector 73 indicates the conduction state of the FET which reveals the presence or absence of charge Q_I in the following manner.

A positive pulse delivered by power source 64 recombines any residual charge Q_I and primes the device for detection. A negative pulse places negative charge on plate 63 and depletes the region under that electrode for collecting holes delivered (or not delivered from terminal stage 24*n*. The gate 66 is biased at the same potential leaving the FET in an "on" condition indicated at 73. If charge Q_I enters the region below plate 63, the negative potential on the plate will be reduced. The corresponding reduction in potential at the gate electrode 66 will place the FET in an "off" condition. If there is no charge Q_I the FET remains "on".

The device of Fig. 5c is shown partly integrated. The FET device can be used separately or the device can be further integrated, e.g. the elements 65, 71 and the electrical connections can be integrated.

The charge translating mechanism described in connection with Fig. 1 relies on thermal diffusion to transport carriers from potential well 14 to potential well 14'. While this transport mechanism is adequate, the response time of devices using this mechanism can be significantly reduced by using an electric field to drive the charge to the new location. In many cases the use of the drive field will also improve the collection efficiency. One means of achieving this is to shape the potential well so that a field gradient exists between adjacent wells. This, which for the purpose of this description will be termed "field enhancement," will be described by way of example with reference to Figs. 6a and 6b.

Fig. 6a shows two conductors 72 and 73 situated on insulating layer 74 which in turn covers semiconductor substrate 75. With the conductors 72 and 73 biased, their respective depletion layers appear to have shapes indicated by dashed lines 76 and 77. These lines are a function of the field potential at the semi-conductor-insulation interface. Thus it is convenient in this discussion to consider these boundary lines as field profiles along the surface of the semiconductor where the charge is stored. As a consequence of making the dimensions of the electrode comparable to, or less than, the thickness of the insulator, the field approaches the situation where it appears to emanate as if from a point rather than a plane (as in Fig. 1) and produces a continuous field gradient along the surface. This field gradient is aptly described as a potential well and tends to confine the charge at its centre. When these wells are made to overlap (a condition implicit from the previous discussion, e.g. the pulse program of Fig. 3) the composite field profile is described by the chain-doted line 78 of Fig. 6a. Now it is intuitively obvious that the charges will transport from the region directly under electrode 72 toward electrode 73. After the depletion field represented by line 76 collapses, the charges will be swept to the surface region of highest potential in the well represented by line 77, or directly under electrode 73.

Field enhancement can be made more effective by using a shaped pulse as shown in Fig. 6b. For example, if a saw-tooth pulse is applied to electrodes 72 and 73, then at a time t_1 during the period of pulse overlap (the charge translating period), electrode 72 will be biased at a lower voltage than electrode 73. The separate field profiles at t_1 are described by dashed lines 79 and 80 with the composite profile appearing as dotted line 89. The field gradient in the direction of desired charge translation extends instantaneously all the way to the region immediately below electrode 73.

Other ways of producing a field gradient or drive field will occur to those skilled in the art.

A multichannel register will now be described with reference to Fig. 7. It is evident that the linear array of Fig. 2 requires at least *n* crossovers (the figure shows $3n-3$ crossovers but a straightforward modification reduces this number to *n*). Crossovers are used more economically in the arrangement of Fig. 7 wherein the same number of crossovers may provide a large number of channels. Fig. 7 shows four channels but this number can be extended without adding additional crossover connections. The conductor arrangement of conductors 81', 82' and 83' is the same as that in Fig. 2 with conductor 81' connected to contacts 81*a* to 81*n* in sheet 86 and likewise with conductors 82', 83' and electrodes 82*a* to 82*n* and 83*a* to 83*n*. Input stages 84 and output stages 85 have been discussed previously.

This multichannel shift register has many practical uses, e.g. multiplexing. For example, the four channels shown can be filled concurrently, then dumped sequentially on a common transmission line.

This would suggest a slightly more elaborate drive field and switching network than that shown in Fig. 7 as the electrodes of

each channel would require independent biasing. A way of avoiding independent biasing is to use the common conductor arrangement of Fig. 7 and to recirculate all channels except the one being read into the multiplexing signal. This would require only a single switch for each channel.

Various other mutiplexing arrangements will occur to those skilled in the art. For example, if the inputs to all channels are simultaneously sampled, different time delays can be built into each channel by varying the number of storage sites. The common output of all channels will then be multiplexed in time division.

Minority charge carriers may be produced in the semiconductor by photon absorption, as mentioned previously, and as described in United States Patent No. 3,403,284. One form of device using this mechanism is a video camera target one form of which is illustrated schematically in Fig. 8. The essential characteristic of this class of device is parallel read-in of information. Light in the form of the optical image being recorded is incident on the side of the semiconductor 90 opposite to the storage control elements. The latter again comprise metal-insulator-semiconductor devices as in Fig. 2 or other types of depletion layer devices such as transistor-type structures. The array shown contains three bit locations comprising three electrodes designated 92*a* to 94*a*, 92*b* to 94*b*, and 92*c* to 94*c* connected to conductors 92′, 93′ and 94′ in a manner similar to the arrangement of Fig. 2. Except for the parallel read-in, the charge translation and readout operation can follow the teachings described above. The linear array shown in Fig. 8 may represent one raster line in a video system. The charge is stored at locations 92*a*—92*c* during the optical integration period. It may be read out serially by translating the charge to the readout section (refer to Fig. 2). By sequentially reading each raster line, the video frame is constructed.

In accordance with the invention devices similar to those described can be used in a parallel readout made for optical display. An example will be described with reference to Fig. 9. The semiconductor 100 which, while serving the function described in connection with Figs. 1a to 1d, is also chosen for the property of efficient light emission with charge recombination. Gallium arsenide is a good example of such a semiconductor although its emission is in the infrared. For visible displays it would be necessary to use a secondary emissive coating on the output face of the device as shown for example at 106. Such coatings are known in the art and are described in copending U.K. applications Nos. 18162/70; 18161/70; 18164/70 (serial nos. 1,317,732, 1,317,731, and 1,313,395). Other semiconductor materials will occur to those skilled in the art. Insulating layer 101, electrodes 102*a*, 103*a*, and 104*a*, conductors 102′, 103′ and 104′ and input stage 105 correspond to similar elements in Fig. 2. For video display, the video signal is read into the input stage and stepped along to the storage sites. In this device an output stage is not essential. When the line is filled the switch 107 is opened removing the bias at each electrode, e.g. electrode 104*a*, and collapsing the depletion regions. The stored carriers recombine with majority carriers entering the storage region to generate a light output that has a local intensity representative of the amount of charge at each site. The use of a direct bandgap semiconductor such as GaAs would also ensure that light emission in the direction away from the surface would be efficiently absorbed rather than scattered to appear at a different location. As in a conventional display, each line may represent a single raster line in normal video frame.

A preferred form of the device additionally includes a bias source 108 which, as discussed in connection with Fig. 4, maintains a uniform depletion region in the device during the writing operation. This inhibits spontaneous recombination during the writing operation.

An alternative shift register structure utilising carrier recombination for producing a light display is shown in Fig. 10 in combination with a signal generator and clock pulse generator. As shown, the monolithic structure 110 includes a bulk portion 112 of a first type conductivity semiconductive material (shown illustratively as N-type) adjacent the surface of which there are a plurality of localised zones 117*a* to 117*n* and 118*a* to 118*n* of the other type conductivity, i.e. P-type. The surface of the wafer is covered with a dielectric layer 114 upon which there are formed a plurality of electrodes 115*a* to 115*n* and 116*a* to 116*n* registered in a one-to-one correspondence with the plurality of localised zones. Conductors designated 115′ and 116′ are connected to each second electrode, i.e. to electrodes 115*a*—115*n* and 116*a*—116*n*, respectively. An input zone 120 is connected through electrode 119 to an input terminal 122.

Each pair of closest zones, e.g. 120 and 117*a*, 117*a* and 118*a*, 118*a* and 117*b*, etc. may be thought of as the source and drain of an insulated gate field effect transistor (IGFET). It will be appreciated then that one of the electrodes 115*a*—115*n* and 116*a*—116*n* may be thought of as the gate electrode of an IGFET and the N-type surface portion between any pair of closest zones will be thought of as the channel of an IGFET.

It should be noted that each of the electrodes is delimited in lateral extent so as to extend over substantially all of the space

between a pair of closest zones, i.e. over the channel, and over a substantial portion of one of its pair of zones so that the capacitance between the electrode and the zone over which it extends is substantially greater than the capacitance between the electrode and the other zone of its pair of zones. More specifically, and for example, electrode 116*a* overlies the N-type portion between zones 117*a* and 118*a* and overlies a much greater portion of zone 118*a* than of zone 117*a*.

In operation, clock pulses $\phi 1$ and $\phi 2$, supplied by two-phase clock means 129, are applied to conduction paths 115′ and 116′ respectively. Electrodes 115*a*—115*n*, connected to conduction path 115′, and electrodes 116*a*—116*n*, connected to conduction path 116′, simultaneously are driven alternatively positive and negative as ϕ_1 and ϕ_2, respectively, alternate between positive and negative potentials.

Bulk portion 112 is shown connected through an ohmic contact (metallic electrode 113) to ground. Of course, electrode 113 need not be connected to ground, but may be connected to any fixed reference potential provided the clock voltages are correspondingly adjusted. It is advantageous for the electrode 113 to be essentially transparent or preferably omitted altogether if the n^+ conductivity is sufficiently high.

Assume that at time equals zero, ϕ_1 is pulsed to its most negative value and ϕ_2 is pulsed to its most positive value. If the ϕ_1 pulse is sufficiently negative, i.e. more negative than some threshold voltage V_T, the gate electrodes numbered 115 (115*a*—115*n*) induce a P-type surface channel in the N-type silicon surface portions underlying those gate electrodes. The localised surface zones 117 (117*a*—117*n*) also are driven negative because of the capacitive coupling between electrodes 115 and zones 117. Since at this time ϕ_2 is pulsed positive, electrodes 116 (116*a*—116*n*) tend to inhibit the formation of P-type channels in those N-type surface portions thereunder; and, because of the capacitive coupling between electrodes 116 and zones 118 (118*a*—118*n*—1), zones 118 are all driven positive. Notice that electrode 116*n* need not substantially overlap zone 118*n* because zone 118*n* is held at a negative bias by output circuitry including, for example, a battery 130 in series with a resistor 131.

Correspondingly, when the clock pulses reverse polarity one-half clock cycle later, electrodes 116 induce P-type channels thereunder and tend to drive zones 118 negative while electrodes 115 inhibit P-type channels thereunder and tend to drive zones 117 positive.

For the purpose of discussion, we define V_N to be the most negative clock voltage and V_P to be the most positive clock voltage. The threshold voltage V_T is a gate voltage at which the N-type surface is just beginning to invert to P-type.

If the input is left floating so that no charge can be introduced at input zone 120, and if the clock is allowed to run for a while, the system reaches a steady state where the potentials of localised zones 117 and 118 alternate between $V_N—V_T$ and $2V_N—V_P—V_T$ at each reversal of the clock pulse. For example, if $V_T=-2$ volts, $V_N=-6$ volts, and $V_P=0$, the potentials of zones 117 and 118 will alternate between −4 volts and −10 volts at each reversal of the clock. As the N-type portion 112 is grounded, these negative voltages on zones 117 and 118 cause all of the pn junctions between those zones and the bulk to be reverse-biased. Consequently, at this steady state, there is a deficiency of majority carriers (holes) in each of zones 117 and 118.

Assume now that a number of majority carriers are introduced into input zone 120 during one of the times when ϕ_1 is most negative. This can be done, for example by applying a voltage to input terminal 122 sufficient to make the voltage between the input zone 120 and electrode 115*a* greater than the threshold voltage V_T. Because the negative voltage on electrode 115*a* has induced a P-type surface channel between zones 120 and 117*a*, and because zone 117*a* is negative with respect to zone 120, those majority carriers will transfer to the right into zone 117*a*.

If the potentials of the clock lines 115′ and 116′ are now reversed, such that a positive voltage is applied to electrodes 115 and a negative voltage is applied to electrodes 116, surface channels will be induced under electrodes 116 and inhibited under electrodes 115. Additionally, zones 118 will become more negative than zones 117 because of the capacitive coupling. Accordingly, those majority carriers will transfer another step to the right into zone 118*a*. In like fashion, at each interval of the clock polarity, those majority carriers will transfer sequentially to the next zone to the right.

Similarly, if when clock pulse ϕ_1 is negative input zone 120 is made negative with respect to electrode 115*a* no excess majority carriers (above the steady state deficiency level) will be transferred during that clock cycle from zone 120 to zone 117*a*. Accordingly at the reversal of the clock pulse there will be no net charge to transfer from 117*a* to 118*a*. Thus either a quantity of charge or the absence of such a quality is shifted step by step in digital shift register fashion towards the output.

When the shift register is filled the stored carriers are recombined to give a light output with a localised intensity corresponding to the amount of charge stored at a given site. With the device of Fig. 10 this is achieved by applying a positive pulse to all electrodes via

output bias 134. This drives all the diodes into forward bias thereby injecting the holes stored in the respective storage sites into the bulk region 112 where they combine according to well-known principles and emit light. The semiconductor wafer 112 should be thin for optimum output and to avoid loss of resolution due to internal reflection. For this purpose a thickness of less than 40μ and preferably less than 20μ is recommended.

Preferably signal generator 123, resistor 124, and circuitry 126 are provided for the purpose of maintaining a continual bias on the electrodes even when a "zero" is being transferred. This is described in more detail in copending application no. 21831/71 (Serial No. 1,340,618).

The device of Fig. 10 has much the same application as the device of Fig. 9. For example, if the information shifted into the register is a video line the output will be a video image.

In some cases a brighter image may be desired than that obtained with the display devices of Figs. 9 and 10. This can be achieved with the arrangement indicated schematically in Fig. 11. Here a line of the video signal is stored in a regenerative circulating memory 140 which may be the device of Fig. 2. After the line is read into the memory, part of the signal is transmitted to the appropriate line of the video display 141. The other part is recirculated. A desired signal level (this can be even stronger than the level of the original) can be restored by the regenerative circuit. With appropriate switching apparatus, the start of a new video line at the video input acts as a clocking pulse to open the circulating circuit and dump the old information. The line repetition rate in the video display corresponds to the frame time multiplied by the number of lines, rather than simply the frame time as in the usual system. Thus the amount of light generated over the frame interval will be larger by a factor equal to the number of video lines. Another consequence of this system is that the frame period can be adjusted within reasonable limits with no possibility of flicker. By extending the frame time, transmission bandwidth can be reduced. The light decay in this device can be very fast compared with that of typical phosphors so that there would be no image persistence. The very high field rate of such a display also eliminates the need for bandwidth saving display schemes, which contribute objectionable features to the display. For example, the use of interlace produces line crawl or interline flicker. A simple line sequential raster formation is all that is necessary.

With the present state of the art the size of the display would be limited by cost considerations for the semiconductor device. It is preferable not to design a direct viewing display device, but instead the display device just described could be used in conjunction with a photocathode and phosphor display screen to enlarge the image as shown in Fig. 12. The vacuum tube envelope 150 contains the usual phosphor screen 151. The electron source in this case is the photocathode 152. Conventional focussing means not shown are used to image the electron pattern from the photocathode onto the display screen 151. The photocathode is driven with the optical device 153 which has a storage device having the functional elements of Fig. 9 or Fig. 10. The luminescent output of the storage device is imaged on the photocathode by a lens system indicated schematically at 154. It is apparent that for this device the luminescent output from the storage device 153 does not have to be visible. Therefore gallium arsenide, which emits efficiently in the infrared, is an appropriate semiconductor for the storage device. Appropriate photocathode materials and phosphors are well known in the art. Image converters are of course widely known, often functioning as image intensifiers and by simply reversing the optics the proposed image expander is obtained. The essential difference in this device is in the element used to drive the photocathode, i.e. the novel storage and display unit 153. It will be appreciated that the scanning function is served in a highly controlled manner by the semiconductor storage element so that the electron tube requires simply a magnetic or electrostatic focussing arrangement. The elimination of electron beam scanning leads to greater reliability, and cost reduction as compared to a conventional cathode ray tube.

It may also allow improvement in resolution since the instantaneous current density can be considerably less than in a cathode ray tube in a single scanned electron beam.

The described devices can be fabricated using gallium arsenide diodes according to well-established technology. A high efficiency GaAs electroluminescent device is described in *IEEE Trans. Electron Devices*, ED-12, 531 (1965). Insulators such as SiO_2, and combinations of SiO_2—SiN, SiO_2—Al_2O_3, etc. are useful as the insulating layer. Known electrode materials are gold, aluminium and doped-silicon. The device of Figs. 9 and 10 could employ gallium arsenide as the base layer and 1,000 Å to 2,000 Å of deposited SiO_2 as the insulating layer. The electrodes may be gold in any typical thickness, e.g. 0.1 to a few microns.

Reference is directed to our copending applications nos. 21831/71 and 21832/71 (Serial Nos. 1,340,618 and 1,340,619) which relate to devices in which information is storable in the form of charge carriers.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a

output bias 134. This drives all the diodes into forward bias thereby injecting the holes stored in the respective storage sites into the bulk region 112 where they combine according to well-known principles and emit light. The semiconductor wafer 112 should be thin for optimum output and to avoid loss of resolution due to internal reflection. For this purpose a thickness of less than 40μ and preferably less than 20μ is recommended.

Preferably signal generator 123, resistor 124, and circuitry 126 are provided for the purpose of maintaining a continual bias on the electrodes even when a "zero" is being transferred. This is described in more detail in copending application no. 21831/71 (Serial No. 1,340,618).

The device of Fig. 10 has much the same application as the device of Fig. 9. For example, if the information shifted into the register is a video line the output will be a video image.

In some cases a brighter image may be desired than that obtained with the display devices of Figs. 9 and 10. This can be achieved with the arrangement indicated schematically in Fig. 11. Here a line of the video signal is stored in a regenerative circulating memory 140 which may be the device of Fig. 2. After the line is read into the memory, part of the signal is transmitted to the appropriate line of the video display 141. The other part is recirculated. A desired signal level (this can be even stronger than the level of the original) can be restored by the regenerative circuit. With appropriate switching apparatus, the start of a new video line at the video input acts as a clocking pulse to open the circulating circuit and dump the old information. The line repetition rate in the video display corresponds to the frame time multiplied by the number of lines, rather than simply the frame time as in the usual system. Thus the amount of light generated over the frame interval will be larger by a factor equal to the number of video lines. Another consequence of this system is that the frame period can be adjusted within reasonable limits with no possibility of flicker. By extending the frame time, transmission bandwidth can be reduced. The light decay in this device can be very fast compared with that of typical phosphors so that there would be no image persistence. The very high field rate of such a display also eliminates the need for bandwidth saving display schemes, which contribute objectionable features to the display. For example, the use of interlace produces line crawl or interline flicker. A simple line sequential raster formation is all that is necessary.

With the present state of the art the size of the display would be limited by cost considerations for the semiconductor device. It is preferable not to design a direct viewing display device, but instead the display device just described could be used in conjunction with a photocathode and phosphor display screen to enlarge the image as shown in Fig. 12. The vacuum tube envelope 150 contains the usual phosphor screen 151. The electron source in this case is the photocathode 152. Conventional focussing means not shown are used to image the electron pattern from the photocathode onto the display screen 151. The photocathode is driven with the optical device 153 which has a storage device having the functional elements of Fig. 9 or Fig. 10. The luminescent output of the storage device is imaged on the photocathode by a lens system indicated schematically at 154. It is apparent that for this device the luminescent output from the storage device 153 does not have to be visible. Therefore gallium arsenide, which emits efficiently in the infrared, is an appropriate semiconductor for the storage device. Appropriate photocathode materials and phosphors are well known in the art. Image converters are of course widely known, often functioning as image intensifiers and by simply reversing the optics the proposed image expander is obtained. The essential difference in this device is in the element used to drive the photocathode, i.e. the novel storage and display unit 153. It will be appreciated that the scanning function is served in a highly controlled manner by the semiconductor storage element so that the electron tube requires simply a magnetic or electrostatic focussing arrangement. The elimination of electron beam scanning leads to greater reliability, and cost reduction as compared to a conventional cathode ray tube.

It may also allow improvement in resolution since the instantaneous current density can be considerably less than in a cathode ray tube in a single scanned electron beam.

The described devices can be fabricated using gallium arsenide diodes according to well-established technology. A high efficiency GaAs electroluminescent device is described in *IEEE Trans. Electron Devices*, ED-12, 531 (1965). Insulators such as SiO_2, and combinations of SiO_2—SiN, SiO_2—Al_2O_3, etc. are useful as the insulating layer. Known electrode materials are gold, aluminium and doped-silicon. The device of Figs. 9 and 10 could employ gallium arsenide as the base layer and 1,000 Å to 2,000 Å of deposited SiO_2 as the insulating layer. The electrodes may be gold in any typical thickness, e.g. 0.1 to a few microns.

Reference is directed to our copending applications nos. 21831/71 and 21832/71 (Serial Nos. 1,340,618 and 1,340,619) which relate to devices in which information is storable in the form of charge carriers.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a

semiconductive, electroluminescent, charge carrier storage medium, first means for storing or for permitting the storage of, when energised, electrical charge carriers at a first discrete site at or near a surface of said medium, and second means for transferring, when energised, said charge carriers through said medium to a second discrete site at or near said surface, said device being such that in operation a detectable radiative output is produced on carriers of said medium.

2. A device as claimed in claim 1 wherein at least a portion of said surface is covered with an insulating layer, and said first and second means comprise respectively first and second electrodes on said layer.

3. A device as claimed in claim 2 wherein there are a plurality of said second electrodes on said layer defining a path along said surface.

4. A semiconductor device comprising an electroluminescent, semiconductive, medium of a first conductivity type, first means for storing or for permitting the storage of, when energised, electrical charge carriers of opposite type to the bulk carriers of said medium at a first discrete site at or near a surface of said medium, a plurality of spaced localised zones of opposite type conductivity disposed adjacent said surface of and forming a corresponding plurality of p—n junctions with said medium, an insulating layer disposed over said surface covering said plurality of zones, a plurality of localised conductive electrodes for transferring, when energised, said charge carriers from said site to a said zone and from zone to zone, each of said plurality of electrodes being disposed over said insulating layer and registered in one-to-one correspondence with said plurality of zones and delimited in lateral extent so as to extend only over substantially all of the space between a pair of said zones and over a portion of one zone of the pair of zones, each said portion being sufficiently large that the capacitance between the electrode and said one zone is substantially larger than the capacitance between the electrode and the other zone of said pair of zones, said device being such that, in operation, a detectable radiative output is produced on recombination of said charge carriers with bulk carriers of said medium.

5. A device as claimed in claim 4 wherein said first means comprises a zone of said opposite conductivity type disposed adjacent said surface and forming with said medium a pn junction, and a conductive electrode contacting said zone.

6. A device as claimed in any one of claims 2 to 5 wherein said insulating layer is of or includes SiO_2.

7. A device as claimed in any one preceding claim wherein said medium is gallium arsenide.

8. Apparatus including a device as claimed in any one preceding claim, means for energising said first means to store said charge carriers at said first site, means for energising said second means or said plurality of electrodes to transfer said charge carriers to said or a said second site or zone, and means for permitting or causing said charge carriers to recombine with the bulk carriers in said medium.

9. Apparatus as claimed in claim 8 including means for detecting said radiative output.

10. Apparatus as claimed in claim 9 wherein said detecting means comprises a photocathode.

11. Apparatus as claimed in claim 10 including display means for producing a visible display in response to electrons incident thereon, and means for focussing the electron image emitted by said photocathode in response to said radiative output onto said display means.

12. Apparatus as claimed in claim 8 including means coupled to said device for taking off an electrical output signal representative of said charge carriers (if any) at an output position in said medium.

13. Apparatus as claimed in claim 12 wherein said means for energising said first means includes means for coupling said signal or a signal derived therefrom to said first means.

14. A device or apparatus adapted to provide a detectable radiative output substantially as herein described with reference to Fig. 9, 10, 11 or 12 of the accompanying drawings.

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