CLAIMS

WHAT IS CLAIMED IS:

1. A one time programmable (OTP) memory comprising:

an OTP cell array including a plurality of OTP cells and configured to store OTP key values in the plurality of OTP cells arranged at intersections of a plurality of word lines and a plurality of bit lines; and

a control circuit configured to receive an erase instruction signal and erase all the OTP key values by programming the plurality of OTP cells to an identical OTP key value in response to the erase instruction signal having a first logic level,

wherein a first OTP cell of the plurality of OTP cells comprises:

a first transistor including a gate connected to a program word line and configured to store a first OTP key value;

a second transistor including a gate connected to a read word line and configured to read the first OTP key value; and

a bit line connected to a drain of the second transistor and configured to transmit the first OTP key value, and

wherein the control circuit comprises:

a first logic gate configured to receive a first signal and the erase instruction signal, and output a program word line signal to the program word line based on the first signal and the erase instruction signal; and

a second logic gate configured to receive a second signal and the erase instruction signal, and output a read word line signal to the read word line based on the second signal and the erase instruction signal.

2. The OTP memory of claim 1, wherein the control circuit is configured to erase all

the OTP key values when a power is on in the OTP memory.

3. The OTP memory of claim 1 or claim 2, wherein the control circuit is connected to an external circuit, and configured to receive the erase instruction signal at a first node through the external circuit connected to either a power source or a ground.

4 The OTP memory of any one of claims 1 to 3, wherein the control circuit is configured to erase the first OTP cell by breaking an oxide film of the first transistor.

5. The OTP memory of any one of claims 1 to 4, wherein the control circuit further comprises:

a bit line logic circuit configured to receive a third signal and the erase instruction signal, and determine a bit line signal of the bit line based on the third signal and the erase instruction signal.

6. The OTP memory of claim 5, wherein the control circuit is configured to program the plurality of OTP cells to an identical key value regardless of the first to third signals in response to the erase instruction signal having the first logic level.

7. The OTP memory of claim 5 or claim 6, further comprising:

a read circuit configured to compare the bit line signal to a reference signal, and output the first OTP key value based on a result of the comparison.

8. A storage device comprising:

a one time programmable (OTP) memory including a plurality of OTP cells and configured to store OTP key values in the plurality of OTP cells;

an erase instruction circuit that is detachably mounted on the storage device and connected to the OTP memory; and

a controller configured to encrypt data stored in the storage device by using the OTP key values,

wherein when the erase instruction circuit is removed from the storage device, the OTP memory is configured to receive the erase instruction signal having a first logic level and permanently erase all the OTP key values stored in the plurality of OTP cells by programming the plurality of OTP cells to an identical OTP key value in response to the erase instruction signal having the first logic level, and

wherein when the erase instruction circuit is mounted on the storage device, the OTP memory is configured to receive the erase instruction signal having a second logic level opposite the first logic level through the erase instruction circuit and program a target OTP cell of the plurality of OTP cells to an OTP key value in response to the erase instruction signal having the second logic level.